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Hybrid GaN and CMOS Integrated Module Radiation Hard DC-to-DC Converter

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A radiation-hard, compact, low-mass, hybrid GaN and CMOS integrated module DC-DC converter has been designed with an input voltage of up to 14V regulated down to an output voltage of 1.5V, with 6A maximum load current. The converter exhibits greater than 70% efficiency. Discrete GaN transistors are used for the power stage, and the controller circuitry and power device drivers are integrated on a 0.35um CMOS chip. Radiation hardening by design (RHBD) techniques have been employed to meet TID levels greater than 150 megarad (Si). This work presents the design and successful measurement results of the custom-designed CMOS driver/controller integrated circuit (IC) and the entire DC-DC converter module that uses this IC. The next version of the controller/driver IC has been sent to fabrication in the fall 2018 and it is expected to provide 18V to 1.5V conversion with >75% efficiency.

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1. Introduction

Large high energy physics experiments, such as the detectors of the Large Hadron Collider (LHC), are currently driving the development of higher radiation hardness, smaller form factor and more efficient powering schemes to handle the increase of power demanded by the upgraded high-density front-end electronics boards. Due to high radiation levels up to hundreds of Mrad(Si) existing at the detector cores, commercial DC-DC converters cannot be used in these powering schemes. Therefore, a critical need exists for custom-designed radiation-hard DC-DC converters. Another requirement for these converters is the ability to function in an environment of high magnetic fields.

Gallium Nitride (GaN) material is one of the most promising wide bandgap (WBG) materials for high efficiency, high frequency, and low to medium range power applications that provides inherent radiation hardness, high switching frequency and large breakdown voltage. GaN devices are a viable contender for implementing the presented converter circuits. In the converter presented in this paper, discrete commercial GaN transistors are used for the power stage, and the controller circuitry and power device driver are integrated on chip with a commercial 0.35 µm CMOS process. Radiation hardening by design (RHBD) techniques have been implemented such that the converter should function at total ionizing dose (TID) levels above 150 Mrad(Si), and neutron fluence levels greater than 2.0×10^{15} n/cm^2, while remaining immune to single event latchup (SEL). The converter will also be designed to cope with high magnetic field constraints, and exhibit low electromagnetic interference (EMI) for operation in close proximity to the noise-sensitive front-end electronic boards.

One benefit provided by the GaN approach is that it enables fast switching, which in turn allows for a small output filter inductor in the converter. This is especially important for the high magnetic field applications that require air-core inductors that consume significant physical area. Smaller inductors are beneficial to the LHC for two reasons: 1) less mass in the path of radiation particles in the detectors close to the core (trackers), and 2) smaller module size to place in the converter in tight space locations. Although the presented converter prototype has been developed to provide optimal performance with switching frequencies of 2-6 MHz and inductor sizes of 300-500nH, the converter has been shown to function up to 20MHz of switching frequency with a 100nH air core inductor.

At TWEPP 2017 we presented the first converter module which consisted of a GaN power stage and commercial off-the-shelf (COTS) driver IC. Three architectures, including single-phase, multi-phase (2 phases) and stacked interleaved architectures, were chosen for the DC-DC buck converters to evaluate performance of the different power stages [1]. The test results showed that with 24 V input voltage, 5.0 V output voltage and 5.0 A output current, the prototype achieves 88.3% peak efficiency at 2 MHz swiching frequency. Moreover, the efficiency was measured as 82.7% at 5 MHz swiching frequency for 24 V input voltage, 5.0 V output voltage and 5.0 A output current.

In this paper, we present the test results of the second version that has a custom designed and radiation hardened driver/controller CMOS IC. Performance tests of the module demonstrate 70% efficiency with 14V-to-1.5V conversion at 4MHz switching frequency, with 6A load current using a 400nH inductor. The efficiency of this first version of the driver/controller IC does not achieve as high efficiency as the the COTS version. This is due to the fact that some of the implemented hardening techniques increase the circuit parasitics to a point that they affect the efficiency. The main objective has been to achieve radiation hardness of 150Mrad(Si). Alphacore

and ASU were able to increase the efficiency >75% and the input voltage to 18V for the next IC version, taped out in September 2018. However, the efficiency measurement is based on simulations on extracted layout netlists and the actual silicon evaluations for the second version of the IC will occur in April 2019.

1.1 Design Specifications

Based on the application requirements, the hybrid GaN and CMOS integrated module DC-DC converter should meet the goal specifications listed in Table 1.

Table 1. Design Specifications of the Proposed RH DC-DC Converter

Parameter	Specifications	Unit
Input voltage	8 - 18	V
Output voltage	1.2 – 5.0	V
Max Load current	5 - 7	A
Overall efficiency	>70	%
Switching Frequency	>2	MHz
Temperature range	-10 to +55	°C
TID tolerance	>150	Mrad(Si)
Neutron fluence	$>2\times10^{15}$	n/cm^2 (1 MeV equiv.)
Single event latchup	>40	MeV-cm^2/mg
Magnetic field	>4	tesla
Physical Dimensions	< 20 × 10 × 3	mm^3

The block diagram of the DC-DC converter is shown in Figure 1. Impressive prior work has been reported for POL converters targeting similar operation environments [2]. This work explores the possibility of using a GaN power stage with higher input voltage and load current as compared to existing solutions. Higher input voltage delivered to the input of a point-of-load (POL) converter core can significantly reduce the power dissipation and ease the cooling requirements in high energy particle detector applications. Higher load current per unit module allows using fewer of them in applications with strict size requirements. The overall efficiency is targeted at >70%. This is a tradeoff considering the overall requirement of an integrated, compact, low-mass, single-module DC-DC converter solution. In the presented work, small form factor for the entire converter, extreme radiation hardness, and the capability to operate under high magnetic fields are more important parameters than maximized efficiency.

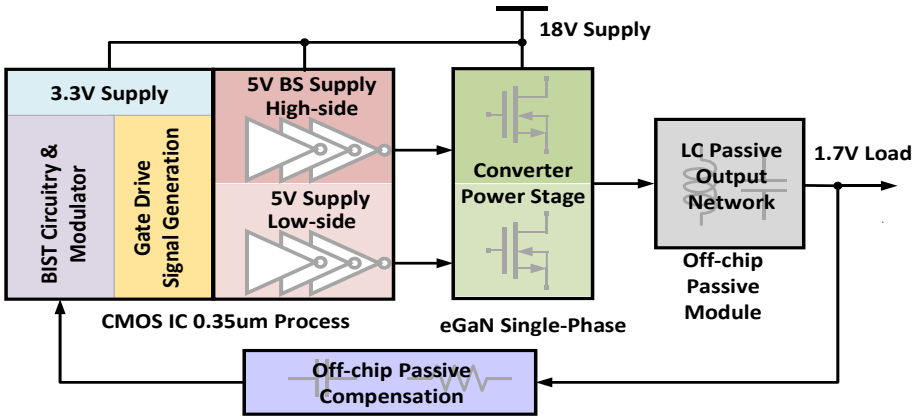

Figure 1. Block diagram of the RHBD DC-DC converter under development

1.2 Custom Rad-Hard Driver and Controller IC Design

The top-level block diagram of the designed single-phase DC-DC buck converter is shown in Figure 2. Two on-chip low voltage dropout regulators are included to provide stable power supplies for the driver and all other integrated control circuits. In this first prototype design, the capacitors and resistors for the Type III compensation are implemented off-chip for adjustment during prototype testing.

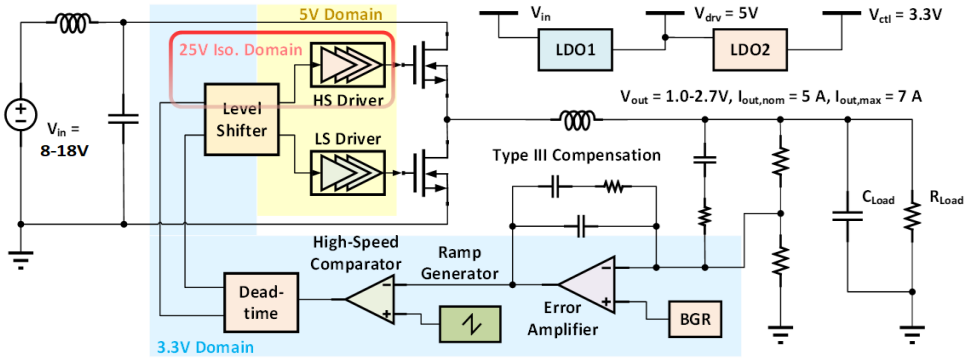

Figure 2. Block diagram of the DC-DC converter with the custom on-chip driver/controller

The selection of the 0.35um CMOS process was based on rigorous process characterization work completed by another group who has been able to achieve good functionality for DC-DC converter designs beyond 100Mrad(Si) in this particular process [3], [4]. We have also had numerous discussions with a member from this particular group [5]. Based on our literature search and these discussions we have selected to avoid the use of PMOS transistors where possible, due to their higher TID-induced threshold voltage shift. In addition, the expected I_{ON} degradation of the P-type LDMOS devices due to extreme neutron fluence has been taken into account in the design margin calculations. The TID induced leakage currents of the 3.3V NMOS transistors can be effectively blocked with the enlosed gate layout (ELT) technique. In the presented custom IC, all NMOS transistors have been implemented with ELT layouts, and P+ guard rings are used for latchup prevention throughout the design.

Figure 3 shows the completed taped out layout. The circuits inside the padframe on the far left are individual sub-circuit test blocks, and the complete driver/controller is located inside the larger padframe on the right. The rightmost figure shows the die micrograph of the controller/driver IC after fabrication.

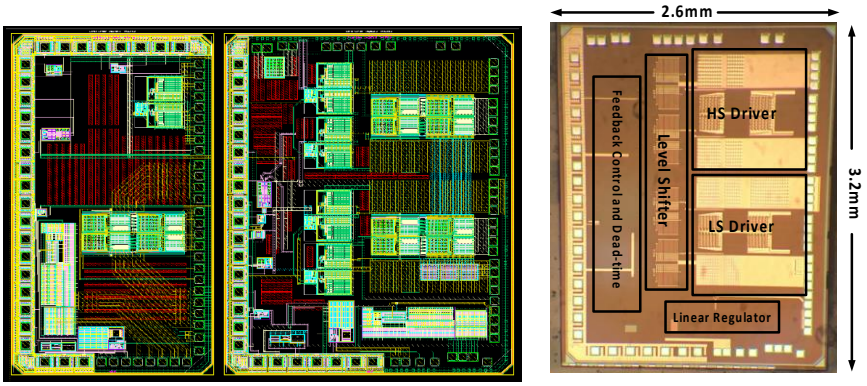

Figure 3. (left) Layouts of the proposed radiation hardened controller/driver and standalone sub-circuit test structure chips. (right) Die micrograph of the controller/driver IC.

1.3 Measurement Results

Figure 4 (a) shows the test board that was designed and fabricated for the purpose of testing the hybrid CMOS and GaN DC-DC converter. The board module consists of the custom-designed controller/driver IC, GaN power stage, and surface-mount discrete passive components (inductors and capacitors). The size of the module has not yet been minimized at this stage, as the final CMOS IC is not yet available. Figure 4 (b) shows measured evaluation results for the hybrid DC-DC converter. The converter provides >70% efficiency up to 14V input voltage when the output voltage is 1.5V and the load current is up to 6A. The value of the inductor used in this configuration is 400nH.

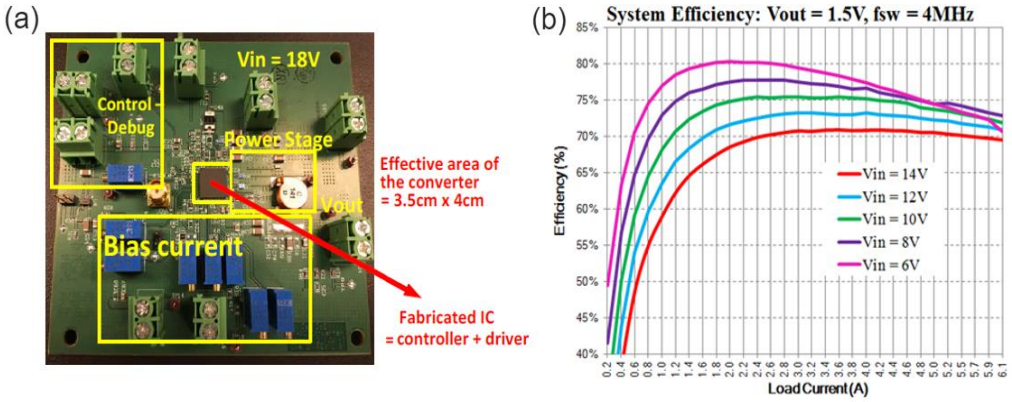

Figure 4: (a) Integrated CMOS IC + GaN power stage test module (size not optimized), (b) Measured results for the test module in (a)

1.4 Summary and Conclusion

A highly integrated, high switching speed CMOS plus GaN hybrid buck converter topology with extreme radiation hardness and small physical form-factor is under development. A fully customized single-chip driver and controller IC enhanced with various RHBD techniques has been fabricated in a 0.35um CMOS process. The IC is integrated into a hybrid GaN-CMOS converter module and measurement results are presented in this work. The module provides over 70% efficiency in a 14V-to-1.5V conversion with 6A load current at 4MHz switching frequency. The second version of the controller chip, optimized to be used up to 18V input voltage with >75% efficiency, has been sent for fabrication in the Fall of 2018 and will be measured for functionality and radiation robustness in the Spring of 2019. The new ASIC is also optimized to be used and in a complete, fully-integrated CMOS-GaN DC-DC converter module product. It includes features such as under-voltage lockout (UVLO), over-current protection (OCP), over-temperature protection (OTP), output voltage protection, and adaptive dead-time control.

References

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[5] Personal communication with F. Faccio.