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High-Voltage Silicon JFET for HV Multiplexing for the ATLAS MicroStrip Staves

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We present a new kind of silicon device: a High-Voltage vertical JFET, originally conceived as a candidate for the High-Voltage Multiplexing switch in the ATLAS upgrade of the silicon microstrip Inner Tracker (ITk). The development of the geometry as well as of the technology process flow was carried out by the help of numerical simulations, which confirmed the feasibility of such a device. Using a planar process flow, both *n*-type and *p*-type HV-JFETs have been successfully fabricated in the silicon processing facility of Brookhaven National Laboratory, starting from epitaxial wafers which have been grown according to strict specifications. Probe station measurements of un-irradiated devices show low leakage current and high breakdown voltage (up to 600V) in the OFF state, and high currents in the ON state. These JFETs, thus, satisfy most of the specs required by the HV Multiplexing switch. However, only irradiation campaigns with protons and neutrons will assess their suitability as rad-hard switches.

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1. Introduction

In the ATLAS ITk upgrade, a few (three or four) silicon microstrip detectors will be biased by a single common High-Voltage (HV) line. Failure of one detector which draws a high current would mean switching off the power supply to all the other good detectors, thus losing a fairly large detector area, unless the faulty detector is disconnected from the bias line. If a switch that excludes the faulty sensor can be placed between each strip sensor and the common HV line, the other good detectors on the same mini-stave can work normally [1]. To work in the radiation-harsh environment foreseen for the ITk, the switch must be radiation hard up to $1.2 \cdot 10^{15} 1MeV - n_{eq}/cm^2$, be insensitive to magnetic field, have a breakdown voltage larger than 600V in the OFF state, while it must exhibit a low R_{DS} in the ON state (especially after irradiation), and preferably be normally ON. These requirements exclude electro-mechanical switches and power MOSFETs, among others. While GaN transistors are the primary choice and have demonstrated excellent performances, at Brookhaven National Lab (BNL) we conceived a new kind of high-voltage silicon JFET, which at least before irradiation is expected to satisfy most of these requirements. In this paper, in Section 2 we briefly describe the structure of the device, while getting an insight of its behaviour by means of TCAD numerical simulations. Section 3 reports the fabrication carried out at BNL and Section 4 describes the static characterization of such devices.

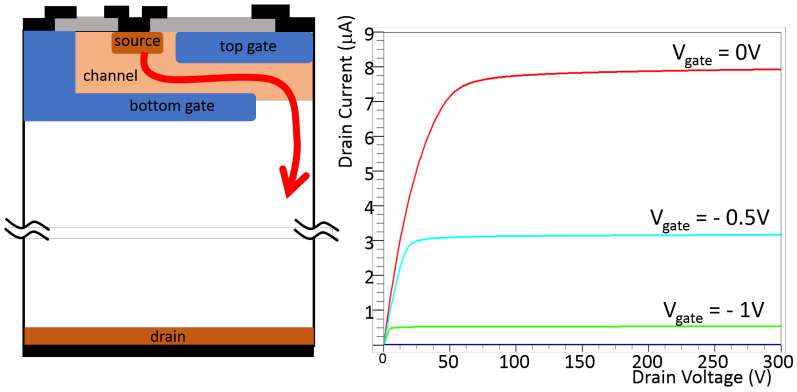

Figure 1: Left: sketch of the proposed vertical structure for the High Voltage silicon JFET; the red arrow shows the source-to-drain current path. Right: simulated output characteristics for the structure on the left (see text for parameters).

2. Structure of the HV Silicon JFET

The proposed structure is sketched in Figure 1. As well as other silicon power devices, it is based on a vertical structure, where the drain is the blank uniform contact on the back of the silicon substrate. On the front side of the device, there are the source, the channel and the top and bottom gates, obtained by ion-implantation. A gap in the bottom gate, below the top gate, allows the source current to flow to the drain. The channel implant runs all over the surface of the device, interrupted just by a deep implant that connects the bottom gate to the surface, for biasing. The channel length, as in a conventional JFET, is given by the overlap of the two gates.

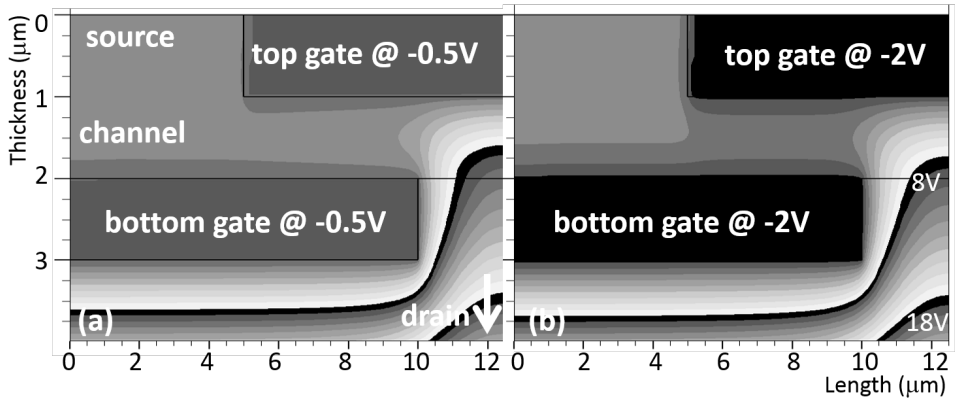

Figure 2: Simulated electrostatic potential of the first 4μm from the top of the $n-$channel JFET, whose output characteristics are plotted in Figure 1. $V_{drain} = 500V$, $V_{source} = 0V$ and $V_{gate} = -0.5V$ in (a) (channel open) or $V_{gate} = -2V$ in (b) (channel closed: pinch-off condition). Contiguous grey bands of different shade are separated by 1V.

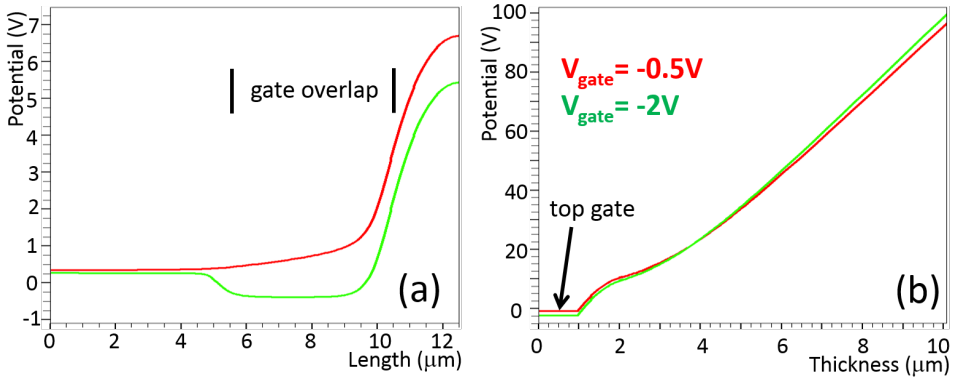

Figure 3: (a) Horizontal cut-line of the electrostatic potential in Figure 2, taken at mid-channel (Y=1.5 μm). (b) Vertical cut-line of the electrostatic potential in Figure 2, taken at mid-gap (X=12.5 μm).

By applying a reverse voltage to the gate/channel junctions, the source-to-drain current can be modulated, resulting in a set of current-voltage curves as shown in Figure 1. The simulated output characteristics refer to a $1-\mu$m wide n-type device, having channel length of 5μm, a channel thickness of 1μm, and a channel doping of $10^{16}cm^{-3}$; top and bottom gate are short-circuited during the simulation (i.e. JFET is biased in triode configuration). We verified that the magnitude of the current is the same as in the case of a conventional JFET that shares the same parameters for the channel. The two parameters which are very different in the two cases are the maximum V_{drain} which can be applied to the structure (in this simulation which does not take into account the guard ring termination external to the bottom gate, the breakdown voltage is 850V) and the V_{drain} at the onset of the saturation, which is much higher than in the case of the standard JFET (on the order of a few volts). This is due to the fact that, as can be appreciated in Figure 2, the voltage applied to the drain hardly penetrate the gap, so that the channel end reaches the necessary voltage to pinch off the channel at higher drain voltages.

In Figure 3, horizontal cut-lines of the electrostatic potential at mid channel and vertical cut-lines at mid gap are plotted, for the HV-JFET with the channel either open (red curve) or closed (green curve). The potential in the channel is very similar to the one in the standard JFET, where a potential barrier exists at pinch-off to prevent the current from the source to flow, while -when the channel is open- no barrier stops the flow. Also in the bulk, the current drifts to the drain without encountering any potential barrier (Figure 3 (b)).

3. Fabrication

The fabrication has been carried out in the Class-100 Clean Room run by the Instrumentation Division at BNL. The silicon wafers were 4", featuring a 50μm thick epitaxial layer with doping concentration of $10^{14} cm^{-3}$. Both *n*-type and *p*-type substrate have been used. The wafers have been grown by Topsil [1], according to our specs. The choice of the substrate parameters was dictated by a trade-off against the conflicting requirements to have drain voltages larger than 600V in the OFF state (which calls for thicker substrates and higher resistivities) and low R_{ds} in the ON state (which calls for thin substrates and lower resistivities).

The fabrication needed five ion-implantations (source, channel, top and bottom gates, and a further deep implant to connect the two gates), and seven lithographies (the five implantations plus contact opening and metallization). We used exclusively a planar process, differing from another approach for a HV silicon vertical JFET, which used a 3D technology [2].

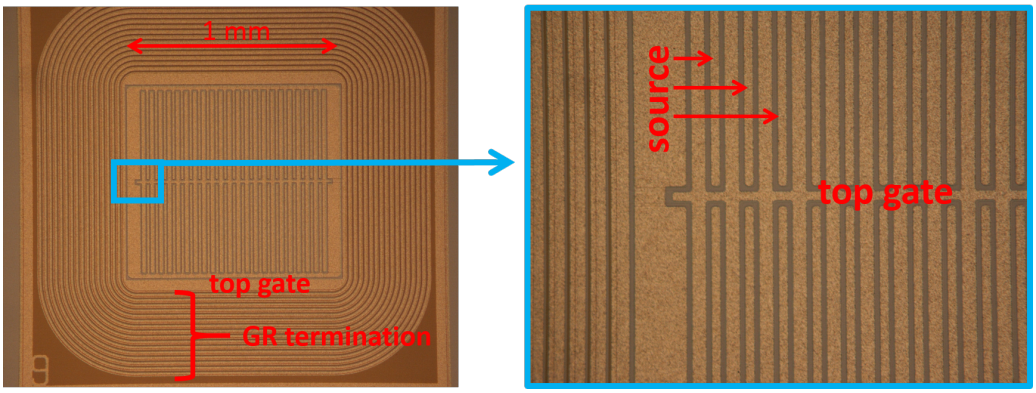

Figure 4: Microscope picture of a HV JFET, detailing the main structures on the front side. The backside (the drain) is a uniform contact.

A microscope picture of a HV JFET is shown in Figure 4. To increase the current in the ON state, very wide source and gates have been designed in an interdigitated configuration. The total source width is about 2*cm*. The top gate is shorted to the bottom gate at the periphery of the device, through a deep implant, so that the JFETs can only be biased in triode configuration.

4. Static Characterization at the Probe Station

Examples of the output characteristics of fabricated devices are reported in Figure 5 (a) for an *n*-channel device and in Figure 5 (b) for a *p*-type device. These devices are completely different

[1] Topsil GlobalWafers A/Si, Siliciumvej 1, DK-3600 Frederikssund, Denmark

from the ones whose simulations are reported in Section 2, and whose only aim was to introduce the HV-JFET concept. V_{drain} is applied trough a Keithley high-voltage source module, while source and gate are connected to a high-precision semiconductor parameter analyzer (HP 4145B), for an accurate current reading. To limit the power dissipation within the device, the full V_{drain} has not been applied for the lower V_{gate}. We verified that the breakdown occurs between drain and gate at about V=600V and V=400V for $n-$ and $p-$ type JFET, respectively. Current-voltage measurements on simple diodes on the same wafers which share the same multi Guard Ring termination of the JFETs show a breakdown voltage in excess of 700V, indicating that the HV JFET breaks down due to an internal structure. The latter can possibly be either the bottom gate edge or the region at the junction top gate/channel at mid-gap, which numerical simulations indicate as the spots with the largest electric fields.

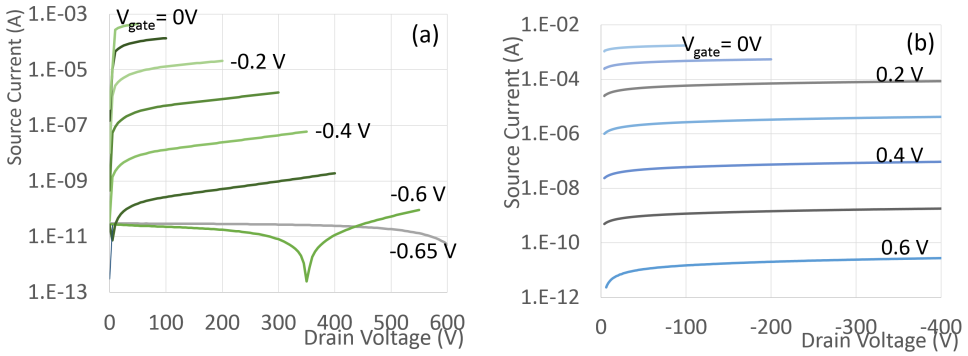

Figure 5: Measured output characteristics (source current vs drain voltage for several gate voltages) of an (a) $n-$type JFET and of a (b) $p-$type JFET, fabricated in the Clean Room of BNL. For higher drain voltages than the ones displayed, there is a breakdown between bottom gate and drain. A dip in the logarithmic source current indicates that the leakage current of the source/gate junction is larger than the (opposite sign) source-drain current.

5. Conclusions

We demonstrated by numerical simulations and by actual fabrications in clean room the feasibility of a HV silicon JFET using only a planar process. Before irradiation, this HV JFET satisfies most of the specs required by the HV-Mux in the ATLAS ITk; however it must be tested against radiation damage to assess whether it could meet the specifications for the HV-Mux.

References

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[2] P. Fernandez-Martinez, M. Ullan, D. Flores, S. Hidalgo, D. Quirion, D. Lynn, *Rad-hard vertical jfet switch for the HV-mux system of the ATLAS upgrade inner tracker*, Journal of Instrumentation 11 (01) (2016) C01043.