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Front-end hybrids for the strip-strip modules of the CMS Outer Tracker Upgrade

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Abstract

The CMS Outer Tracker planned for the HL-LHC Upgrade contains strip-strip and pixel-strip silicon modules. Each of them includes two high-density front-end hybrid circuits, equipped with flip-chip ASICs, passives, connectors and mechanical structures. Several strip-strip hybrid prototypes have been produced using the CBC2 front-end ASIC. Feedback from these developments helped improving the hybrid's testability and the production yield. The availability of the concentrator ASIC's footprint and of the new CBC3 front-end ASIC enables the design of all strip-strip hybrid variants. In this work, the development milestones and the final designs are presented together with chosen solutions.

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1. Introduction

The operation of HL-LHC imposes demanding requirements on the particle detectors. The target integrated luminosity will be raised by a factor of 10 beyond the original LHC design value, reaching 3000 fb^{-1}. A complete replacement of the CMS Outer Tracker is foreseen to adapt to this new environment, with expected fluence of 9.6×10^{14} [n_{eq}/cm^2] in its innermost region [1].

The functional building blocks of the future tracker's structure are based on two types of double-sensor modules: pixel-strip (PS) and strip-strip (2S). The 2S modules will be produced in two versions that vary in the distance between their sensor planes. Each module contains two high-density front-end hybrid circuits. In the 2S module, hybrids host eight binary readout flip-chip ASICs (CBC) and a data concentrator ASIC (CIC), which aggregates and serializes digital information received from CBCs. Additionally, each hybrid is equipped with passive components and mechanical reinforcement structures, which serve as a cooling interface. In total four different 2S front-end hybrid geometries are foreseen in the project. It is planned to use 15,360 hybrids of this type inside of the CMS tracking volume [1].

A reduced-size hybrid, called 2CBC3, has been produced to qualify the new front-end ASIC and its testing features. It was received and tested in 2017, delivering feedback on the lateral communication feature of the front-end chip. Lateral communication is a mechanism of exchanging information about the particle's hit position between the neighbouring ASICs, crucial for the complete discrimination of the high transverse momentum particles. The 2CBC3 also served as a validation platform for the implemented routing methodology and test structures thus giving a green light for a full-size object called 8CBC3 (still without the CIC). This new full-size hybrid shall be available for qualification in Q4 of 2018 and is intended to host the final CBC3.1 for its evaluation. In meantime, a design of the data concentrator has matured enough to derive its first footprint and pin assignments. Consequently, a full routing exercise of the 2S front-end hybrid became possible. The designed hybrid matches the geometry driven by recent models of the 2S modules and is a result of a long development path of prototype hybrids.

This work reports on the design constraints and chosen solutions for the 2S front-end hybrids. The 2CBC3 prototype is presented with its test results, followed by a design expansion towards the 8CBC3. Ultimately, the integration of the CIC into the final 2S hybrid is discussed.

2. Physical and mechanical constraints for 2S hybrids, chosen solutions

The production of the 2S front-end circuits relies on the use of flex technology. It enables the circuit's folding over a very lightweight structure of carbon fibre (CF) composites. That is to comply with the low mass requirement and to adjust the hybrid's thickness to different separations between sensors, without the need of changing the PCB's stack-up. The conceptual design of the 2S module and the interconnection between sensors and the hybrid are shown in Figure 1.

To match the 1.8 mm sensors' separation in the thinnest module, the 2S flex must allow for bending with a radius of 0.9 mm without developing any circuit defects. A constraint for the circuit's thickness has been set below 200 μm. This brought limitations to the number of conductor layers present in the stack-up shown in Figure 2. Another consequence was a limited choice of dielectric materials and their thicknesses. The solder mask material turned out to be especially problematic, causing a development of failure modes in the fold region of the past assemblies. A solution to that problem was the selection of NPR-80 [2], which is a photo-image, alkaline developed type solder mask suitable for flex application and allowing for sharp folds required by the project.

The 2S front-end circuit carries nearly 6,500 signal interconnections, out of which more than 2,000 are analogue. On top of that there are 9 ASICs present on the circuit and over 50 passives. All that must fit inside a 125 mm by 27.95 mm envelope leading to a very High Density Interconnect (HDI) design, with traces and separation distances as thin as 42.5 µm in the fan-out region of the ASICs. The digital signals are driven differentially through an edge coupled coated microstrip with the 50 µm lines width and the 60 µm separation between them. Digital signal distortion caused by the transmission line has been measured over full hybrid's distance (125 mm) with a signal rate beyond the design value (320 Mbps) and the designated SLVS driver. Very clear eye diagrams were obtained suggesting a very good impedance match over the line (Figure 2).

To reduce the footprint area, all the ASICs are mounted with a flip-chip technology resulting in more than 6,700 on-board bump connections. The pitch of the raster of neighbouring analogue pins is 250 µm in both X and Y directions, leading to a very challenging routing exercise. To enable routability in such a dense region, with a 4-layer stack-up limitation, it was necessary to use a micro via-in-pad together with the blind and buried via technology. The feature size of vias used in the hybrid's designs is 110 µm pad and a maximum drill of 50 µm. These values are at the manufacturing limit for the flex contractors qualified for the project. The production and assembly of the hybrids is very demanding. Several reliability issues have been identified along the prototyping phase and have been addressed. Those problems are discussed in detail in [3].

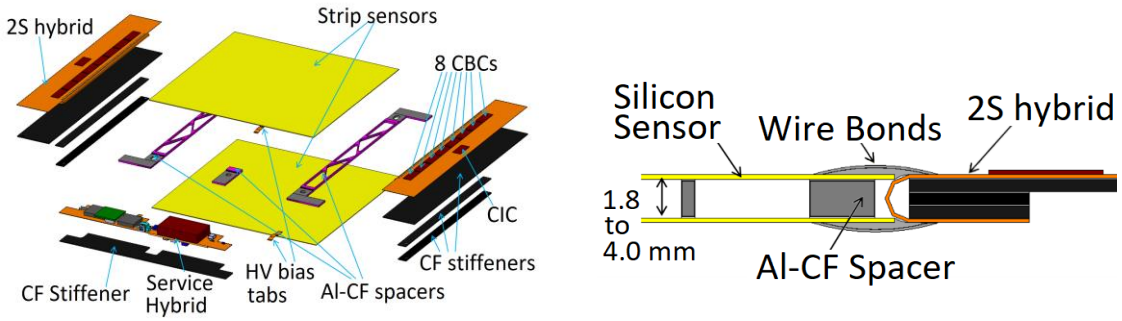

Figure 1: An exploaded view of the 2S module concept (left), and a cross-section view of the interconnection between a folded front-end hybrid and both sensors (right).

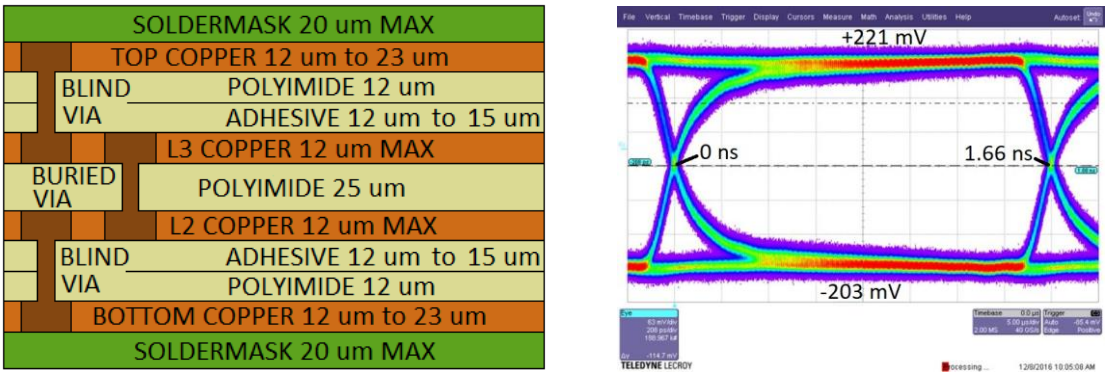

Figure 2: Flex stack-up of 2S hybrid prototype developments (left). An eye diagram measured on a tesboard with target geometry differential line and 600 Mbps PRBS signal driven from target SLVS driver (right).

3. Prototype front-end hybrids with 2 CBC3 ASICs

The third generation of the CBC front-end ASIC implements the full functionality expected from the 2S front-end ASIC: data rates of 320 Mbps, hit correlation logic with adjustable window

search of high transverse momentum particles trajectories (called "stubs") and a chip to chip communication for the detection of particles crossing edge channels of two ASICs. A new hybrid circuit was designed to test the chip's functionality and its new features.

The flex circuit hosts just 2 CBC3 ASICs and implements the target 2S hybrids' 4-layer stack-up with the total thickness of approximately 150 µm. The build-up of the hybrid was simplified by using two FR4 stiffeners instead of 3 carbon fibre pieces. The hybrid was the first of its family running with a clock at 320 MHz. A few test features were hosted on board: an access to the analogue multiplexers of the CBCs, probing points for 40 MHz clock, temperature monitoring and a high voltage filter for the sensor biasing.

25 hybrids were produced and successfully qualified. Two minor undesired features were discovered in the ASIC and will be corrected in its 3.1 version: incorrect net assignment of some lateral communication ports in the ASIC and high power consumption with the default settings at the start-up. Few hybrids were equipped with silicon sensors and tested in the beam test facility at Fermilab, shown in Figure 3. The test campaign demonstrated that the stub finding efficiency is very high (>99%) and that the transverse momentum cut-off is as expected for the sensor type.

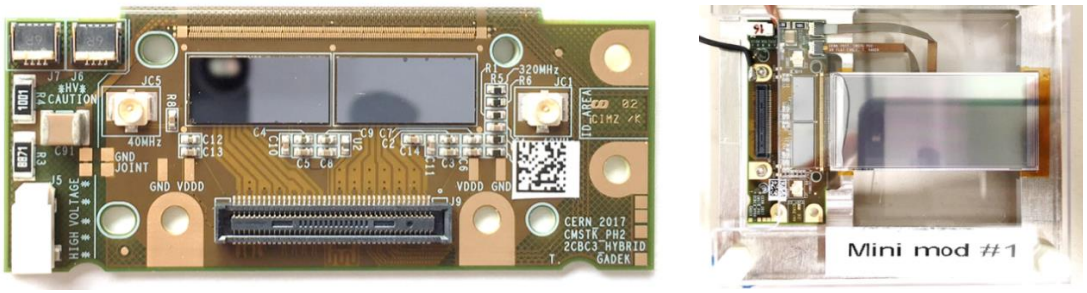

Figure 3: A picture of a produced hybrid with 2 CBC3 ASICs (left), and a picture of a mini module built with that hybrid (right).

4. Design of a prototype front-end hybrid with 8 CBC3 / CBC3.1 ASICs

After a successful production of 2 CBC3 hybrid, a larger object is needed, which enables production of a full-size prototype 2S module. This new 8-ASIC circuit will host either CBC3 or CBC3.1 chips that are footprint and pinout compatible. First batch of the hybrids should arrive in Q4 2018. The flex still misses the concentrator ASIC. The functionality of CIC will be substituted by a back-end FPGA interconnected via two 100-pin fine pitch connectors visible at the bottom of the hybrid's design. Additionally, a mezzanine board hosting a wire-bonded version of the CIC prototype has been designed and is shown in Figure 4. The board is meant to be plugged directly onto the hybrid's connectors and has been designed in the flex-rigid technology.

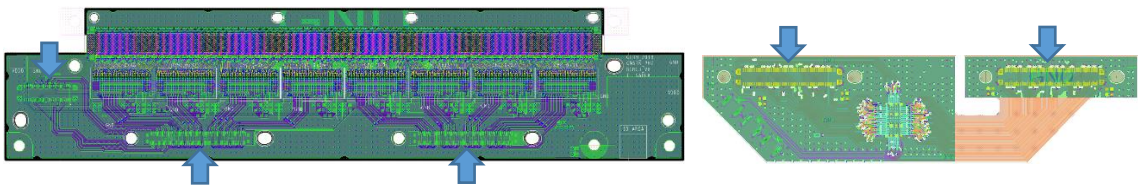

Figure 4: Layout of a hybrid with 8 CBC3/CBC3.1 ASICs (left), and a layout of a CIC mezzanine flex-rigid board (right). Blue arrows point at the footprints of the fine pitch connectors.

5. Design of a complete 2S type front-end hybrid

Availability of the CIC bump map and its preliminary pin assignment enabled a complete 2S front-end hybrid design, see Figure 5. The hybrid fulfills all the dimensional and mechanical

requirements up to date. It is compatible with the latest Service Hybrid design and its connector's pin assignment. It was fully routed following the manufacturing constraints and implementing all necessary testing features described in [4]. The design was studied in terms of the voltage drop budget across the power and return plane, which are well balanced as shown in Figure 5.

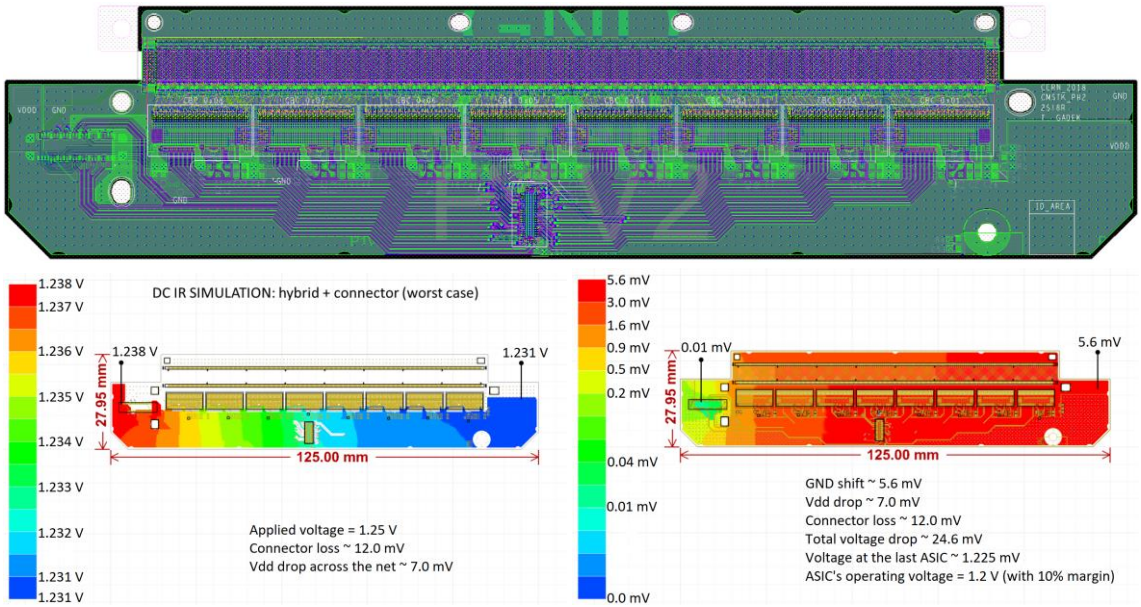

Figure 5: Layout of the 2S front-end hybrid (top). A simulation of the voltage drop across the power plane of the design (bottom left), and a simulation of the voltage shift across the ground plane (bottom right).

6. Conclusion

The CMS Outer Tracker planned for the HL-LHC Upgrade contains 7680 strip-strip silicon modules. Each of them includes two high-density front-end hybrid circuits, equipped with flip-chip ASICs, passives, connectors and mechanical structures. The hybrid's design choices were made for the flex technology and its stack-up. The materials have been selected based on the prototyping experience. Two strip-strip hybrid prototypes have been designed using the CBC3 front-end ASIC one of which was already produced and tested. Feedback from these developments guides the designs of final 2S hybrids as well as helps improving the front-end ASIC, its pinout and communication interfaces. The availability of the concentrator ASIC's footprint and of the new CBC3.1 front-end ASIC enabled the first complete design of the 2S front-end hybrid. The design in the current shape is ready for the pre-production phase of the project.

References

[1] CMS collaboration, *Technical Proposal for the Phase-II Upgrade of the CMS Detector*, CERN-LHCC-2015-010

[2] Nippon Polytech Corp., *NPR-80 Series,* http://www.nptcorp.com/en/product/npr80/index.html

[3] M. Kovacs et al., *Reliability test results of the interconnect structures of the front-end hybrids for the CMS Phase-2 Tracker Upgrade*, in these proceedings.

[4] T. Gadek et al., *Testing of the Front-End Hybrid Circuits for the CMS Tracker Upgrade*, 2017 JINST 12 C01010