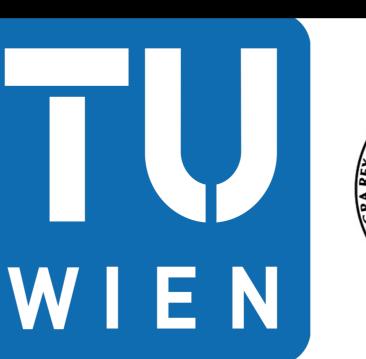
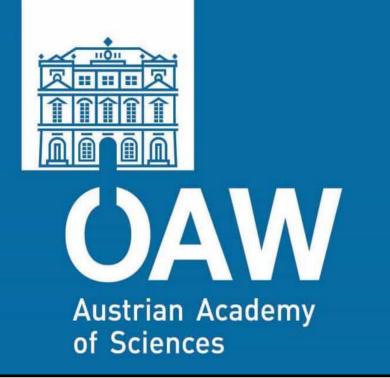


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Update on the TowerJazz CMOS DMAPS development for the ATLAS ITK

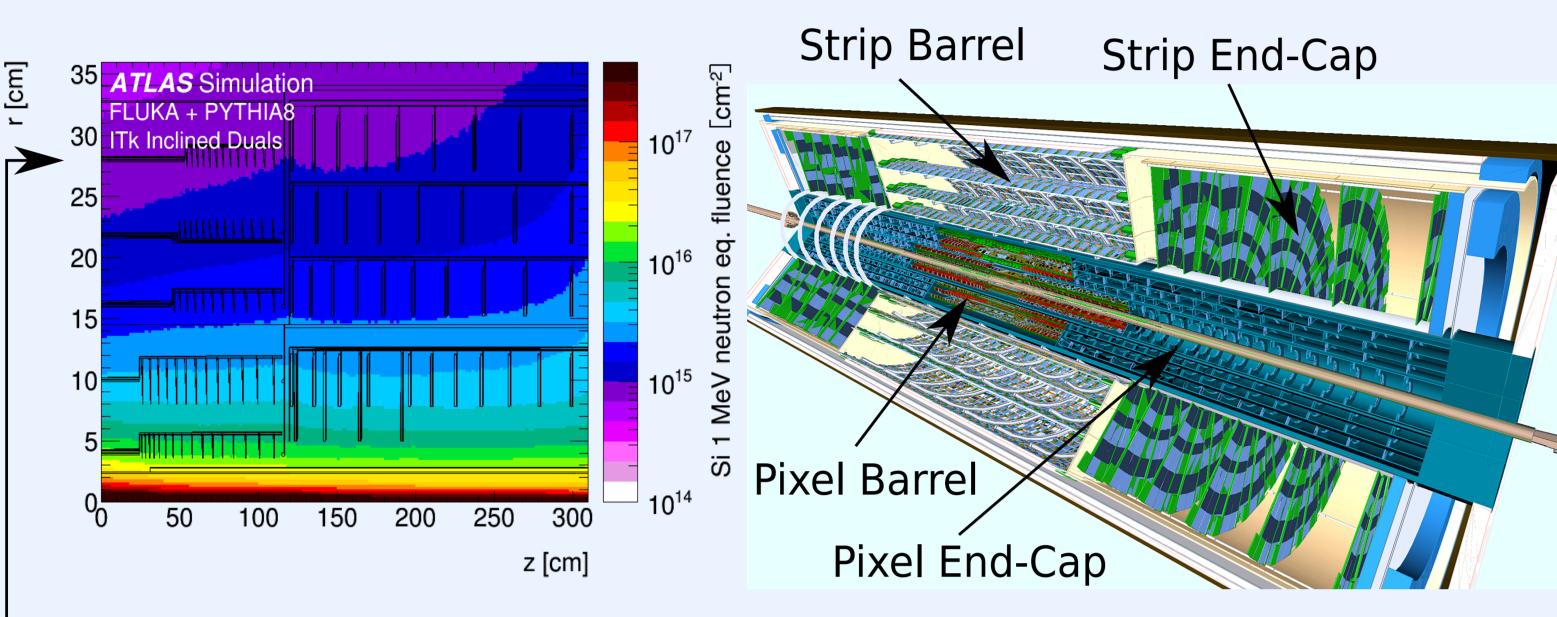
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Glossary:

CMOS: Complementary Metal Oxide Semiconductor **DMAPS**: Depleted Monolithic Active Pixel Sensor ITk: Inner Tracker (of the ATLAS experiment)

ATLAS ITk Pixel Detector



-5th layer of pixel tracker:

Challenges:

Occupancy: 1MHz/mm²

Expected NIEL: 10¹⁵ N_{eq}/cm²

TID: 50 Mrad

ITk Strip Tech. Design Report,

Active area of 5th layer: 3 m²

Upgrades and Changes:

 \supset η coverage increased to 4.0

All silicon designs to cope

with occupancy and pile up in HL-LHC

Radiation Resistant CMOS Sensors

IP-Substrate (>1kΩ cm)

P-Substrate (>1k Ω cm)

Kolanoski, Wermes 2015

Kolanoski, Wermes 2015

Two variants:

CMOS circuitry inside collection diode

CMOS circuitry in separate deep p-well

Advantages:

Complex electronics in active area of pixel matrix

Very thin at around 100µm Cheaper by a factor~3 (no front end

no bump bonding) Production in large quantities much

easier (layer 5 of ITk is largest!)

Signal Generation:

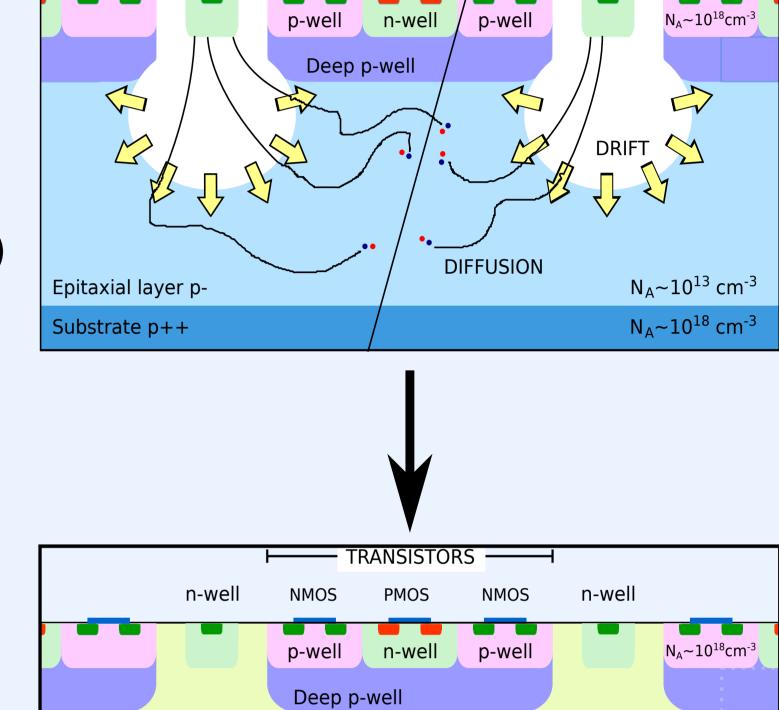
Voltage on collection diode drops when charge from an incident particle is collected and is "slowly" recovered via diode reset

Initial diode signal is amplified by the in-pixel circuitry and then read out

TJ180nm CMOS Process Modification

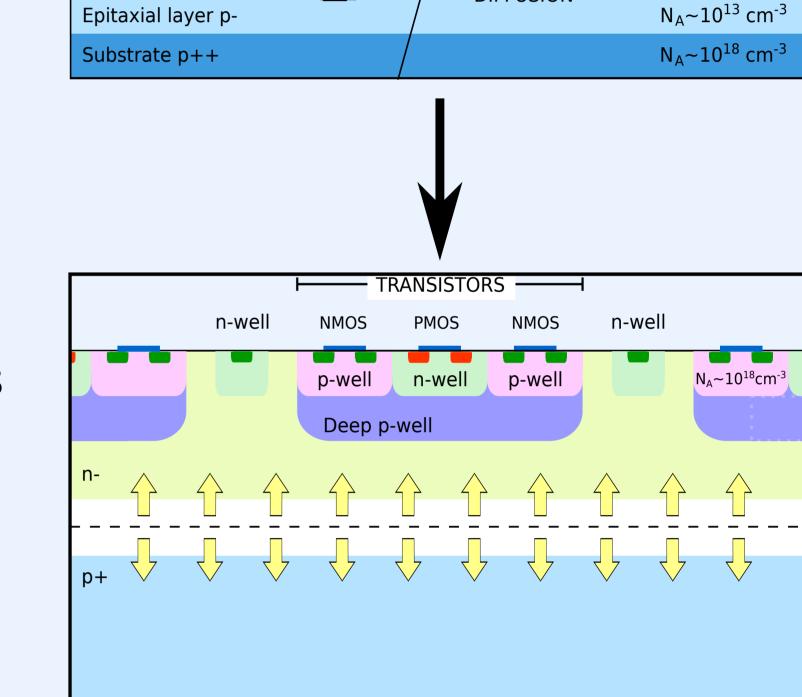
Standard Process:

- Depletion only around collection diode
- Charge collection partially via diffusion (far from electrode) and via drift (close to electrode)



Modified Process:

- Interstitial n-implant ensures homogeneous depletion across whole bulk
- Charge collection **only via** drift thus faster and more radiation tolerant

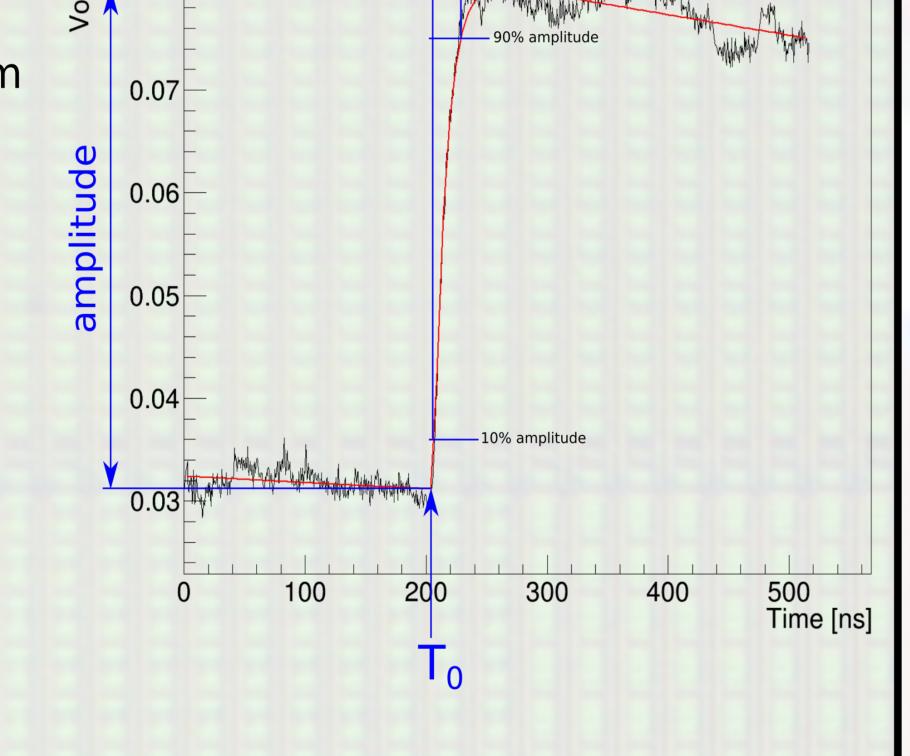


CERN-LHCC-2017-005. ATLAS-TDR-025

Towerlazz Investigator

Features:

- > 134 "mini-matrices" with a great variety of pixel designs
 - } pixel pitches range from 20μm to 50μm
 - > variable deep p-well coverage
 - > variable shape of collection diode analogue output of signal waveform for detailed analysis
 - 3T (3 transistor) readout
 - dedicated reset
 - single pixel readout



30µm

rise time

Minimatrix 106:

Mini-matrix 106 was measured extensively

- 30μm x 30μm pixel pitch
- 3µm collection diode
- } large deep p-well extends close to collection diode
- is close to the design of the pixels for the first full sized digital chip "MALTA"

collection diode

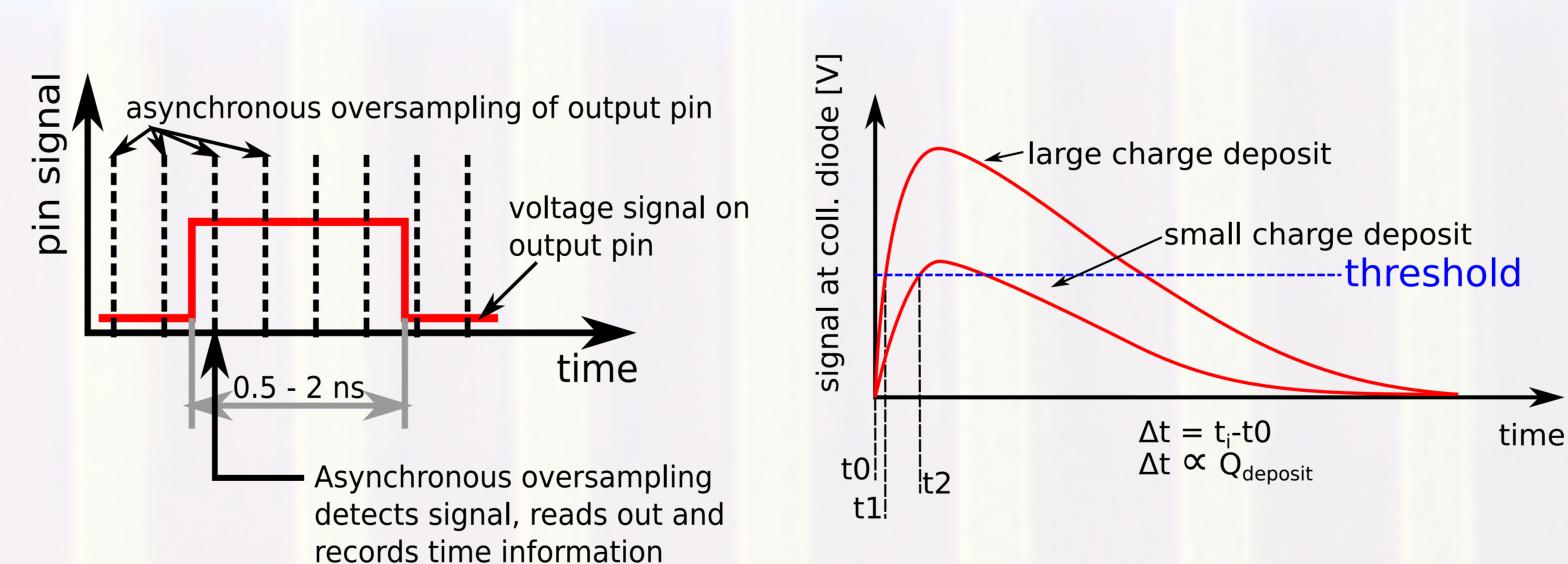
Results:

- > software threshold of 110e
- high efficiency maintained after irradiation of 10¹⁵ N_{eq}/cm²
- efficency is maintained at pixel borders and edges (see center of efficiency plot)
- | cluster size cleary indicates charge sharing even further away from pixel borders

Efficiency **Cluster Size** Center Efficiency 0.934 ± 0.019 20 30 x Pos [um] x Pos [um] Drop of efficiency caused by readout issue with 4th pixel limited telescope resolution

General Information:

- | full sized digital chip
- ≥ 25µm epil layer, fully depleted
- \supset 512 x 512 pixels with a 36.4 x 36.4 μ m² pitch
- > 8 sectors of 64 columns with different pixel flavours
- > fully asynchronous operation
 - readout via asynchronous oversampling



Special Features:

> very small collection diode with low capacitance of <5pF

low capacitance greatly reduces noise

low noise allows for operation at very low thresholds

⇒ ENC of only ~15-20e possible!

|> low thresholds are needed for thin epi layers of 25µm thickness which can be fully depleted

| full depletion of epi layer means charge is only collected via drift

chip is faster and more tolerant to radiation damages > charge deposition is inferred from time walk of signal

> 500nA/pixel or <70mW/cm²

