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LEVEL-1 DATA DRIVER CARD - A high bandwidth radiation tolerant aggregator board for detectors

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The Level-1 Data Driver Card (L1DDC) was designed for the needs of the future upgrades of the innermost stations of the ATLAS end-cap muon spectrometer. The detectors located at the muon Small Wheels will be replaced by a set of precision tracking and trigger detectors, the resistive Micromegas (MM) and the small-strip Thin Gap Chambers (sTGC). After the upgrade, the number of interactions per bunch-crossing will be increased up to 140, resulting in a dramatically large amount of produced data. The high number of electronic channels (about two million for the MM and about 300 k for the sTGC) along with a harsh environment (radiation dose up to 1700 Gy (inner radius) and a magnetic field up to 0.4 T in the end cap region) led to the development of new radiation tolerant electronics and a scalable readout scheme able to handle the new data rates. In addition, correction mechanisms for Single Event Upsets (SEU) and communication errors must be implemented to assure the integrity of the transmitted data. The L1DDC is a high speed aggregator board capable of communicating with multiple front-end (FE) electronic boards. It collects detector along with monitoring data and transmits them to a back-end system through bidirectional and/or unidirectional fibre links at 4.8 Gbps each. In addition, the L1DDC distributes synchronous clocks, trigger and configuration data coming from the back-end system to the FE boards. The L1DDC is completely transparent to the data being transmitted or received and can be used in any readout system. Three different types of L1DDC boards will be fabricated handling up to 9.6 Gbps of user data and consist of the same custom made radiation tolerant ASICs. In this paper the L1DDC boards will be described and the results from radiation tests will be presented.

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1. Introduction

The L1DDC is part of the Data AcQuisition (DAQ) for both MM and sTGC detectors. It is an intermediate board that aggregates and transmits data from up to eight FE boards to the back-end electronics which consist of commercial electronics with Field Programmable Gate Arrays (FPGA). In general, the L1DDC combines three distinct paths: Timing and Trigger, Data Acquisition and Slow Control information, into one or more bidirectional optical links at a rate of 4.8 Gbps each. This is achieved using custom Application Specific Integrated Circuit (ASIC) chipset designed at CERN. This chipset includes a high speed serializer/deserializer GigaBit Transceiver (GBTX) [1], a Slow Control Adapter (SCA) [2], a GigaBit TransImpedance amplifier (GBTIA) [3] and a GigaBit Laser Driver (GBLD) [4]. The GBTIA and the GBLD form the Versatile optical Transceiver (VTRX) and two GBLDs the Versatile Twin Transmitter (VTTX) module. Moreover the CERN custom FEAST [5] DC-DC converter will be also used for the power distribution.

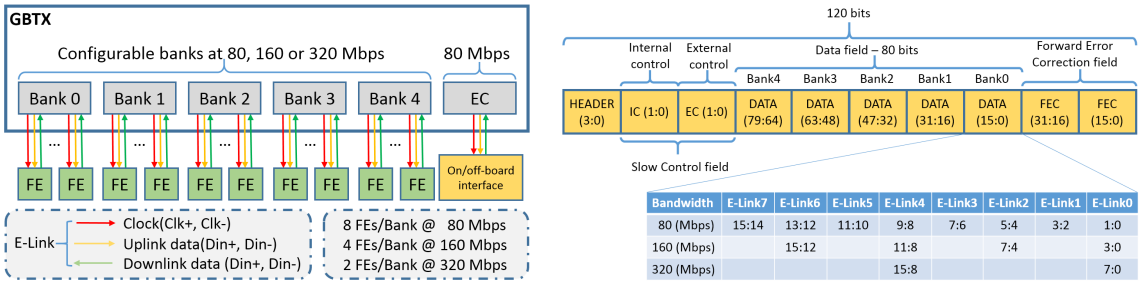
2. Connectivity and Functionality

For the interconnection of the on-detector electronics the 36 position mini Serial Attached Small Computer System Interface (miniSAS) connectors and cables are used. Signal transmission is implemented by using differential serial lines (up to nine) with a bandwidth of 80, 160 or 320 Mbps using the Scalable Low-Voltage Signaling (SLVS) for 400 mV (SLVS-400) [6]. The SLVS is a differential standard with a swing of 0.2 V, centered on 0.2 V. On the other hand, for the interconnection of the L1DDC with the off-detector electronics, multi-mode duplex LC-LC fibres will be used. Due to the different characteristics, requirements and space limitations of both MM and sTGC detector technologies different L1DDC boards will be fabricated: the MM-L1DDC, the sTGC-L1DDC and the RIM-L1DDC. All L1DDC boards utilize the same ASICs but different configuration is implemented according to the data rate of each detector.

2.1 ASIC description

The GBTX is a radiation tolerant ASIC fabricated using the IBM/GlobalFoundries 130 nm CMOS technology. Its power supply is 1.5 V and its power consumption is 2.2 W in full operation able to be reduced to $\sim$ 1 W when it is configured as a transmitter. The GBTX is capable of multiplexing a number of serial links (E-Links) to a single fibre. One E-Link, consists of three differential pairs being the clock (Clk+ and Clk-), the uplink data (Din+ and Din-) and the downlink data (Dout+ and Dout-). The GBTX can support up to 40 E-Links divided into five groups called banks. Each bank can support up to eight E-Links at 80 Mbps, four E-Links at 160 Mbps or two E-Links at 320 Mbps. The GBTX has an extra E-Link with a fixed rate at 80 Mbps for slow control information, as shown on the left of figure 1. The transmitting data use the Double Data Rate (DDR) signaling and have the same relative phase with the clock. For the return links, a dedicated phase-aligner is used to phase align the incoming data with the clock for each E-Link.

On the fiber side the GBTX transmits and receives frames of 120 bits in the interval of 25 ns, resulting in a line rate of 4.8 Gbps. In that frame four bits are used for the frame header (H), 32 for Forward Error Correction (FEC) and the 84 bits are the user data. From the 84 bits, four are dedicated for Slow Control (SC) information (two for Internal Control (IC) and two for External



Bandwidth	E-Link7	E-Link6	E-Link5	E-Link4	E-Link3	E-Link2	E-Link1	E-Link0
80 (Mbps)	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
160 (Mbps)		15:12		11:8		7:4		3:0
320 (Mbps)				15:8				7:0

Figure 1: Left: The E-Link configuration. The GBTX has five banks with up to eight E-Links per bank. Each bank can be independently configured at 80, 160 or 320 Mbps. Right: The GBTX frame format and frame to E-Link bit mapping.

Control (EC) fields). If a bank is configured at 80 Mbps then two bits of the frame are mapped to each E-link, four if it configured at 160 Mbps and eight if it is configured at 320 Mbps. The frame format and the frame to E-Link bit mapping are outlined on the right of figure 1. Initial configuration information is taken from the on chip e-Fuses that can then be modified later via the optical link itself (IC) or via an I^2C slave interface. In the transmitter part the data are SCRambled (SCR), to obtain DC balance, and then encoded with a FEC code before being serialized and sent to the optical transceiver. The FEC algorithm is built by interleaving two Reed-Solomon RS(15,11) encoded words with 4-bit symbols, each capable of correcting a double symbol error. This means that a sequence of up to 16 consecutive corrupted bits can be corrected. Finally, all configuration registers inside the GBTX are fully protected against SEUs with triple redundant registers [1].

The GBTIA and GBLD ASICs have a maximum bit rate of 5 Gbps and the power supply voltage is 2.5 V. The SCA is used to distribute control and monitoring signals to the on-detector FE electronics and perform monitoring operations of detector environmental parameters. The dedicated EC E-Link of the GBTX (80 Mbps) is used for the communication with the on-board SCA. The SCA integrates I^2C masters, General Purpose IOs (GPIOs) and 12 bit Analogue to Digital Converters (ADCs). The I^2C buses are used for the configuration of the GBTXs, the GPIOs to provide control signals and the ADCs for temperature and voltage monitoring. For the power distribution scheme the FEAST DC-DC converter is used. This is also an ASIC fabricated at CERN and has an input voltage range from 5 V to 12 V, 4 A load capacity and achieves 76 % efficiency.

2.2 L1DDC board description

The MM-L1DDC interfaces with eight FE and one trigger board. To increase the maximum bandwidth three GBTX ASICs were used. With this scheme a maximum of 1.28 Gbps readout rate (out of the total 9.44 Gbps) can be achieved per connector. To minimize the amount of fibres the two GBTXs are configured as transmitters using a VTTX. With this scheme the two extra GBTXs could not be configured via the optical link and an SCA was added on the board. Configuration data are sent to the SCA through the GBTX which is connected to the VTRX, and then the SCA can configure the two additional GBTXs through the I^2C master. All ASICs were placed to the bottom side of the board and this side will be attached to a copper plate of the cooling channel. The size of the L1DDC board for the MM detectors is 200 mm in length, 60 mm in width and 12 mm in

height as shown on the top left side of figure 2. For the power distribution two FEAST ASICs were used (one for 1.5 V and one for 2.5 V). The overall power consumption of the MM-L1DDC is 7 W.

For the sTGC detectors the sTGC-L1DDC interfaces with three FE boards. To support the high rates of the inner FE boards (close to the interaction point) the sTGC-L1DDC has two GBTXs and an additional miniSAS connector (total four) to provide sufficient differential pairs. For the E-link side the total downlink bandwidth is 1.2 Gbps and the total uplink bandwidth is 5.36 Gbps. Two VTRXs provide the configuration data to the GBTXs through the IC channel and then the GBTXs can configure the VTRXs through the I^2C master.The size of the L1DDC for the sTGC detectors will be 125 mm in length, 60 mm in width and 12 mm in height as shown on the bottom left side of figure 2. Two FEAST ASICs (one for 1.5 V and one for 2.5 V) provide sufficient power for the board. The overall power consumption of the sTGC-L1DDC is 6 W.

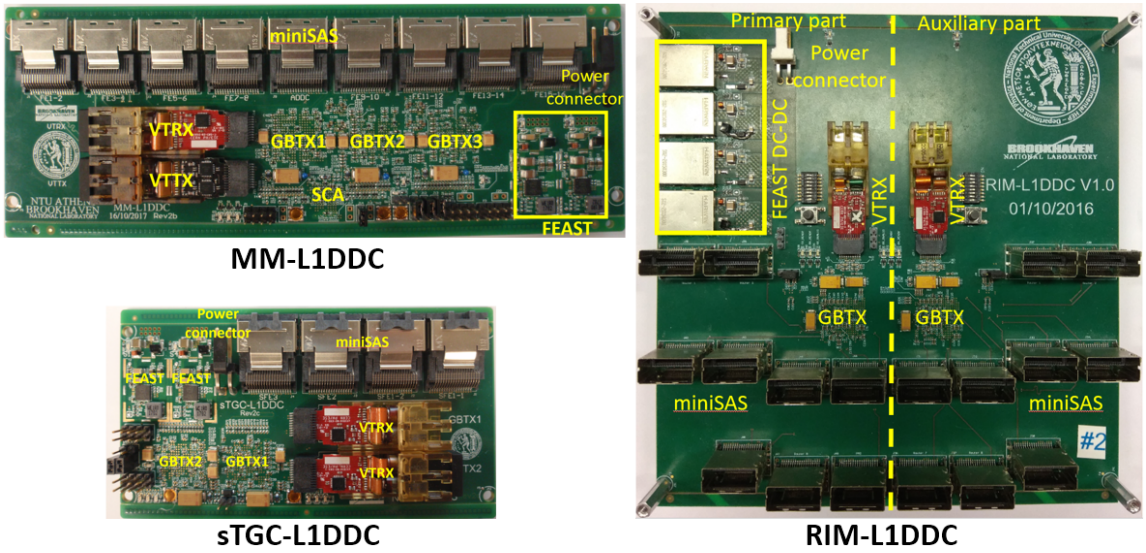


Figure 2: The MM-L1DDC, the sTGC-L1DDC and the RIM-L1DDC board. The miniSAS connectors, the power connector, the FEAST DC-DC converters, the VTRX and the VTTX are visible. The GBTXs, the SCA and the fanout buffers are placed on the bottom layer of the board.

A third L1DDC board, called RIM-L1DDC, will be used to provide synchronous along with high quality clocks, configuration and any additional data to the on-detector trigger boards of the sTGC detectors. It is basically two independent boards, one primary and one auxiliary, sharing the same PCB including one GBTXs, one VTRX and nine miniSAS connectors per side. This gives the ability to alter dynamically between the two sides providing fully redundancy in case of failure. In this case, two miniSAS connectors, one primary and one auxiliary are used for interfacing with each of the sTGC trigger boards. Various tests showed that GBTX output clocks may not be ideal for the high demanding Xilinx FPGA transceivers of the sTGC trigger boards. For this reason dedicated fibres will be used and two extra VTRXs will be added on the next prototype to provide the low jitter clocks. Fan-out chips will be used for the selection between the GBTX E-Link clock with a jitter of about 3.8 ps and the dedicated clock estimated to be close to 1 ps. The size of the RIM-L1DDC will be 170 mm in length, 170 mm in width and 15 mm in height. The first prototype of the board is shown on the right side of figure 2. The overall power consumption of the final

RIM-L1DDC is estimated to be 7.5 W.

3. Radiation tests

Neutron irradiation tests on the GBTX were performed in May 2017 at the 5.5 MV HV TN-11 TANDEM Van Der Graaff accelerator of NCSR "Demokritos" in Athens, Greece. For the purposes of these tests, mono-energetic neutrons were produced via the ^{3}H$(d,n)^4$He reaction where a deuteron beam of 4-5.9 MeV impinged on a thin solid tritiated titanium target deposited on a copper backing. The ^{3}H$(d,n)^4$He reaction using this setup under the aforementioned experimental conditions yielded neutrons of 19-24 MeV. For the purposes of these tests, the RIM-L1DDC was placed at a distance of 14.8 cm up to 30.2 cm from the tritiated target. The RIM-L1DDC was irradiated for a total of five days with various hours and fluence per day with a total dose of 2.71E+09 and total time of about 48 hours.

Prefixed data from an evaluation board, running a GBTX emulator firmware, were send to the RIM-L1DDC and with external loop-backs (using 0.5 m long twinax cables over 320 Mbps E-Links) back to the evaluation board comparing the received and transmitted data. The evaluation board was placed outside the beam area and was connected with the RIM-L1DDC via a 50 m long fibre. About 6 TB of user data were transmitted during the test period without any errors. The SEU correction and the FEC registers of the GBTX were also monitored and no errors were observed.

4. Conclusion

The L1DDC is a radiation tolerant board that interfaces with the off-detector electronics. It is capable to aggregate multiple serial links with various speeds (80, 160 or 320 Mbps) into a single or multiple fibres at 4.8 Gbps each and can provide synchronous clocks to the FE boards. The L1DDC is transparent to the data being received or transmitted and is equipped with SEU mechanisms to ensure the signal integrity. Moreover RIM-L1DDC can distribute low jitter clocks to drive the FPGA transceivers and it is implemented in a fully redundant way. Three prototypes with different size and configuration provide flexibility for both MM and sTGC detectors. Various prototypes and tests confirm that L1DDC boards can operate reliably and full-fill all detector requirements.

References

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