

VMM3, an ASIC for Micropattern Detectors

George Iakovidis^{*†}

Brookhaven National Laboratory

E-mail: george.iakovidis@cern.ch

The VMM is a custom Application Specific Integrated Circuit (ASIC). It will be used in the front-end readout electronics of both the Micromegas and sTGC detectors of the New Small Wheel upgrade [1] of the ATLAS experiment at CERN. It is being developed at Brookhaven National Laboratory and fabricated in the 130nm Global Foundries 8RF-DM process (former IBM 8RF-DM). The 64 channels ASIC has highly configurable parameters and is able to handle signals of opposite polarities and a high range of capacitances while being low noise and low on power consumption. The VMM has four independent data output paths. First is the “precision” (10-bit) amplitude and (effective) 20-bit time stamp read out continuously (250ns dead-time per channel) or at when a trigger occurs. Second, a serial output called Address in Real Time (ART). This is the address of the channel which had a signal above threshold within the bunch crossing clock. Third, the parallel prompt outputs from all 64 channels in a variety of selectable formats (including a 6-bit ADC). Finally a multiplexed analogue amplitude and timing outputs in which the ASIC provides analogue outputs to be digitised externally. The ASIC has undergone 3 versions. Version 3, was submitted in 2016 in a dedicated run and has all the design features including the deep readout buffer logic and SEU mitigation circuitry for the configuration registers, the state machines, and the FIFO pointers. The device is packaged in a Ball Grid Array with outline dimensions of $21 \times 21 \text{ mm}^2$ and is being tested for the last years. Since few bugs already found, a version called VMM3a was submitted in October 2017 addressing them. The VMM3 was tested with Micromegas prototype detectors and performance is reported.

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^{*}Speaker.

[†]on behalf of the ATLAS Muon Collaboration

1. Description of the VMM3

The VMM is composed of 64 linear front-end channels. A block diagram of one of the identical channels is shown in Figure 1. Each channel integrates a low-noise charge amplifier (CA) with adaptive feedback, test capacitor. The polarity is adjustable by a common to all channel register. The input MOSFET is a p-channel with gate area of $L \times W = 180 \text{ nm} \times 10 \text{ mm}$ (200 fingers, $50 \mu\text{m}$ each) biased at a drain current $I_D = 2 \text{ mA}$; this corresponds to an inversion coefficient $IC \approx 0.22$, a transconductance $g_m \approx 50 \text{ mS}$, and a gate capacitance $C_g \approx 11 \text{ pF}$. The filter (shaper) is a third-order (one real pole and two complex conjugate poles) designed in delayed dissipative feedback (DDF) [2], has adjustable peaking time (25, 50, 100, and 200 ns) and stabilized, band-gap referenced, baseline. The VMM3 was also modified to recover from $\sim 6 \text{ pC}$ within 200 ns. The DDF architecture offers higher analogue dynamic range with a relatively high resolution. The gain is adjustable in eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC).

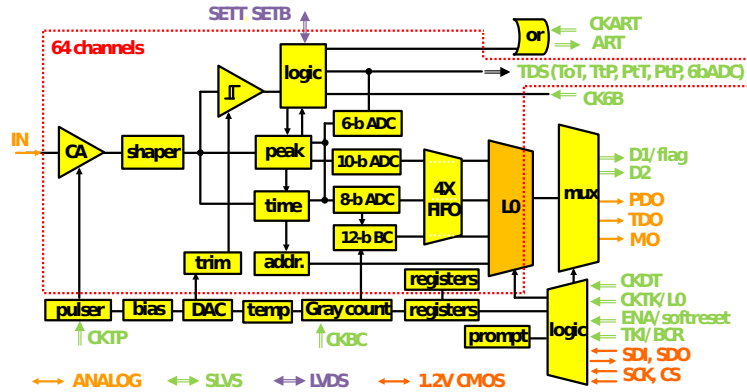


Figure 1: Architecture of VMM3.

Next to the shapers are the sub-hysteresis discriminators [3] with neighbour enabling logic, and individual threshold trimming, the peak detector, and the time detector. The sub-hysteresis function allows discrimination of pulses smaller than the hysteresis of the comparator circuit. The threshold is adjusted by a global 10-bit Digital to Analogue Converter (DAC) and an individual channel 5-bit trimming DAC. The neighbour channel logic forces the measurements of channels neighbouring a triggered one, even those channels did not exceed the set threshold and extends to two neighbouring chips through bidirectional IO. The peak detector measures the peak amplitude and stores it in an analogue memory. The time detector measures the timing using a time-to-amplitude converter (TAC), i.e., a voltage ramp that starts either at threshold crossing or at the time of the peak and stops at a clock cycle of the BC clock. The TAC value is stored in an analogue memory and the ramp duration is adjustable in four values (60 ns, 100 ns, 350 ns, 650 ns). The peak and time detectors are followed by a set of three low-power ADCs (a 6-bit, a 10-bit, and a 8-bit), characterized by a domino architecture [4] but of a new concept. The ASIC includes an adjustable pulse generator connected to the injection capacitor of each channel, adjustable with a global 10-bit DAC, and triggered by an external clock. Finally, the ASIC integrates analogue monitor capability to directly measure the global DACs, the band-gap reference, the temperature sensor, the analogue baseline, the analogue pulse, and the channel threshold (after trimming).

2. Readout Modes

The ASIC can be readout in a two phase analogue mode, in a continuous simultaneous read/write mode and in the so-called Level-0 mode. It implements other independent data paths like the Address in Real Time¹ (called ART and used in the Micromegas trigger schema) and the direct outputs of all 64 channels in parallel, in one of five selectable formats², used in the sTGC trigger.

In the two phase mode data are registered while the VMM is in acquisition mode and then read out, after the system is switched to the read out mode (mode originally implemented in the VMM1). The set of amplitude and time voltages is made available at the analogue outputs and digitised externally while the address of the channel is serialized and made available at the data output. Acquisition is re-enabled after the readout phase is completed.

In continuous mode the simultaneous read/write of data assures dead-timeless operation that can handle rates up to the maximum of 4MHz per channel (250ns digitisation from the 10-bit ADC). In this mode the peak and time detectors convert the voltages into currents that are routed to the 10-bit ADC and 8-bit ADC respectively. The 8-bit ADC provides the conversion of the timing measured using the TAC from the time of the peak or the threshold to a stop signal (CKBC). The bunch crossing counter value at the TAC stop time is latched into a local 12-bit memory, thus providing a total of 20-bit deep time-stamp with a nanosecond resolution. In continuous (digital) mode a total of 38-bits are generated for each event. The event is read out using a token-passing scheme where the token is passed first-come first-serve only among those FIFOs that contain valid events. The data in the FIFOs is thus sequentially multiplexed to the two digital outputs. A timing diagram of this readout mode is shown in the Figure 2 (left).

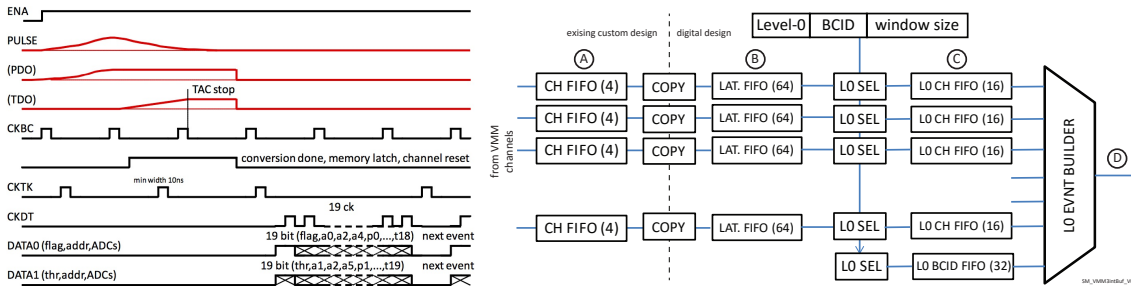


Figure 2: Left: Data Readout with ADCs (continuous mode, 1 bit/ck). Right: The FIFO structure and the trigger matching architecture of the Level-0 mode.

In the Level-0 mode the event processing is done in the same way but the readout is different. Each channel has a Level-0 Selector circuit which is connected to the output of the channel's latency FIFO as shown in Figure 2 (right). The selector finds events upon an external trigger within a selectable window and copies them to the channel FIFO. The data are available at the output of the two data lines and can be readout at a speed of 640 Mbps (160MHz clock, effective bandwidth 560 Mbps due to 8b/10b encoding).

¹The address of the channel with the earliest signal occurred within a clock tick of the CKBC

²time-over-threshold (ToT), threshold-to-peak (TtP), peak-to-threshold (PtT), 10ns pulse occurring at peak (PtP) or the peak detector output with a 6-bit ADC

3. Detector Performance with the VMM3

The VMM3 was tested with two $10 \times 10 \text{ cm}^2$ resistive strip micromegas prototypes³ with 1D readout at CERN. The strip pitch of those detectors is $400 \mu\text{m}$ and the capacitance is $\sim 30 \text{ pF}$. They were operated with the drift high voltage at -300 V and an amplification high voltage, applied to the resistive strips, of 545 V while the mesh was kept to the ground. The gas mixture used was $\text{Ar}+7\%\text{CO}_2$. The drift gap is 5 mm while the amplification gap is kept at $128 \mu\text{m}$ above the resistive strip⁴.

The noise⁵ of the VMM3 was measured on the monitoring output of the VMM with an oscilloscope while the board was mounted on the detector or being on the bench. The measurement was converted to equivalent noise charge (ENC). Figure 3 shows the noise levels of the VMM3 as a function of the electronics gain (left) and the setup of two micromegas detectors on the testbeam at CERN (right). It should be mentioned that the measured noise is very close to the intrinsic noise of the ASIC.

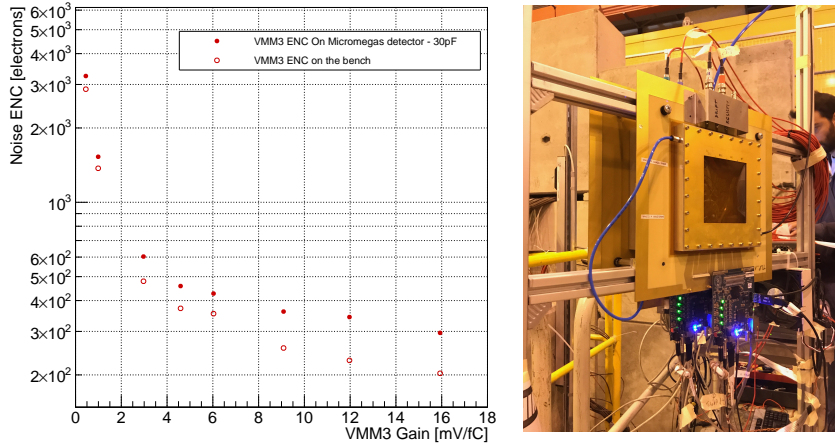


Figure 3: Left: The ENC of the VMM3 as a function of its gain. Right: The Micromegas setup at the CERN testbeam.

The data collected were analysed in a way that is described in details here [7]. For tracks perpendicular to the detector surface, the centroid method was used requiring the strips to be adjacent, lie in a time window of 150 ns and being at least two of them to form a cluster. The resolution is calculated from the residual distribution by dividing the result with the $\sqrt{2}$ since those detectors are identical. Figure 4 shows the residual distribution obtained with tracks perpendicular to the detector surface, reconstructed with the centroid method (left). The distribution is corrected for alignment and rotation between the two detectors.

Data analysis was also performed with tracks inclined by 30° with respect to the detector precision coordinate. The tracks were reconstructed with the μTPC method[7]. For the cluster selection,

³Similar setup was used before [5].

⁴Those micromegas detectors are of bulk technology[6] by the pillar structure.

⁵For the measurement the oscilloscope was set to measure the peak to peak variance and the standard deviation of one thousand random triggers was used.

the Hough transform was used to reject noise and three strips were the minimum requirement to form a cluster. Figure 4 shows the distribution of the residuals (resolution quoted is divided by $\sqrt{2}$) for the events reconstructed. The distributions of Figure 4 are fitted with a double-Gaussian function to account for the tails.

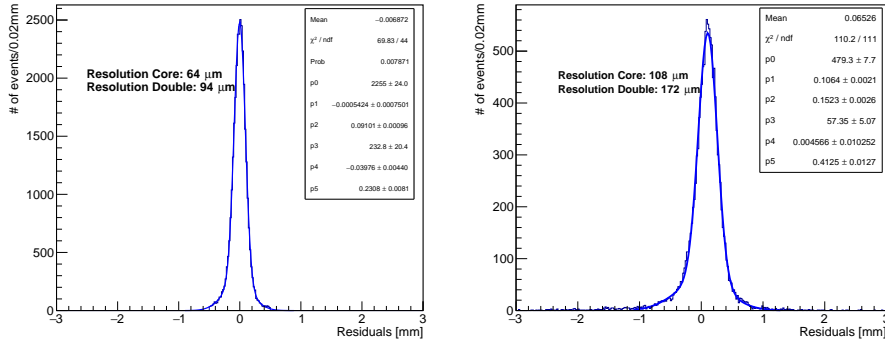


Figure 4: Left: Residual distribution for perpendicular tracks. Right: Residual distribution for tracks under 30° .

The performance of the ASIC with the prototype micromegas detectors is as expected. The spatial resolution measured is consistent with earlier measurements performed by different electronics [8]. Further improvements are expected with the new prototype of the ASIC called VMM3a.

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