PROCEEDINGS OF SCIENCE

New Muon Trigger Chambers for ATLAS Phase I upgrade: DAQ system

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The ATLAS muon spectrometer is an essential component of the detector, providing trigger and track reconstruction for every physics process containing high-energy muons. This is possible thanks to the combination of different tracking sub-detectors, providing both a very fast trigger system and an accurate track reconstruction. A dedicated toroidal magnetic field, in order to measure the muon momentum, is provided in this outer region of the detector. The higher interaction rate that the ATLAS muon barrel detector is going to sustain after the Phase I upgrade due to the increased LHC luminosity requires a better fake track rejection in critical detector regions without hindering the trigger efficiency. This is accomplished by adding new trigger chambers, in particular in the pseudo-rapidity region $1<|\eta|<1.3$. These new detector chambers, denominated BIS78, are updated Resistive Plate Chambers design, thinner than the one previously installed in order to fit in the small space made available by the upgrade of the Monitor Drift Tube chambers. The Trigger and Data Acquisition system for the new detector chambers are illustrated in this presentation, from the Front-End electronics to the Read-Out software, including results from prototype tests. The system is comprised of a combination of custom and commercially available hardware of the same type that will be adopted by every ATLAS system the in High Luminosity LHC (ultimate luminosity $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$), after the end of the Phase II detector upgrade ($\sim$2025), thus representing also a first test-bench for the whole detector.

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1. Introduction

LHC Phase I interaction rates require improved fake trigger rejection and efficiency, especially in the transition region $1 < |\eta| < 1.3$. As a part of the BIS78 project, new thin-gap Resistive Plate Chambers (RPC) will be installed there, providing more track points for reconstruction and fake rejection. This is also a pilot project for the HL-LHC large scale upgrade of the BI layer [1].
Data Acquisition must process data at the design rate of the RPC's $\sim 10\,\mathrm{kHz/cm^2}$, providing the first level trigger information within the ATLAS $\sim 2.2\,\mu$s latency window.
In this document the Data Acquisition system of the new RPC's installed in the barrel region is treated. Its structure is shown in Figure 1. The on-detector Front-End amplifies the chamber signals, acts as hit discriminator and sends LVDS signals to the High Performance Time-to-Digital Converters. This information is sent to the trigger system and prepared for acquisition. If the trigger accept is positive the data is sent over optical fibre to the Read-Out board, that aggregates data from several chambers and propagates back the trigger accept signals. The Read-Out software connects to the board PC, reading the data for monitoring and storage and sends configuration files to the Front-End

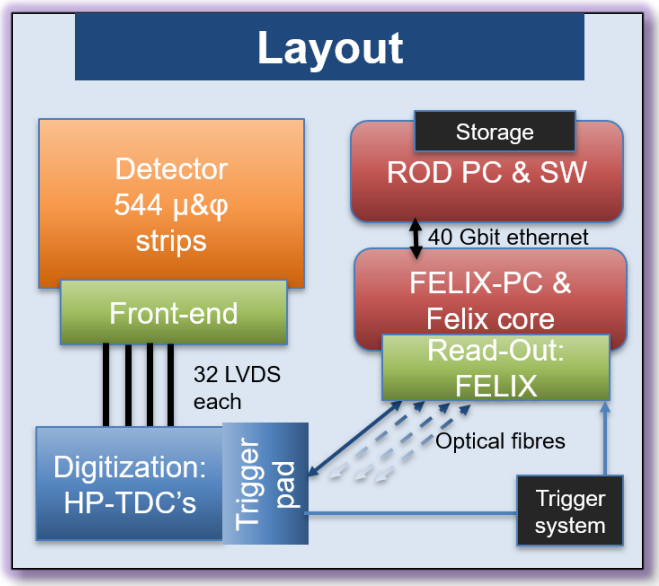

Figure 1: Structure of the DAQ system for the barrel RPC chambers that will be installed for the Phase I upgrade.

2. Thin RPC's

A new generation of Resistive Plate Chambers, thinner than the ones previously produced, are going to be installed in the small space made available by the upgrade of the MDT chambers for the New Small Wheel detector. 16 BIS78 triplet chambers are planned to be built, characterized by

1 mm gas gaps and 1.2 mm electrodes (HPL laminate). The final prototype, shown in Figure 2, has already been tested.

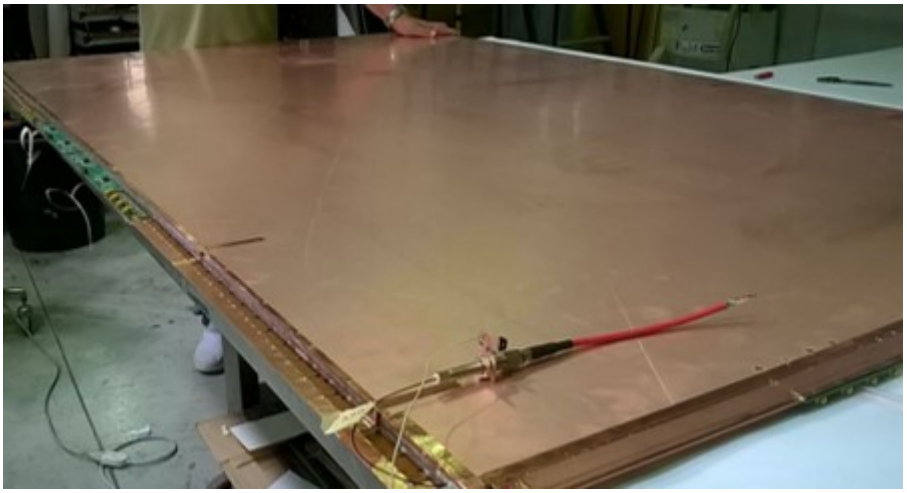

Figure 2: The new thin RPC triplet prototype tested at CERN.

3. Front-End electronics

The chamber FE is the first step in the acquisition chain, residing on the detector digitize the signal with the minimum necessary amplification; the electronic system comprises:

- a Si amplifier, with an amplification factor of $2-4\,\mathrm{mV/fC}$, a power envelope of $3-5$ V, $1-2$ mA and a bandwidth of 100 MHz;
- a SiGe custom discriminator with a threshold of 0.5 mV, a power envelope of $2-3$ V, $4-5$ mA and a bandwidth of 100 MHz;
- an LVDS transceiver.

A flat connector technology has been developed to fit in the very tight spaces in which the chambers will operate, at the same time maintaining the largest possible acceptance. After a careful study of the signal noise and degradation, LVDS signals were chosen for transmission for their high reliability.

4. Digitization

Coincidence measurement is based on High Performance TDC's (7-bit, 195 ps time resolution). 3 HPTDC-GOL (Gigabit Optical Link) pairs compose each mezzanine card, installed on a common motherboard [2] that can house and power up to 6 cards thanks to 8 FEAST circuits. The board is shown in Figure 3. Each motherboard will read a triplet chamber, servicing 544 RO strips.

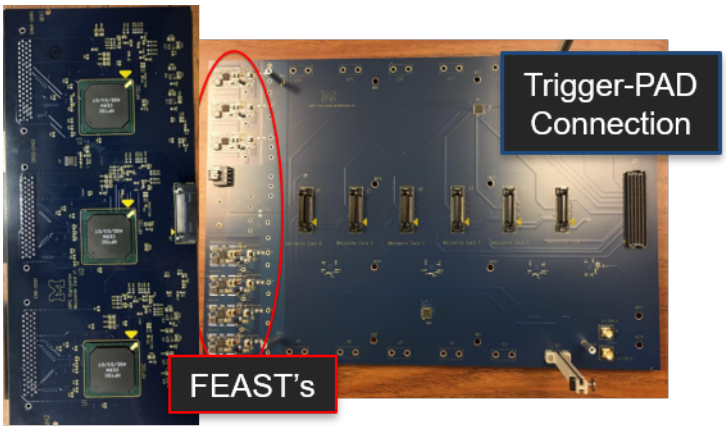

Figure 3: An HPTDC-GOL mezzanine and 6-board motherboard.

5. Trigger PAD

An FMC processor board was developed to process trigger information, read out the formatted data, enforce 0-suppression, control the JTAG chain and monitor currents, voltages and temperatures. The processor board features an HPC-FMC connector, a Kintex-7 FPGA for data processing, a GBTx chip to handle transceiver communication and to operate the GBT-SCA chip, which in turn handles the JTAG chain and the sensors. It is powered by several FEAST circuits. The transmission to and from the FELIX board will be at 320 Mbit/sec, using the GBT protocol, while communication to the GBT-SCA is performed with the HDLC protocol at 80 Mbit/sec. The PAD will also send the RPC data to the trigger system, receiving back the LVL1 Accept from the TTC system through Felix.

6. Read-Out electronics and software

The ATLAS TDAQ system for HL-LHC will be based on the FELIX (Front-End LInk eXchange card) [3] to aggregate signals from the GBTx chips on the Front-End systems and to communicate with them, sending configuration and trigger signals. The BIS78 project is among the few early adopters, starting from its Phase I implementation.
The data is sent over PCIe to a local software core and then to the local or remote Read-Out software (SW ROD). The functions of the Read-Out electronics and software are: propagation of the ATLAS clock and trigger signals, Front-End configuration, data-fragment aggregation, data monitoring and ultimately event building.
The current system prototype uses the Xilinx VC709 demo board as a FELIX temporary solution. The prototype Read-Out can already receive data over the links and monitor them through polling, as well as send commands to the GBT-SCA.

7. Current developments

The thin RPC prototypes are now undergoing a long series of tests using muon beams at

CERN. The results will be used to finalize the design for the full-scale production. The on-detector Front-End electronic system has also been extensively tested at the same time. After performance testing with generated data, the TDC system has also been included in one of these test-beams, showing its capabilities and pointing towards the current development. The full DAQ chain has not yet been validated.
With the end of the ATLAS data taking in December 2018 the project will enter in the production and installation phases. On the DAQ side this means that by then the essential features of the system have to be implemented, all the prototypes tested and the Final Design Report be compiled. There are still some items that need to be addressed before the system installation and commissioning, taking place during the long 2019-2020 shut-down:

- GBTx configuration needs to be finalized and tested.
- The PAD firmware needs to be functional and tested.
- The configuration system needs to be moved from standalone tools to one based on the OPC-UA server structure, with communication integrated in the DAQ ROD software and DCS systems.
- The DAQ monitoring system will need to handle all of the data coming from at least a PAD board.
- The DCS system needs to support the advanced monitoring and diagnostics

The BI RPC Phase-II upgrade will benefit directly from the BIS78 R&D program, design effort and installation and operations experience. The core features will thus be tested and evaluated in a real running environment before Phase II, allowing for a more stable and reliable core performance.

References

[1] ATLAS Collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer*, 2017, LHCC-2017-017

[2] X.T. Meng et al, *A readout digitization system for the ATLAS muon spectrometer phase-I tRPC trigger upgrade*, 2017, JINST 12 T10007

[3] J. Anderson et al, *FELIX: a PCIe based high-throughput approach for interfacing Front-End and trigger electronics in the ATLAS Upgrade framework*, 2016, JINST 11 C12023