PROCEEDINGS OF SCIENCE

Integration and Commissioning of the ATLAS Fast TracKer system

Milene Calvetti[*ab] **and Nicolò Vladi Biesuz**[b] **on behalf of the ATLAS collaboration**
[a] *University of Pisa*
[b] *INFN Pisa*
E-mail: milene.calvetti@cern.ch, nicolo.vladi.biesuz@cern.ch

The Fast TracKer (FTK) system is a track reconstruction processor designed to perform full event tracking synchronously with the ATLAS Level 1 trigger acceptance rate. The high-quality tracks produced by the system will be used by High Level Trigger algorithms to improve the identification of physics objects such as b-jets and taus, as well as to help mitigate the effects of pile-up. The combinatorial challenge of the global track finding requires the use of a custom designed track processor. The idea behind FTK is to simulate all possible tracks before an ATLAS data-taking run. During the actual data-taking, the hits coming from the detector are compared with the hits expected from the simulated tracks. This comparison or 'pattern matching' is then followed by a two step linearized track fit. This task is executed by a system of seven custom electronics board types that will process data from the Inner Detector at the 100 kHz rate of the Level 1 trigger. Currently, the FTK system is under installation and commissioning into the ATLAS Data Acquisition System. The status of the system integration is presented and a review of the first data collected by the FTK system is shown.

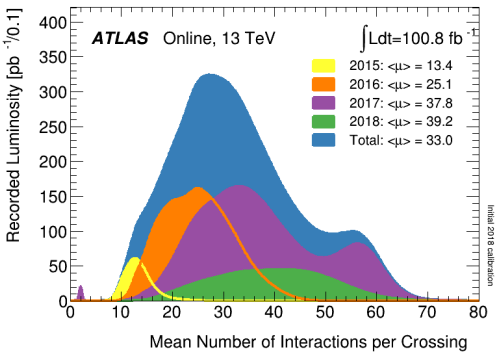
Sixth Annual Conference on Large Hadron Collider Physics (LHCP2018)
4-9 June 2018
Bologna, Italy

*Speaker.

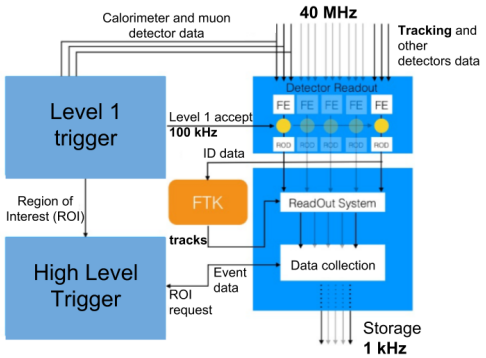
PoS(LHCP2018)028

1. LHC challenges and the ATLAS Fast TracKer (FTK) system

The Large Hadron Collider (LHC) second data-taking run (Run 2) begun in 2015 and is currently ongoing. During this run the accelerator performances steadily increased. Therefore the experiments operating at the LHC are faced with more and more challenging data-taking conditions. A critical parameter for the experiments is the mean number of interactions per bunch crossing (pile-up). As shown in Figure 1a this parameter has reached a maximum of ≈ 60 interactions per bunch crossing in proton-proton collision collected by the ATLAS detector, operating at LHC. During the next data-taking phase foreseen by 2021 (Run 3), the luminosity will be leveled at or above pile-up of 60. Track-based trigger selection is fundamental for selecting events with good purity and efficiency. At the same time, high pile-up constitutes a major combinatorial challenge to tracking, which is currently limited by available CPU resources. This challenge has been addressed in ATLAS by designing the FTK system, a track reconstruction processor able to perform full event tracking at a rate of 100 kHz with a latency of $\approx 200\,\mu$s.



(a)



(b)

Figure 1: (a) Luminosity-weighted distribution of the mean number of interactions per bunch crossing for the 2015-2018 collision data. All data recorded by ATLAS during stable beams is shown [2]. (b) ATLAS trigger diagram including the FTK system.

The FTK system is being installed and it will be fully integrated in the ATLAS trigger during the shutdown period foreseen in 2019-2020. A schematic diagram of the ATLAS trigger, including the FTK system, is shown in Figure 1b. The ATLAS trigger system consists of a hardware-based first-Level trigger (L1) and a software-based High-Level Trigger (HLT) implemented on standard CPUs [1]. The L1 trigger, using input from the calorimeters and from the muon system, reduces the event rate from about 40 MHz (the bunch crossing rate) to about 100 kHz. Events accepted by the L1 trigger are buffered in the Read-Out-System to be processed by the HLT. The HLT uses the Region-of-Interest (RoI) information from L1 and the data from the RoI regions to reconstruct trigger objects and to reduce the output rate to 1 kHz.

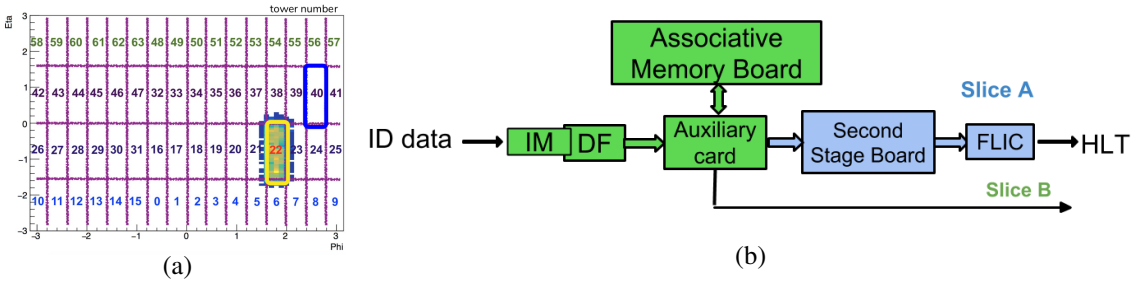
The information from ATLAS tracking detectors is presently exploited in the HLT only for a subset of the events or for limited detector regions (RoIs) due to timing limitations. The FTK system will process data from the ATLAS Inner Detector (ID) for the full event and it will perform tracking for all events accepted by L1 [3].

The key idea of the FTK system is to simulate all possible tracks before an ATLAS data-taking run

and to compare the ID hits with the hits expected from the simulated tracks as they are read out. The comparison is performed using a dedicated content addressable memory chip, the associative memory, and using high performance Field Programmable Gate Arrays to provide the needed computing power.
The FTK system will provide full-event reconstruction of all tracks with $p_T > 1$ GeV with resolutions close to those found by offline track reconstruction. Extensive use of FTK tracking, including vertexing using those tracks, will be exploited by HLT algorithms to improve the identification of physics objects such as b-jets and τ leptons [4]. Information from tracks provided by the FTK system will also improve secondary vertex identification and help mitigating the effects of pile-up. It will as well allow the use of looser HLT jet thresholds and therefore help to refine the missing transverse momentum. The system will allow the design of new trigger algorithms specific for analysis channels using objects that will be better identified with FTK, and at a lower energy threshold, such as $hh \to b\bar{b}b\bar{b}$, fundamental for studying the Higgs boson self-coupling at the LHC.

2. Hardware for the FTK system

FTK is a highly parallelized system; the information from the ID is divided in 64 $\eta \times \phi$ towers processed in parallel by custom electronics boards (FTK slice). The numbering of the 64 towers is shown in Figure 2a.



(a) (b)

Figure 2: a) $\eta \times \phi$ position of the 64 ID towers.
(b) Diagram of the electronic boards forming FTK slices. The configuration of two test slices is stressed. Slice A is a full FTK slice while Slice B is a partial slice and the AUX card directly sends 8-layers tracks to the Read-Out system.

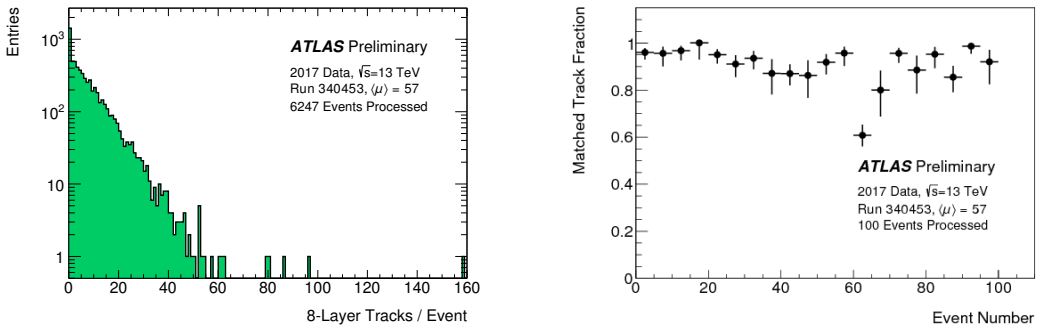
A diagram of an FTK slice, showing the connections between the electronic boards, is presented in Figure 2b. The boards receiving inputs from the ID are the Input Mezzanines (IM): these boards handle the inputs and perform the hit clustering. The Data Formatter boards (DF) receive the clusters and distribute them to the FTK towers. Clusters are then grouped by the Auxiliary card (AUX) into coarse resolution hits that are sent to the Associative Memory Board (AMB). In the AMB, the coarse cluster information is compared simultaneously to O(10^9) patterns determined from simulation. The hits matching a pattern are used by AUX cards to perform a first-stage fit with 8 silicon detector layers. A cut on the fit quality helps to further reduce the data-flow to Second Stage Board (SSB). The SSB retrieves the hit information on four additional silicon detector layers from the DF and performs a 12-layer fit. The second fit, performed with 12 layers reduces strongly the number of fake tracks and increases the final track quality. Finally the tracks are converted to the ATLAS format and sent to the HLT by the FTK to Level-2 Interface Card (FLIC).

3. First data processed with FTK

The FTK system is currently under installation and commissioning with two of the FTK slices being used for testing. The two slices are Slice A, a full FTK slice receiving data from tower 22 and saving 12-layer tracks, and Slice B, a partial slice receiving data from tower 40. In Slice B, data processing is stopped after the AUX card, which outputs 8-layer tracks directly to the Read-Out-System (Figure 2b). For commissioning purposes the input rate for the FTK processing can be controlled by prescaling: the plots shown in this section correspond to the FTK operation at the rate of 35 kHz.

During Run 3 ATLAS will collect events at very high pile-up, so it is important to test that the system can cope with such harsh conditions. The number of 8-layer tracks produced per event from FTK Slice B is shown in Figure 3a. The average number of interaction per bunch crossing for the data shown is $\langle\mu\rangle = 57$. The high number of tracks processed per event tests the ability of the system to run in a high pile-up environment.

During the FTK design phase the full FTK data processing pipeline has been simulated to support the hardware design and to develop trigger strategies at high luminosity [5]. A first test has been done by running the FTK simulation on a subset of the data processed by Slice B (100 events). The FTK simulation inputs are therefore real data, at detector level. The simulation output tracks are then compared with the FTK hardware output. The result of this test is shown in Figure 3b and Figure 4. The fraction of output tracks matched with the tracks produced by running the simulation on the subset of data is shown in Figure 3b. The same data-sample has been also used to study the



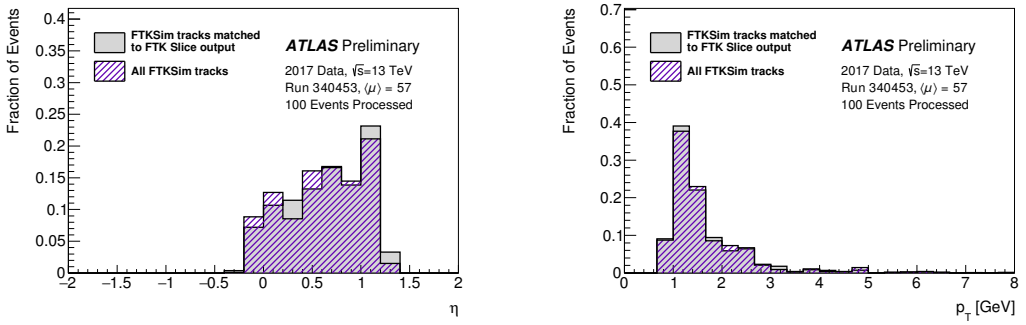
(a) (b)

Figure 3: (a) Number of 8-layer tracks produced per event by FTK Slice B.
(b) Fraction of FTK slice output tracks that are matched to tracks produced by running FTK simulation on a subset of the events processed by Slice B (100 events) [4].

accuracy of the simulation in reproducing the shape of the transverse momentum p_T, η and ϕ. In Figure 4 the distribution of the fraction of simulated tracks that were matched to the tracks output by the FTK Slice B as a function of p_T and η is compared with the distribution of all simulated tracks.

4. Plans for the future

The goal for the next two years is to fully validate FTK so that the HLT can trigger on its output



(a) (b)

Figure 4: The p_T (a) and η (b) distributions of simulated 8-layer FTK tracks that are matched to tracks output by the FTK slice. Data corresponding to a subset of the events processed by the FTK slice is used as input to the simulation (100 events). The distributions of matched simulated tracks (grey) is compared to all simulated tracks for the same events (purple) [4].

in the next data-taking run, planned to start in 2021. The FTK system performance is currently being evaluated using FTK data collected by the two test slices. The installation and initial commissioning of half FTK coverage is scheduled to be completed in 2018. Further validation and optimization will be performed during the LHC shutdown (2018-2020) using simulated data. Validation of patterns will be done running the FTK simulation on collision data collected during Run 2. All FTK boards will be installed during 2019 and 2020 to have a fully functioning system for Run 3.

5. Conclusions

The FTK track processor will be a crucial component to improve the ATLAS trigger and cope with the demanding condition caused by the improved performance of the LHC accelerator during Run 3. It will able to perform full event tracking synchronously with the ATLAS Level 1 trigger acceptance rate. The FTK system is currently under commissioning and the first processed data are available. The first studies on the data processed by a single slice that outputs 8-layer tracks proved the ability of the system to cope with events containing a high number of tracks. It also allowed for the study of the accuracy of the matching between FTK simulation and the hardware.

References

[1] ATLAS Collaboration, "The ATLAS Experiment at the CERN Large Hadron Collider," JINST **3** (2008) S08003. doi:10.1088/1748-0221/3/08/S08003

[2] ATLAS luminosity public results: `https://twiki.cern.ch/twiki/bin/view/AtlasPublic/LuminosityPublicResultsRun2`

[3] A. Annovi *et al.*, "Design of a hardware track finder (Fast TracKer) for the ATLAS trigger," JINST **9** (2014) no.01, C01045. doi:10.1088/1748-0221/9/01/C01045

[4] FTK public results: `https://twiki.cern.ch/twiki/bin/view/AtlasPublic/FTKPublicResults`

[5] J. Adelman *et al.*, "ATLAS FTK Challenge: Simulation of a Billion-fold Hardware Parallelism," Procedia Comput. Sci. **66** (2015) 540. doi:10.1016/j.procs.2015.11.061