PROCEEDINGS OF SCIENCE

Hardware Trigger Processor for the MDT System

Thiago Costa de Paiva[*†]
University of Massachusetts Amherst
E-mail: tcpaiva@cern.ch

We are developing a low-latency hardware trigger processor for the Monitored Drift Tube system for the Muon Spectrometer of the ATLAS Experiment. The processor will fit candidate muon tracks in the drift tubes in real time, improving significantly the momentum resolution provided by the dedicated trigger chambers. We present a novel pure-FPGA implementation of a Legendre transform segment finder, an associative-memory alternative implementation, an ARM (Zynq) processor-based track fitter, and compact ATCA carrier board architecture. The ATCA architecture is designed to allow a modular, staged approach to deployment of the system and exploration of alternative technologies.

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[*]Speaker.
[†]on behalf of the ATLAS Collaboration

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The Large Hadron Collider (LHC) will enter in the High Luminosity (HL) era, named as HL-LHC, around 2025 with a nominal leveled instantaneous value of $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, and the goal of the HL-LHC upgrade of ATLAS [1] is to maintain the necessary performance of the precision measurements. In order to improve the muon trigger system rate under that challenging condition, the ATLAS Experiment [2] will include Muon Drift Tube (MDT) chamber information to the Level-0 trigger, making use of information from surrounding detectors, Figure 1.

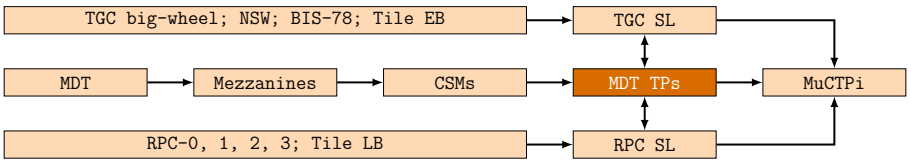
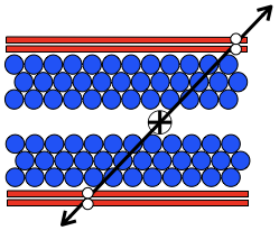


Figure 1: MDT trigger processor in the ATLAS muon system context will receive information from surrounding detectors to constraint track searches and reduce latency.

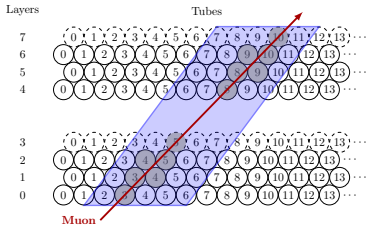
Basically, this proposal is divided in three major stages. First, search for hits are constrained as explained in Section 1. Then Segment Finders look up for pieces of tracks in stations, which is described in Section 2. And finally, those segments are connected to each other by the track fitter, as shown in Section 3. Section 4 details the proposed processing structure envisioned.

1. Hit Extraction

An Region of Interest (ROI) is determined in the barrel Sector Logic (SL) from a coincidence of hits in the Resistive Plate Chambers (RPCs) trigger system likely to be originating from a single track. Reference segments are reconstructed per MDT station from these RPC hits, Figure 2(a), each one used to generate an ROI where track hits can be identified, Figure 2(b). A similar process is applied with respect to the end-cap and the Thin Gap Chambers trigger system. Matching of MDT hits to ROI will be performed in an Field Programmable Gate Array (FPGA). Tube coordinates are transformed to convenient station-local coordinates, drift time is converted into distance, and information is sent to the segment finder modules.



(a) Reference segment reconstructed with information from surrounding detectors.



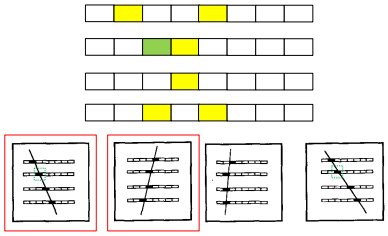
(b) MDT hits matching in an ROI built from the reconstructed reference segment.

Figure 2: ROI reconstruction from surrounding detector systems and matched MDT hits in an ROI region.

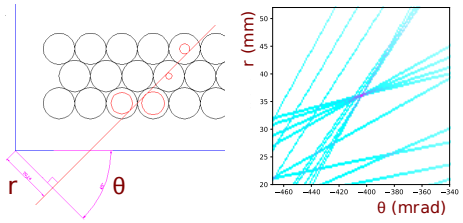
2. Segment Finding

After the MDT hits are selected in accordance with an ROI, MDT segments are reconstructed within the scope of a station. One of the proposed designs under consideration for this stage is the content-addressable memory, also known as Associative Memories (AM). This devices store a library of all possible track patterns and compare actual hits against the track patterns, producing a low-resolution segment candidate, Figure 3(a).

The second approach, Figure 3(b), uses FPGA logic to implement a Legendre Transform (LT) based segment finder. This logic evaluates in parallel a total of 128 possible track segment angles for each MDT hit, calculating in a fast FPGA pipeline the offset of each track candidate from an arbitrary origin for each angle. The (angle, offset) pairs are used to fill a 2D histogram, with the maximum peak in the histogram representing a likely track where a number of drift circles concur on the position and angle [3]. As part of the filling process, the 128 highest-occupancy bin locations are maintained, so finding the overall histogram maximum requires only a few clock cycles. Preliminary results indicate that the total latency to process 100 MDT hits in an ROI is less than 1 µs.



(a) Track patterns from hits using AM technique.



(b) A track is identified by coincidences of curves after LT is applied on hits.

Figure 3: Segment finding approaches under consideration.

3. Track Fitting

Each station (inner, middle, outer) will process hits and identify track segments independently. After that, all information will be used to evaluate a final parameterized track fit. Depending on how many segments can be reconstructed per muon candidate in the different MDT stations, the muon's transverse momentum (p_{T}) can be determined using two different methods [4].

If three segments are found, Figure 4(a), each in a different MDT station, the positions of these can be combined to measure the track curvature by calculating the sagitta from the three points (3-station method). Otherwise, two segments in different MDT stations still can be combined to extract the p_{T} by measuring their deflection angle (2-station method), Figure 4(b).

(a) Track fitting by Sagitta method.

(b) Track fitting by deflection angle.

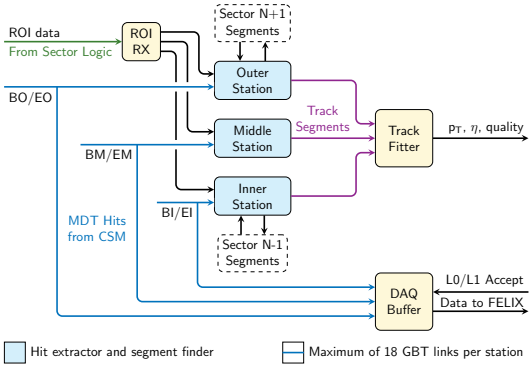
Figure 4: Track fitting using two different approaches.

4. Hardware description

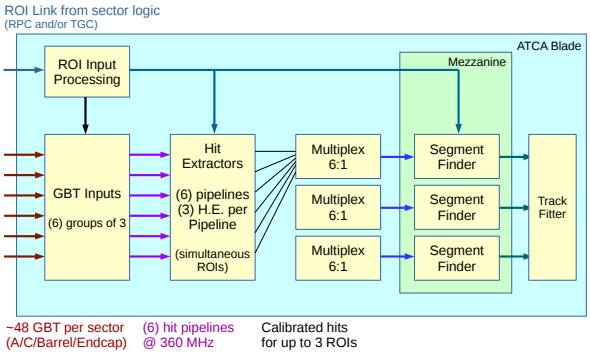
A total of 192 copies of the following logic will be implemented in a set of 64 Advanced Telecommunication Computing Architecture (ATCA) carrier boards. The ATCA standard provides basic services including module and firmware management, power conditioning, and base Ethernet.

The front board is envisioned with one Xilinx Ultrascale-class FPGA which will handle the reception of the MDT data via Multi-Gigabit Transceiver (MGT) links, ROI information, hit extraction and calibration, and transmission of hits to the segment finding modules on attached mezzanines, which makes possible different approaches to be tested.

As illustrated in Figure 5, raw hits are received on three groups of MGTs links from inner, middle and outer MDT stations, ROI data are received on a single fiber per sector from the SL. ROI matched hits are sent to segment finding modules. Segment data is transferred back to the carrier board for track fitting, which results in fitted track parameters transmitted to the Global Muon Trigger.



(a) Data received from detectors are matched upon ROI for each station and than fitted. Raw data is kept in a buffer waiting for requests.



(b) Distribution of the trigger path (ROI matching, segment finder, track fitter) on hardware, where data is multiplexed according to resources availability.

Figure 5: Overview and trigger path diagrams.

The combination of FPGA with Central Processing Unit (CPU) in the Xilinx Zynq chip provides an Ethernet interface and might also be used to implement certain track fitting algorithms. The Zynq device requires Random Access Memory (RAM) for its operating system as well as an interface to a μSD card or other flash file system storage.

In addition, the carrier board FPGA will transfer the MDT hits to the ATLAS Data Acquisition (DAQ) via Front End LInk eXchange (FELIX) system. Figure 6 shows that all hits are buffered and are matched to time windows around L0/L1 trigger accept signals; matching hits sit in a second level buffer waiting for readout, which may require an external Double Data Rate (DDR) memory device.

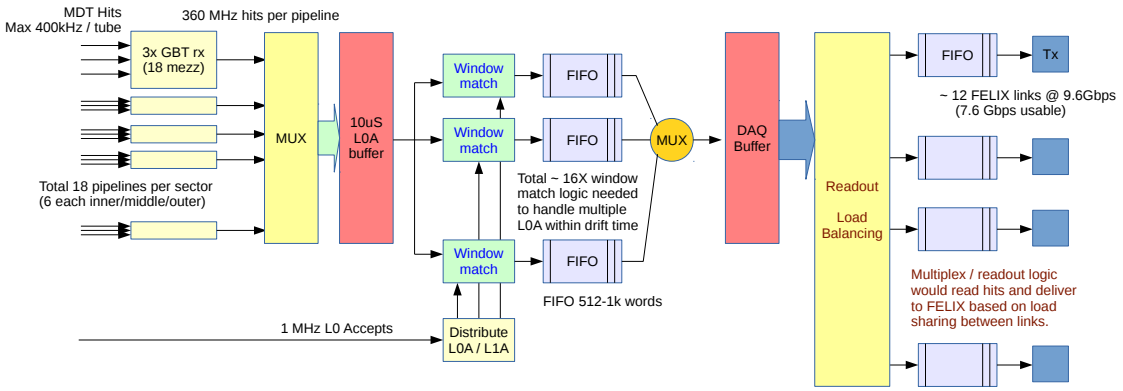


Figure 6: Diagram for the data acquisition part of the MDT trigger system, where hits are buffered for later matching within Level-0/Level-1 requests. Several match engines operates simultaneously. Selected data is then buffered again for load balancing before redout.

5. Conclusions and future work

A very comprehensive and flexible three-stage low-latency ATCA-based hardware trigger processor design has been proposed to meet the requirements for barrel and end-cap MDT detectors, while allowing assessment of different approaches for segment finding. Information from surrounding detectors is used to optimize search procedures.

A detailed conceptual design with extensive simulation studies is being prepared now, to be published in the ATLAS Trigger and Data Acquisition Technical Design Report. A first generation of hardware prototypes is planned for 2018 – 2019, with a full system ready for installation in approximately 2024.

References

[1] ATLAS Collaboration, *ATLAS Phase-II Upgrade Scoping Document*, CERN-LHCC-2015-020. LHCC-G-166.

[2] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, *Journal of Instrumentation* **3** (2008) S08003.

[3] T. Alexopoulos, M. Bachtis, E. Gazis and G. Tsipolitis, *Implementation of the legendre transform for track segment reconstruction in drift tube chambers*, *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* **592** (2008) 456 – 462.

[4] P. P. Gadow, *Development of a Concept for the Muon Trigger of the ATLAS Detector at the HL-LHC*, Master's thesis, Munich, Max Planck Inst., 2016.