PROCEEDINGS OF SCIENCE

The Development of Global Feature eXtractor (gFEX) – the ATLAS Calorimeter Level 1 Trigger for ATLAS at High Luminosity LHC

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Abstract - As part of the ATLAS Phase-I Upgrade, the gFEX is designed to help maintain the ATLAS Level-1 trigger acceptance rate with the increasing LHC luminosity. The gFEX identifies patterns of energy associated with the hadronic decays of high momentum Higgs, W, & Z bosons, top quarks, and exotic particles in real time at the 40MHz LHC bunch crossing rate. The prototype v1 and v2 were designed and fully tested in 2015 and 2016 respectively. A pre-production gFEX board has been manufactured, which is an ATCA module consisting of three UltraScale+ FPGAs and one ZYNQ UltraScale+, and 35 MiniPODs are implemented in an ATCA module. This board receives coarse-granularity (0.2x0.2) information from the entire ATLAS calorimeters on up to 300 optical fibers and 96 links to the L1Topo at the speed up to 12.8 Gb/s.

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1. Introduction

To increase the luminosity in the next ten years, a series of upgrades will be done on the Large Hadron Collider (LHC). The ATLAS [1] experiment will also follow the same upgrade steps. During the so-called Phase-I upgrade, a new component in the first level calorimeter trigger system (called L1Calo) will be upgraded in the ATLAS first level trigger (level-1). It is one of the new components designed to maintain trigger acceptance against increasing luminosity. The gFEX is designed to select large-radius jets, typical of Lorentz-boosted objects, by means of wide-area jet algorithms refined by subjet information.

2. Motivation of gFEX

The high pT bosons and fermions are a key component of the ATLAS physics program. As shown in Fig. 1, the ATLAS Level 1 trigger was designed for narrow jets with limited acceptance for large objects. Including the gFEX in the upgraded system, the acceptance for large radius (large-R) jets will be greatly enhanced.

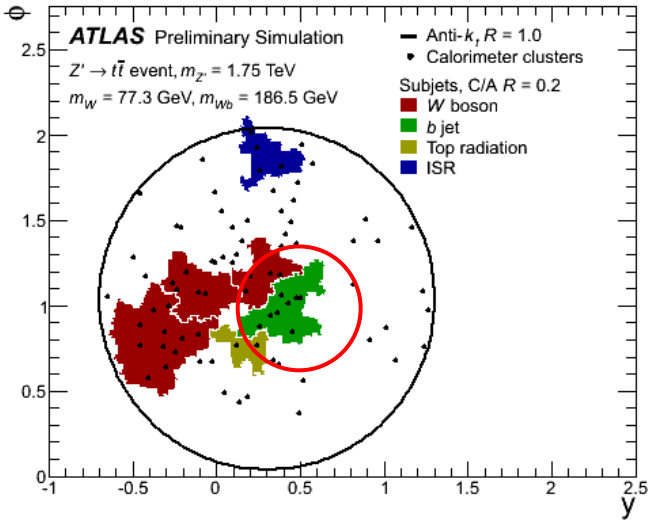

Fig. 1. Effect of jet acceptance with gFEX, compared with current L1 algorithm [9]. The red circle area (R<1) is the L1 narrow jet, and the black circle is the large-R jets with gFEX.

3. gFEX Prototype v2 Design

With the lessons learned from the gFEX v1 prototype [2, 3], a fully functional gFEX v2 prototype is designed. As shown in the Fig. 2, it includes three Virtex Ultrascale FPGAs, one ZYNQ SoC, 28 MiniPODs, and 13 power modules. The MiniPODs are used for the optical links interface with the Liquid Argon Digital Processing Board (LAr LDPB) [4], Level-1 Topological Processor (L1Topo) [5] and the Front-End LInk eXchange (FELIX) [6]. Nine groups of high speed parallel data buses are also implemented on this board between these four FPGAs.

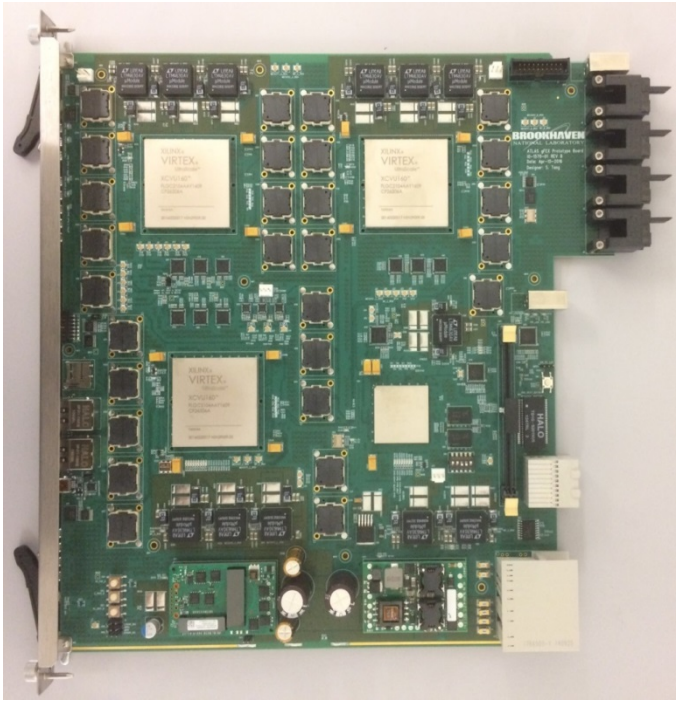

Fig. 2. gFEX v2 board with three ultrascale FPGA, one ZYNQ Soc and 28 MiniPODs

3.1 Power design and sequence

The board is an ATCA based module. The power input source is 48V which is converted to 12V by one DC-DC quater brick module. Then 13 LTM4630As with 26A current capability are used to step down the 12V to 0.95V, 1.0V, 1.2 V, 1.8 V, 2.5 V and 3.3 V respectively. To meet the large current requirement of the Xilinx FPGA, each Virtex Ultrascale FPGA has three LTM4630As.

To protect the board and manage the power sequence of the board, two power monitoring and management chips ADM1066 are used. This chip can be programmed through the I2C bus, so we can define the power sequence, over-voltage and under-voltage based on our requirement.

3.2 High speed parallel data bus and MGTs

There are nine groups of parallel data buses on the board. Six between each two Virtex FPGAs and the other three is between the ZYNQ to another Virtex FPGA. For all the nine groups of parallel data buses, the data rate is 1.12 Gb/s for each data line.

For the MGTs (Multi Gigabit Transceivers) design, there are three kinds of MGTs on the board, GTX on ZYNQ [7], GTH [8] and GTY [9] on the Virtex FPGA. For the MGT connections, there are 280 links connected to the MiniPOD receivers and 40 links to the MiniPODs transmitters and also there are 6 GTY on board connections between processor FPGA A and C, and FPGA A and B respectively, which can run up to 25.6Gb/s.

3.3 ZYNQ FPGA for control and interface

The ZYNQ is used to recover the TTC clock and manage the board, such as monitoring, configuration, and remote upgrade, etc. The Giga-bit Ethernet, QSPI interface, 4Gb DDR3 memories, I2C interface, UART and SD card interface are implemented with the PS system.

4. Test result of gFEX Prototype v2

The functionality and performance tests for the Prototype v2 were done at BNL and also in the integration test of FELIX. The power managment circuit works well as programmed, and all the interfaces of ZYNQ are verified, such as the Ethernet, UART, SD card boot mode and QSPI boot mode. All the optical links and electrical links work as expected.

4.1 Evaluation test at BNL

For the evaluation test, all the functions are verified, including the most important performance tests which are the test of the high speed parallel data bus and the MGT links.

4.1.1 High speed parallel data bus test

The nine groups of parallel data buses are tested with different data patterns (such as PRBS, counter data and constants) to measure their stability and the extension of the stability window for each of them.

With the IP – IDELAYE3[10], we can adjust all the data lines in the ultrascale FPGA. It has 511 steps and each step is about 9.8 ps. All the parallel data buses are running up to 560MHz or 1.12Gb/s with good margin of the stable range.

4.1.2 Link speed test for GTX, GTH and GTY

All optical and electrical links are stable at 12.8Gb/s and all GTY electrical link are stable up to 25.6 Gb/s without any error when doing the IBERT test to 1E-15. Fig. 3 and Fig. 4 show the eye diagram for the 12.8 Gb/s and 25.6 Gb/s of GTY repsepctively.

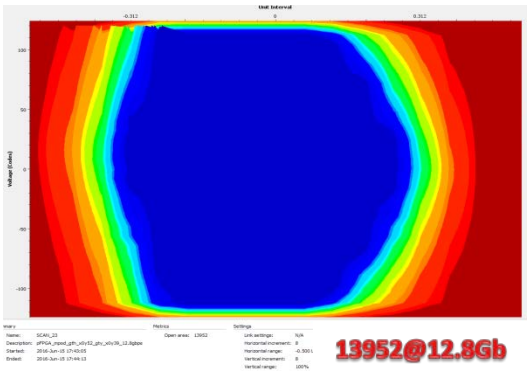

Fig. 3. GTY optical links at 12.8Gb/s

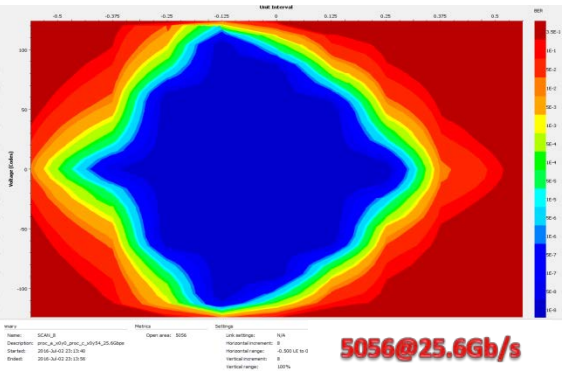

Fig. 4. GTY onboard electrical links at 25.6Gb/s

4.2 Integration test with FELIX

To meet the final design review of gFEX and FELIX, the gFEX and FELIX integration test was carried out at BNL. In this test, the FELIX is used to provide the 40 MHz TTC clock through the GBT link (4.8 Gb/s) and receive the data from gFEX with FULL mode which is 9.6 Gb/s.

The gFEX recovered the 40 MHz TTC clock from FELIX GBT link and then use the on board jitter cleaner (Si5345) to improve the clock quality.

The links from FELIX to gFEX can work well in the latency-fixed GBT mode. The latency is 87.3 ns for FEC mode, and 79 ns for the Wide-Bus mode. The links from gFEX to FELIX can also work well in FULL mode.

With the recovered TTC clock, the GTH can work well at a link speed of 12.8 Gbps, and the GTY work well at 25.6 Gbps. The eye diagrams are shown as Fig. 5 and Fig. 6.

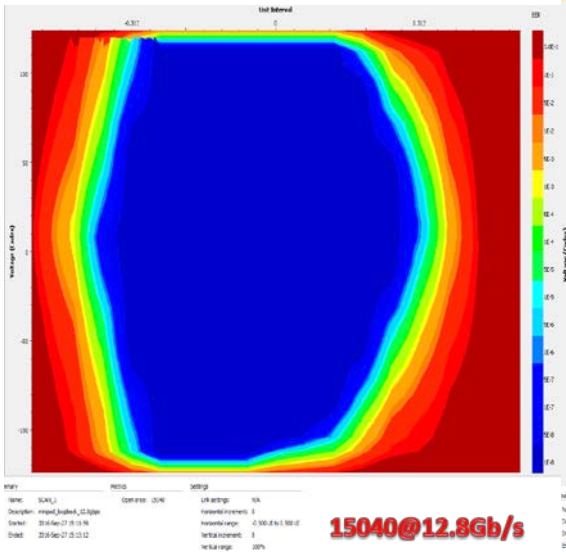

Fig. 5. GTY optical links at 12.8Gb/s

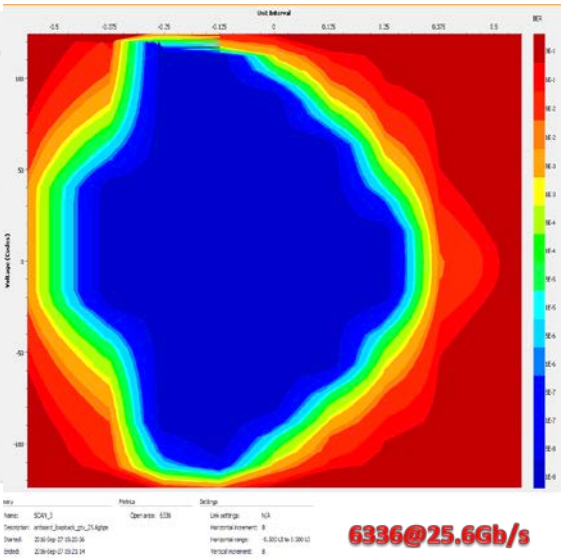

Fig. 6. GTY onboard electrical links at 25.6Gb/s

5. Summary and Conclusion

The gFEX prototype v2 has been used to test all the challenging hardware technology successfully, such as 12.8 Gb/s optical links, 25.6 Gb/s on board electrical links, and 1.12Gb/s on board parallel data buses.

The gFEX prototype v2 has been used in the FELIX integration test, and gFEX firmware development.

A gFEX v3 prototype is also designed and is under testing.

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