PROCEEDINGS OF SCIENCE

The ATLAS Fast Tracker System

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From 2010 to 2012 the Large Hadron Collider (LHC) operated at a centre-of-mass energy of 7 TeV and 8 TeV, colliding bunches of particles every 50 ns. During operation, the ATLAS trigger system has performed efficiently contributing to important results, including the discovery of the Higgs boson in 2012. The LHC restarted in 2015 and will operate for four years at a center of mass energy of 13 TeV and bunch crossing of 50 ns and 25 ns. These running conditions result in the mean number of overlapping proton-proton interactions per bunch crossing increasing from 20 to 60. The Fast Tracker (FTK) system is designed to deliver full event track reconstruction for all tracks with transverse momentum above 1 GeV at a Level-1 rate of 100 kHz with an average latency below 100 microseconds. This will allow the trigger to utilize tracking information from the entire detector at an earlier event selection stage than ever before, allowing for more efficient event rejection. To achieve this goal the system uses a parallel architecture, with algorithms designed to exploit the computing power of custom Associative Memory chips, and modern Field Programmable Gate Arrays. A partial FTK system has been built in 2016, and additional production is ongoing. The system is currently under commissioning. The functionality of the FTK system as well as an overview of the installation and commissioning status are described.

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1. Introduction

The precise Standard Model (SM) measurement and the search for physics beyond the SM are performed with the Large Hadron Collider (LHC) at the European Organization of Nuclear Research (CERN) built in Switzerland and France. Protons are accelerated and collide at a center of mass energy at the TeV scale. The ATLAS detector [1] is placed at one of the interaction points and detects particles which are generated by the interaction of the protons. Many break-through results are obtained such as the discovery of the Higgs boson [2].

To keep or improve the physics sensitivity, the LHC accelerator and the ATLAS detector are planned to be upgraded. The luminosity of the LHC will also be upgraded and become higher. Though more data can be accumulated with higher instantaneous luminosity, it also causes multiple proton-proton interactions per bunch crossing (pile-up) which makes it difficult to distinguish signals from backgrounds, and makes the resolution worse. In 2017, the average number of pile-up events is 40, and it will be more than 60 at LHC Run3 starting from 2021.

Currently two stages of the ATLAS trigger system, the Level-1 trigger and the High Level Trigger (HLT), perform an event selection to reduce the data rate. The events which pass the trigger are stored and used for later analysis. The Fast TracKer (FTK) [3] is a newly installed custom electronic hardware system that performs event-level track reconstruction for the trigger. An overview of the system is shown in Fig. 1. It is implemented between the Level-1 trigger and the HLT. It receives hit information and calculates track information in the entire detector region for all the events which pass the L1 trigger. With the FTK system, the HLT does not need to calculate track information so that it can use the time and track information provided by the FTK for more sophisticated algorithms. The FTK is driven by more than 8,000 ASIC chips and 2,000 Field Programmable Gate Arrays (FPGAs).

2. FTK Working Principle

The FTK utilizes hit information of the tracking detector which are in total about 100M readout channels. To deal with such large input rate, the FTK segments detector regions into 64 η-ϕ towers, each has its own processor. The segmentation is 16 in ϕ and 4 in η. Parallelization is performed on full-mesh Advanced Telecommunications Computing Architecture (ATCA) back plane. A photo of the ATCA crate and an image of data sharing are shown in Fig. 2.

In addition, two key algorithms for fast tracking are implemented which are "pattern matching" and "linear approximation". These processes are done in parallel with 64 η-ϕ towers.

2.1 Pattern Matching

The pattern matching finds track candidates using tracking detector information of 8 layers. Before the operation, a huge amount of track patterns ($>$ 1G patterns) are prepared in advance which consist of coarse resolution hit information which is called Super-Strip (SS). During operation, hit information from the inner detector is transformed into SSs. The input SS and the SSs in the prepared patterns are compared, and all of the matched SSs in the prepared patterns are marked. Then the patterns with all layers or 7 out of 8 layers of the SSs are marked and detected as a track candidate. This comparison process is iterated until all the hit information in an event are loaded.

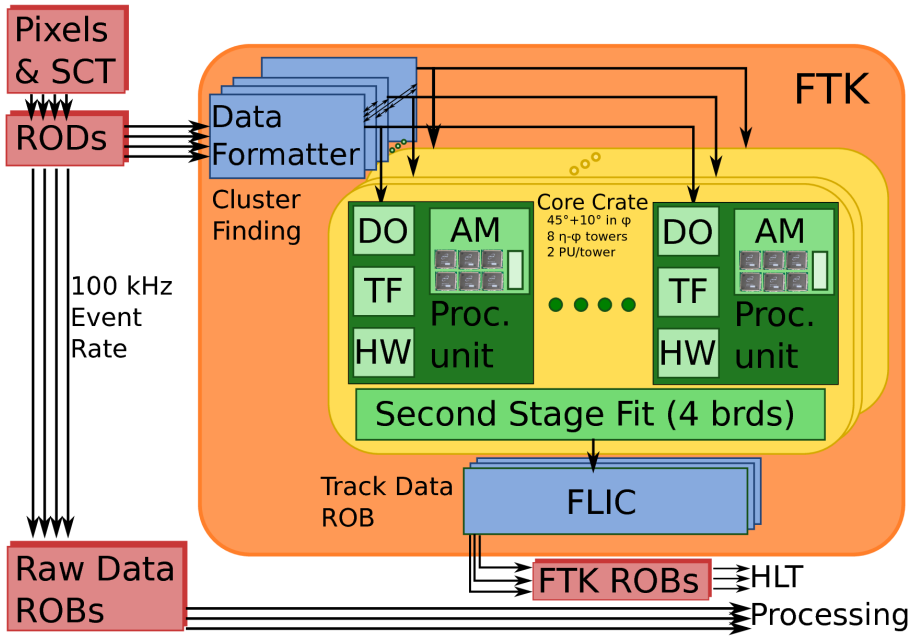

Figure 1: A functional overview of the FTK system. FTK consists of combination of electric boards which are Input Mezzanine (IM), Data Formatter (DF), AUXiliary Card (AUX), Associative Memory (AM), Second Stage Board (SSB), and FTK to Level-2 Interface Card (FLIC).

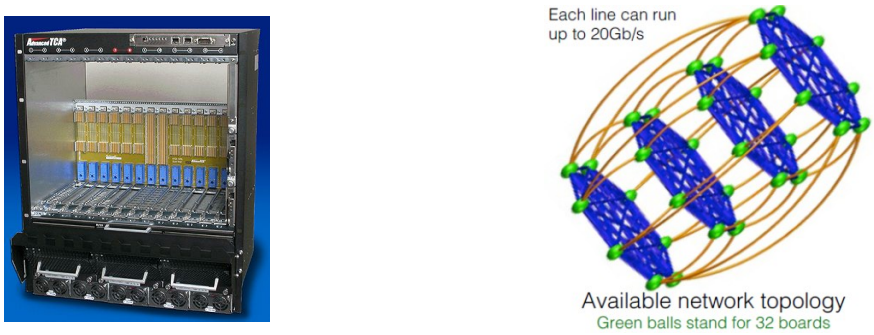

Figure 2: A photo of the ATCA crate (left) and an image of data sharing (right). The green balls represent boards implemented in the ATCA crate, the blue lines represent communication within a crate, and the orange lines represent inter crate communication.

When the input SS matches with the SS in the stored pattern, the Set-Reset Flip-Flop belonging to the pattern memory cell becomes high. Since pattern matching algorithm just takes the logical "AND", the SS comparison with all patterns finishes at one clock after the hit is loaded. Thus the pattern matching is completed at the next clock after the final hit in the event is received.

The patterns are stored in ASIC chips developed specifically for the FTK, which are called Associative Memory (AM) chips [**?**]. The AM chip has been improved significantly during the recent a few years. The initial SVT [6] at the CDF experiment utilized VLSI [7] to store patterns. It works at a 30 MHz clock cycle and can store 128 patterns per chip. Now the FTK utilizes the AMChip06 [4] which works at 100 MHz clock cycle and can store 128k patterns per chip. The initial SVT holds 256 VLSI chips thus it can hold 32k patterns in total. On the other hand the FTK

uses 8,192 chips thus it can store more than 1G patterns in total. The development of the AM chip is summarized in Table 1.

Chip	Technology	#Patterns/chip	#Chips	Clock (MHz)	I/O	Purpose
VLSI	700 nm	128	256	30	parallel bus	CDF SVT (1992)
AMChip03	180 nm	5k	100	50	parallel bus	CDF SVT (2003)
AMChip04	65 nm	8k		100	parallel bus	FTK R&D
AMChip06	65 nm	128k	8192	100	serdes	FTK

Table 1: The improvement of AM chip.

2.2 Track Fitting

The FTK performs track fitting rapidly by implementing a linear approximation of the local hit position with full resolution of each detector layer instead of performing a helical fit. Five track parameters and χ^2 components are estimated by this linear approximation. The linear approximation is expressed by a set of scalar products of hit coordinates and pre-calculated fit constants that take geometry and alignment of the detector into account. The equation is expressed as following.

$$\widetilde{p_i} = \sum_{l=1}^{N} C_{il} x_l + q_i, \tag{2.1}$$

where C_{il} and q_i are pre-calculated constants defined for each track candidate and x_l are N hit coordinates. i corresponds to five track parameters and runs from 1 to 5. χ^2 is the sum of the squares of those functions:

$$\chi^2 = \sum_{i=1}^{6} \Big(\sum_{j=1}^{11} S_{ij} x_j + h_i \Big)^2, \tag{2.2}$$

where S_{ij} and h_i are pre-calculated constants. When the hit coordinates are given, track parameters and χ^2 are calculated immediately. Resolution of the track parameters obtained by this method is almost the same as the helical fit if the region which each pre-calculated fit constant covers is enough small.

3. Installation and Commissioning

In 2016, a part of the FTK was installed which can cope with a small region of the detector. Further board production and installation are ongoing. Boards are installed when they are produced and get ready.

At the commissioning in the real environment of high input rate, to establish stable data flow is a major challenge. The goal is to establish stable processing for the entire FTK system for all the events without any delay and loss of data. The difficulty is to cope with many kinds of input data patterns as well as to perform event synchronization among channels to reconstruct track

information for the entire event. The data is received at different timing from each fiber and the data size in an event is also different. This can be improved by increasing the processing speed by implementing efficient processing algorithm.

At the end of 2016, it was succeeded to build dataflow throughout a slice of the FTK system and to send the data to the ATLAS Readout System. Toward the start of the real operation, there are several issues to be resolved. One of the major issues is the dataflow stability of the entire system with high parallelization. Flow control and event synchronization among many combination of electric boards should be improved.

4. Conclusion

The FTK is a newly installed hardware system which reconstructs tracks at the early stage of the ATLAS trigger system. The HLT obtains track information of the entire event as well as additional processing time since it is not necessary to calculate track information. Thus more sophisticated algorithms such as more precise object ID and vertex reconstruction for the entire event can be implemented at the HLT. The FTK enables fast tracking by pattern matching and linear approximation algorithms with high parallelization. Installation and commissioning are ongoing. First output with a slice of the FTK was achieved at the end of 2016. The FTK will start operation at the end of 2017 or in 2018, and will be upgraded after 2018 to cope with higher luminosity.

References

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