Integration of the CMS Phase 1 Pixel Detector

Andreas Kornmayer[*][†]

European Organization for Nuclear Research (CERN)

E-mail: andreas.kornmayer@cern.ch

During the extended year-end technical stop 2016/17 the CMS Pixel Detector has been replaced. The new Phase 1 Pixel Detector is designed for a luminosity that could exceed L = $2x10^{34}cm^{-2}s^{-1}$. With one additional layer in the barrel and the forward region of the new detector, combined with the higher hit rates as the LHC luminosity increases, these conditions called for an upgrade of the data acquisition system, which was realised based on the μTCA standard. This contribution focuses on the experiences with integration of the new detector readout and control system and reports on the operational performance of the CMS Pixel detector.

---

[*]Speaker.

[†]On behalf on the CMS collaboration

1. Introduction

The Compact Muon Solenoid (CMS) experiment is one of the experiments hosted at the Large Hadron Collider of CERN, Switzerland. The experiment is built in layers around the interaction point where protons or heavy-ions are brought to collision. At the innermost part of the CMS experiment is a pixelated tracking detector engulfed in a 3.8 T strong magnetic field [1]. During an extended year-end technical stop (EYETS) in 2016/17 the original CMS Pixel detector was removed and replaced by a new and improved detector. This new detector, commonly referred to as the Phase 1 Pixel Detector, is built from four layers in its barrel shaped part (BPIX) and three disks at each end of CMS in the forward region (FPIX). The detector is based on the hybrid pixel technology with n-in-n silicon sensors of 285 µm thickness bump bonded to the front-end readout chips (ROCs). Like in its predecessor each pixel has an active area of 150 µm×100 µm but the total number of pixels increased to over 120M in the full detector. The detector is cooled by a two-phase evaporative CO_2 cooling system that doubles as support structure for the pixel modules greatly reducing the amount of non-sensitive material in the detector volume. In order to improve the performance of the new pixel detector the front-end chips and the back-end electronics were upgraded. The two different strategies of evolutionary upgrade and general overhaul will be shown in the following on the examples of the front-end readout chips and the data acquisition system (DAQ).

2. Upgrade Strategies for the Phase 1 Pixel Detector

Two orthogonal strategies were applied during the design phase of the upgrade Pixel detector. The first was to only make improvements were they were needed to match the new system component to the heightened requirements the LHC posed while keeping all other elements untouched. The second strategy was to completely re-imagine the component from scratch using new technologies and design ideas. These two strategies can be best seen in the development of the two front-end readout chips, the PSI46dig and the PROC600, and the DAQ system.

2.1 Front-End Readout Chip Upgrade

For the layers two to four in the barrel and all disks in the forward region the PSI46dig was designed. It is an evolutionary upgrade from the ROC used in the original CMS Pixel detector. This means the changes made to the design were kept to a minimum while still meeting the requirements of an improved hit detection efficiency and higher data output bandwidth. While the double column draining logic from the PSI46dig's predecessor remained untouched, the hit rate capability was improved to sustain 120 MHz/cm^2 by deepening data and timestamp buffers [2]. The data output was switched from a six-level analogue based format transmitted on a 25 MHz clock to a digital 160 MBit scheme. The minimalistic approach made it simple for these changes to be implemented and within the CMS Pixel detector a community of experts already existed to start validation and module production once the ROC was produced.

A different approach was taken for the readout chip for the first layer of the barrel region. In order to cope with the intense particle rates of up to 600 MHz/cm^2 a new readout architecture was implemented in the PROC600 chip [3]. In this completely overhauled ASIC chip pixel hits are

1

collected in a 2x2 pixel cluster draining mechanism drastically reducing the hit detection ineffi-
ciencies compared to the PSI46dig. While giving the designers more freedom in their choices for
the system this approach also came at the risk of having a nonfunctional or not optimal functioning
detector layer due to fixed time constrains on the installation date.

Both presented ROCs were tested to work as expected, used for the production of the new
CMS Phase 1 Pixel detector and successfully operated in the experiment.

2.2 Data Acquisition System Upgrade

The change from analogue to digital readout of the detector front-end made it necessary to also
upgrade the back-end readout and control system of the DAQ. Up to eight ROCs transmit a binary
serial data stream clocked at a speed of 160 MHz. Two of these data streams are multiplexed by
the Token Bit Manager (TBM) to a 320 Mbps stream. An additional 4B/5B encoding is applied to
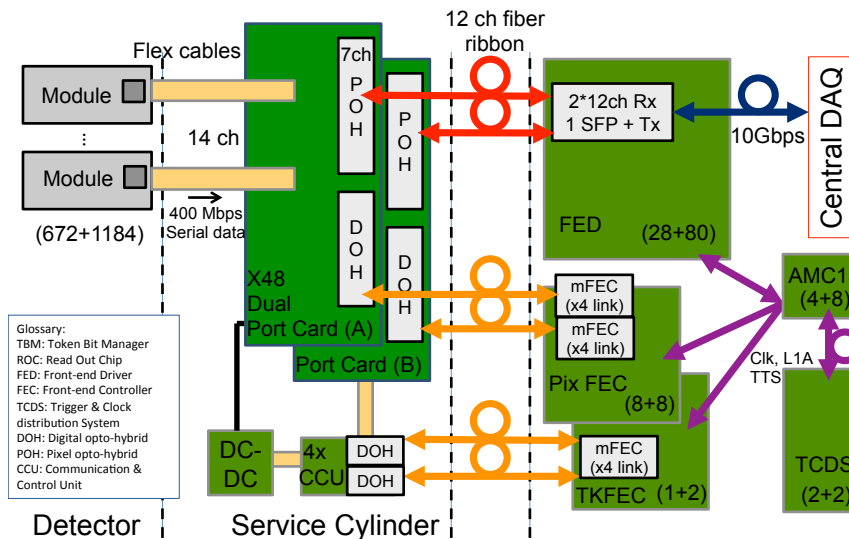balance the data link resulting in a 400 Mbps serial data stream coming from each TBM.

Figure 1: The readout architecture for the new DAQ system for the CMS Phase 1 pixel detector.

A new DAQ system was designed, produced, tested and installed in order to control the front-
end detector and decode the event data it is sending back. In figure 1 the full readout architecture
is shown. For this part of the detector the full overhaul strategy was also chosen since the back-
end readout hardware of the original detector was outdated and difficult to upgrade. In order to
mitigate the risk of failure to finish the DAQ system on time for detector installation, detector
commissioning and first data some adjustments regarding the utilised hardware were made. The
new detector back-end relies on industrial standard components or hardware that is already used by
other sub-systems in the CMS experiment. Only when necessary custom hardware was built. The
CMS Pixel Phase 1 DAQ back-end is based on the μTCA standard [4] that describes a modular
platform to host Advanced Mezzanine Cards (AMCs) directly on a backplane, making it compact
and affordable yet providing high data throughput and redundancy. The AMC used in the system

is the FC7 cards [5] a full size, double width AMC that has become a commonly used card in the CMS experiment. The card is equipped with a Kintex 7 FPGA, 4Gb of DDR3 RAM for data buffering and twelve 10 Gbps high speed links to the crate back plane.

The FC7 cards are the base building blocks for the Front-End Controllers (PixFECs and Tk-FECs), responsible for sending slow-control signals and fast control signals to the detector, and the Front-End Drivers (FEDs) that decode the data coming from the front-end and create events that are sent to Central DAQ system of CMS. The purpose of the card is decided by the custom build FPGA Mezzanine Cards (FMCs) placed on the AMC and the corresponding firmware flashed to the FPGA [6]. The FED FMC is equipped with two optical receivers with twelve input channels each, optimised for a wave length of 1310 nm and compatible with the 400 Mbps serial data stream. In addition a 10 Gbps optical Ethernet SPF+ link can be placed on the card over which event data is transferred to the CMS Central DAQ system. The FEC FMC, PixFEC and TkFEC using the same hardware, hosts up to eight low-speed optical transceivers sending configuration, control and timing commands to the detector front-end.

An additional AMC, the AMC13 card, is placed in each of the crates hosting the FEDs and FECs. This AMC13 is responsible for connecting the crate to the Timing and Control Distribution System (TCDS) [7] of the CMS experiment.
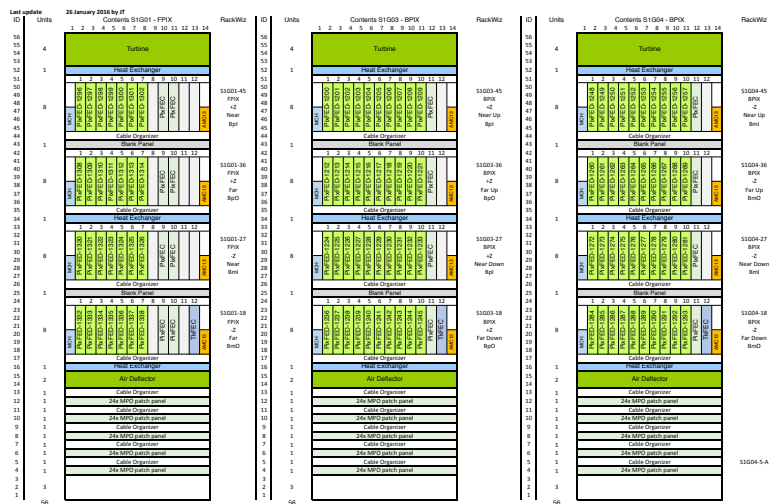

Figure 2: The layout of the final DAQ backend readout system in the CMS service cavern.

The Pixel Phase 1 DAQ system is placed in twelve μTCA crates distributed over 3 racks. One rack holds four crates with the system components for FPIX, while the BPIX parts are held in the other two racks. The FPIX crates are equipped with seven FEDs and two PixFECs each while ten FEDs and a single PixFEC are placed in each BPIX crate. Only one TkFEC per rack is necessary. The rack and crate layout including AMC13 cards, μTCA Carrier Hubs (MCHs) and optical patch panels is shown in Figure 2

2.3 FED and FEC Firmware

With the re-design if the backend electronics hardware also the firmware had to be re-done. The PixFEC and TkFEC were the less critical projects with the old VME based system as an fully

compatible fallback option. The main goal for this part of the detector upgrade was to have all functionality from the old system at installation time and later expand on it and make use of the additional resources provided by the FC7 hardware.

The Phase-1 Pixel FEC is responsible for distributing clock, trigger and fast signals to the detector front-end and for programming the DAC registers of the ROC and TBM chips on the detector modules. These commands are sent via a non-redundant optical control link. Each link in separated in a clock and a data line. The clock line carries the clock signal and encodes all trigger and fast commands while the data line is used for programming of the front-end. For the future it is planned to implement additional features to the PixelFEC firmware such as making use of the DDR3 memory to store detector configurations and FEC-to-FED communication within a crate.

The TkFEC firmware followed the same development approach as PixFEC, all features of the old system were implemented in the new one. The TkFEC has redundant optical links that carry clock and data signals to the connected CCU chips in order to control the auxiliary electronics of the CMS Pixel Detector.

The firmware for the pixel FED was developed in two separated blocks that were later joined. With no fallback options available the FED firmware was one of the focal points of the CMS Pixel Phase 1 Upgrade. The front-end part of the FED firmware is responsible for de-serialising and decoding of the incoming data stream. In order to do so it automatically finds the best sampling point in the 400 Mbps data stream and continuously adjusts its relative phase. The firmware part then decodes the 4b/5b encoded signal and splits the two multiplexed TBM data streams on each of the 24 optical input links creating 48 readout channels. Within the data stream the front-end part detects special markers for TBM HEADER, TBM TRAILER, ROC HEADER and pixel data. The front-end connects via a 36 bit interface to the backend part of the firmware.

The backend part is designed to handle the data from 48 readout channels. Decoded data provided by the front-end part of the firmware is stored in 48 individual buffers that are sequentially drained upon the FED receiving a L1A trigger signal over the TTC link from the AMC13. The FED firmware is fully compliant with the TCDS system via the TTC/TTS interface in order to keep synchronisation between FEDs and FED channels. The FED congregates data from all 48 channels and encapsulates the event data in a SLINK packet that is sent over a 10 Gbps Ethernet connection to the CMS Central DAQ. In case of erroneous data arriving at the FED, such as event number mismatches or missing trailers, the FED has automatic recovery mechanisms. The FED can raise a BUSY flag over the TTS system blocking L1A triggers momentarily for all of CMS. Additionally the FED keeps count of a set of possible errors in the data coming from the detector front-end, FED channels that are repeated offenders can be blocked from readout in the FED. The error numbers are read out in software as well and can trigger the front-end being reprogrammed or a pixel module being disabled entirely. With the FED firmware fully functional at installation and commissioning time of the Phase 1 CMS Pixel detector it is planned to improve the FED firmware data throughput in future firmware releases by parallelising the draining of the FED channel data FIFOs in several cascading groups.

3. Detector Performance

The zero-suppressed data from the front-end modules is transferred via 2368 optical fibres

to the DAQ system. The average number of hits each module sees decreases with its radial and longitudinal distance from the interaction point. In figure 3a the average number of pixel hits per event is shown for all fibres. For the outer layers in the barrel region and the outer rings in the forward region the distribution is uniform, while for the inner most layer the average number of received hits per event has a large spread. Fibres from different layers and z-coordinates have been bundled in groups of twelve in order to balance the data processing load on the FEDs. Most FEDs take two of these fibre bundles as inputs. The distribution of average hits per fibre bundle and per FED can be seen in figure 3b. It shows that the data load is distributed equally across the fibre bundles and thus also across the FEDs, with the FPIX FEDs (FED number >100) receiving slightly higher data rates on average than the BPIX FEDs (FED number <100).

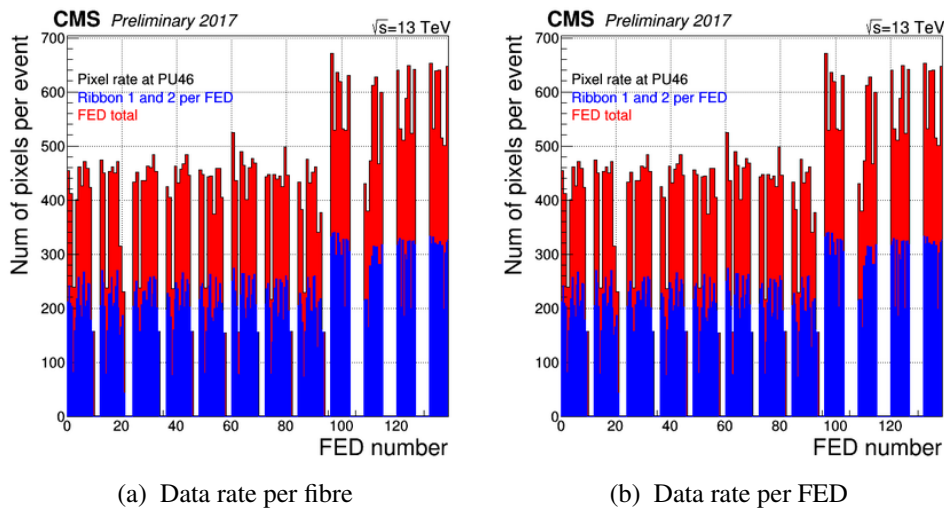(a) Data rate per fibre   (b) Data rate per FED

Figure 3: DAQ system performance plots

A main reason for the replacement of the original CMS Pixel detector with the detector described in this text was the diminishing hit detection performance with the continuos increase of delivered instantaneous luminosity of the LHC accelerator. So, one of the most important performance benchmarks for the new pixel detector is the hit efficiency, the probability to find a cluster within a 1 mm area around the expected hit from a track reconstructed in all other layers of the CMS Tracker and a transverse momentum of $p_T > 1.0\,\text{GeV}$. As shown in figure 4 the hit efficiency for layers two to four of BPIX and all FPIX disks equipped with the PSI46dig front-end readout chip is well above 99% for a large range of instantaneous luminosity. Layer 1 of BPIX equipped with the PROC600 front-end ASIC shows an average efficiency of 99% with a drop at high instantaneous luminosity. Considering the fact that the particle rate is up to a factor 5 higher in this layer this performance is still to be considered excellent.

4. Summary and Outlook

During the EYETS 2016/17 the CMS Pixel detector was replaced and upgraded successfully. Two orthogonal upgrade strategies were followed on different parts of the detector. The front-end readout chips for the outer layers underwent an evolutionary upgrade guaranteeing a consistently
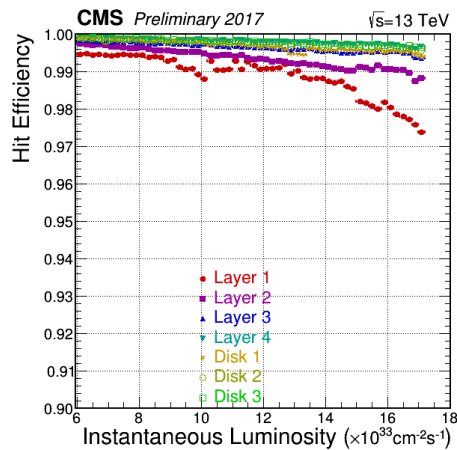
Figure 4: Hit Efficiency as a function of instantaneous luminosity for different layers of the Barrel Pixel detector and the Forward Pixel detector

high hit efficiency.. The fully new developed front-end ASIC for the innermost layer also performs good with low inefficiencies.

The upgrade strategy for the new back-end DAQ system was to rely on existing parts and only build custom hardware when necessary. This made it possible to create a full readout system on a tight schedule and no backup solution. The DAQ system was installed on time, fully functional and tested for infant mortality of components to ensure stable operations for detector commissioning and operations.

The upgrade CMS Pixel detector has been shown to work very well with its front-end and back-end electronics perfectly integrated into the CMS experiment.

References

[1] The CMS Collaboration, CMS *Physics: Technical Design Report Volume 1: Detector Performance and Software*, CERN-LHCC-2006-001.

[2] D. Hits, A. Starodumov, *The CMS Pixel Readout Chip for the Phase 1 Upgrade*, Journal of Instrumentation, vol. 10, no. 05, p. C05029, 2015.

[3] A. Starodumov, P. Berger and M. Meinhard *High rate capability and radiation tolerance of the new CMS pixel detector readout chip PROC600*, 2017 JINST 12 C01078

[4] V. Bobillier, S. Haas,1 M. Joos, J. Mendez, S. Mico and F. Vasey, *MicroTCA and AdvancedTCA equipment evaluation and developments for LHC experiments*, 2016 JINST 11 C02022

[5] M. Pesaresi, M. B. Marin, G. Hall, M. Hansen, G. Iles, A. Rose, F. Vasey, and P. Vichoudis, *The FC7 AMC for generic DAQ & control applications in CMS*, 2015 JINST 10 C03036.

[6] B. Akgün, *Integration and testing of the DAQ system for the CMS Phase 1 pixel upgrade*, 2017 JINST 12 C02078

[7] J. Hegeman et al., *The CMS timing and control distribution system*, IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC) (2015) 1