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Radiation Hardness Studies and Evaluation of SRAM-Based FPGAs for High Energy Physics Experiments

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SRAM Field Programmable Gate Arrays (FPGAs) are beginning to be considered as viable solutions for particle physics experiments and as well as for space applications. This paper summarise some of the radiation hardness measurements done on the KINTEX-7 FPGA by our group using different particle beams like: protons, X-Rays and ion beams. For multiple values of the total ionizing dose, linear energy transfer and proton energy, the cross sections of single-event-effects are estimated. We also give separate results for specific resources like: configuration RAM, block RAM, I/O banks. Preliminary conclusions are reached for this device regarding its radiation tolerance in LHCb-Upgrade case.

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1. Introduction

The reconfigurable logic devices, especially the Field Programmable Gate Arrays (FPGAs), represent viable solutions as replacement for application specific integrated circuits (ASICs) in safety-critical applications or harsh environments with radiation background (e.g. space applications, high energy physics experiments). Because of their lower price, low non-recurring engineering costs (NRE), high logic density and of course, in-flight reconfigurability, the commercial of the shelf SRAM-based FPGAs are the devices with the greatest potential for such applications [1]. The main concern for SRAM-based FPGAs operating in radiation environments are the single event effects (SEE) like upsets (SEUs) or latch-ups (SEL), the former usually occurring in the configuration memory (CRAM), which leads to user logic failures if not properly mitigated.

This paper will describe the device under test (DUT), the irradiation and testing procedures. Also some of the measurements during irradiation with different particle species are highlighted and preliminary conclusions about DUT's radiation hardness are presented.

2. Device Under Test and Tests Description

The smallest device from KINTEX-7 family, XC7K70T, has been chosen for use in the digital read-out systems of the upgraded LHCb RICH sub-detectors [2], hence an irradiation campaign was foreseen in order to establish its tolerance to ionizing radiation. This device has the following main features: 65.6 k of logic cells, 240 DSP slices, 4.86 Mb of Block RAM (BRAM), 8 GTX [3] transceivers, 300 I/O pins and 18884576 bits of configuration memory (CRAM) [4].

For testing, a custom board was designed with minimal components, allowing the device to run in JTAG mode, without any external flash configuration memory. In addition to the testing board, a custom DAQ system controlled by a LabVIEW based graphical user interface (GUI) was designed in order to monitor the electrical parameters and logic configuration of the device [5].

Several configuration files have been designed, to allow testing specific FPGA resources like: Flip-Flops, CRAM, BRAM and I/O banks. SEU mitigation techniques were implemented with several triple modular redundancy (TMR) architectures for logic, and the Soft Error Mitigation (SEM) controller [6] was used for CRAM SEU mitigation.

We have performed several beam tests both with ions and protons using different facilities: ions at SIRAD facility from Legnaro National Laboratories in Italy, ions at Heavy Ion Facility (HIF) from Universite Catholique de Louvain (UCL) in Belgium, 200 MeV protons at Proton Irradiation Facility (PIF) from Paul Scherrer Institute in Switzerland and 35 MeV protons at COSY/JULIC facility from Juelich Research Center in Germany. Another irradiation was done using 10-50 keV X-Ray photons courtesy of Padova University.

In this paper we will summarize the beam test results with ions done at UCL and with protons pursued at Juelich Research Center.

3. Beam Test Results

3.1 Heavy ions beam

During our tests the Heavy Ion Facility from UCL provided different beams of ions with a broad range of linear energy transfer (LET) from 1.3 to 32.4 MeV·cm^2/mg. We had the following ions: ^{13}C at 131 MeV (LET=1.3 MeV·cm^2/mg), ^{22}Ne at 238 MeV (LET=3.3 MeV·cm^2/mg), ^{40}Ar at 379 MeV (LET=10 MeV·cm^2/mg) where DUT was also tilled at 0°, 30° and 50°, ^{58}Ni at 582 MeV (LET=20.4 MeV·cm^2/mg), ^{83}Kr at 769 MeV (LET=32.4 MeV·cm^2/mg). Because of FPGA design, which is implemented in flip-chip technology, the thermal interface material and substrate on the top side of the device was thinned from 250 to about 60 µm in order to allow the ions to penetrate to the active layer.

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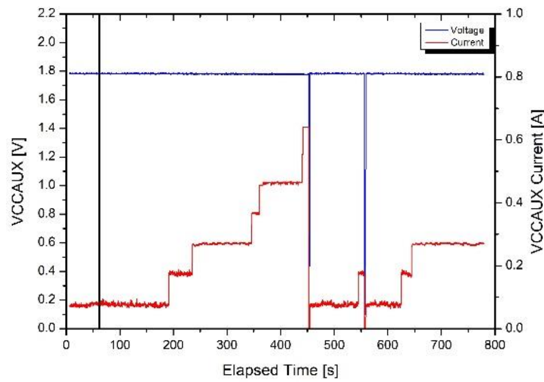

Figure 1. Current steps in VCCAUX rail when irradiated with ^{40}Ar beam with DUT tilled at 50°

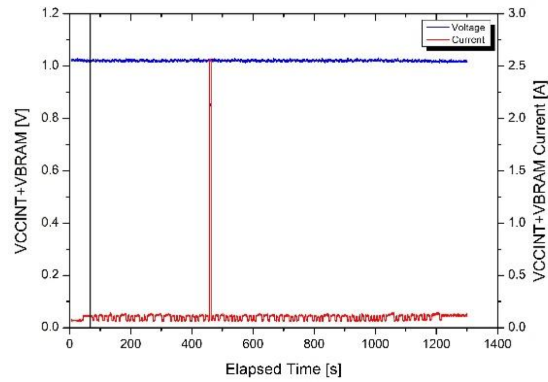

Figure 2. High current states in VCCINT rail induced by SEU which is mitigated within seconds, DUT irradiated with ^{40}Ar beam with DUT tilled at 50°

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During beam tests, large SEU rates have been seen in CRAM even at low LET values, hence the threshold is below 1.3 MeV·cm^2/mg, and by increasing the LET the SEU rate increased for both CRAM and Flip-Flops logic configuration.

However, when exposed to ^{40}Ar beam with DUT tilled at 50°, the effective LET become 15.57 MeV·cm^2/mg, and 100 mA current jumps were observed in the VCCAUX rail, see figure 1. Since, they did not recover during reconfiguration attempts but only after power cycle, these current jumps are the effect of single-event latchups (SEL). In fact, we found the threshold for SEL around 15.57 MeV·cm^2/mg, which is consistent with other tests carried on this device family and described by the literature [7]. Such events are called in the literature micro-latchups and they seem to be caused by an irradiation effect in the circuitry associated with a type of programmable I/O banks, the High Range (HR) I/O banks, for LET values < 40 MeV·cm^2/mg [8].

High current states were observed in VCCINT rail at the same LET, but were recovered by a full reconfiguration of the DUT, see figure 2. Such events are referred to in literature as “Scrub SEFIs”, because they are due to writing multiple frames into the wrong memory location when a scrubber is used. Hence they are triggered either by a SEU in the Frame Address Register (FAR) or by a single event transient (SET) on the clock line connected to the boundary scan registers used to feed the configuration SRAM cells. [9]

The obtained results for CRAM SEU cross-sections values, retrieved from the SEM IP Core report, are: $0.47 \cdot 10^{-10}$ at 1.3 MeV·cm^2/mg and $0.26 \cdot 10^{-8}$ at 32.4 MeV·cm^2/mg.

3.2 Protons beam

Using the JULIC cyclotron from COSY facility, we have irradiated the DUTs with 35 MeV protons with a LET of 0.0132 MeV·cm^2/mg (Si) which we used to test several resources like: Flip-Flops, CRAM, BRAM and I/O banks. Three samples were irradiated, one up to 500 krad (Si) total ionizing dose (TID) and the others two up to 250 krad (Si).

The SEU cross-section for CRAM was determined by analyzing the SEM IP Core reports during and after beam exposure. It was determined to be $4.9 \cdot 10^{-15}$ cm^2/bit. Also, the BRAM cross-section was determined to be $6.9 \cdot 10^{-15}$ cm^2/bit. Both values are consistent with the ones determined by other groups and published in literature [10,11].

The logic failure rates were measured using several architectures which consist of single FFs (Flip-Flops) chain and three types of TMR logic configurations: basic TMR with 3 single chains and a single voter, partitioned TMR with a voter after each Flip-Flop trio and an extended TMR which is a combination of first 2 logics [12]. The voter for each TMR architecture is based on LUT (Look-Up Table). Using these firmware configurations an external 32-bit serial-data stream was injected in each of these chains then shifted outside this DUT. Next, the output is compared

with the input. The first configuration, see table 1, since is not triplicated has the lowest number of essential bits [13].

Detailed in table 1, the second configuration has an extended TMR configuration and 3 times increase in number of FFs with similar increase in number of essential bits. The measured cross-sections are given per device in the table 1 with specified number of configured FFs and LUTs.

TABLE 1 KINTEX-7 LOGIC ELEMENTS CROSS-SECTIONS

Configuration	Logic Elements [FFs + LUTs]	Essential bits	Cross-section [cm^2/device]	Proton Fluence [cm^{-2}]
FF chain	5500+0	300700 (1.59%)	$27.5{\cdot}10^{-11}$	$2.4{\cdot}10^{11}$
Extended TMR	16744+6073	1092465 (5.78 %)	$20.8{\cdot}10^{-11}$	$2.4{\cdot}10^{11}$

In order to test the FPGA's I/Os, we implemented 4 ring oscillators using I/O buffers primitives within all 5 I/O banks of the FPGA. Each oscillator has its fixed oscillation frequency which ranges from 1 MHz to 11 MHz and is strongly dependent of the I/O buffers number. About 71% of I/O resources were used and the essential bits employed by this configuration are a small fraction from total CRAM, only 36688 (0.19 %) essential bits. The simplified firmware architecture is presented in figures 3 and the typical waveforms for these ring oscillators are shown in figure 4.

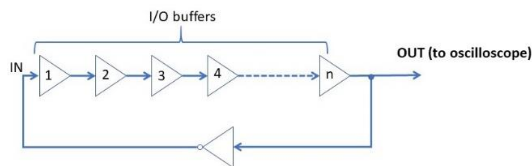

Figure 3. Simplified ring oscillator architecture for one I/O Bank

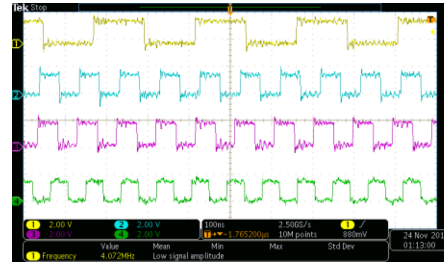

Figure 4. Typical waveform of all 4 I/O ring oscillators

During irradiation, we measured different types of effects: changes in oscillation frequency or the complete disappearance of the oscillating signal. The oscillation frequency varied most of the time with ± 200 KHz from its baseline value, and this study is currently ongoing, hence in table 2 are considered only the events when the signal is disappearing during one run.

TABLE 2 I/O Banks results during one run, proton fluence $1.8{\cdot}10^{11}$ [cm^{-2}]

I/O BANK	Type	Nr. of I/O buffers used	Frequency[MHz]	Nr. of Events
BANK 13	HR	49	1.7	3
BANK 15 & 16	HR	82	4.2	0
BANK 33	HP	49	4.2	2
BANK 34	HP	18	11.4	0

3.3 X-rays beam

Only two of the samples were exposed to an X-ray beam up 150 krad (Si) TID for each device which was delivered in 3 steps of 5 minutes. During irradiation, we tested several resources like: CRAM, Flip-Flops and I/O banks. No significant cumulative effects have been seen, neither SEUs in CRAM/FFs.

4. Conclusions

The KINTEX-7 FPGA behavior under irradiation has been intensively studied and a lot of data have been collected during beam tests.

Its radiation tolerance is still under investigation. However, we saw that the threshold for CRAM SEUs is below 1.3 MeV·cm^2/mg while for SELs is 15.57 MeV·cm^2/mg. DUT survived at

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higher TID, we delivered up to 1 Mrad (Si) total dose for one sample during the entire irradiation campaign.

The TMR configuration doesn't improve too much the SEU mitigation during irradiation, hence applications with an expected TID of hundreds of krad and 10^{12} HEH (High Energy Hadrons) fluences will have problems with large SEE rate, especially for experiments which use hundreds or thousands of FPGAs. In these cases, the change in reconstruction efficiencies could degrade with even few percent during a single run. These extrapolations would be made explicit in another paper of our Bucharest based group.

5. Acknowledgments

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