PROCEEDINGS OF SCIENCE

New slow-control FPGA IP for GBT based system and status update of the GBT-FPGA project

Julian Mendez[1]
CERN
Geneva CH-1211, Switzerland
E-mail: julian.mendez@cern.ch

Sophie Baron[a], **Pedro Vicente Leitao**[b]
CERN
Geneva CH-1211, Switzerland
E-mail: [a]sophie.baron@cern.ch, [b]pedro.leitao@cern.ch

Alessandro Caratelli
Microelectronic System Laboratory (LSM), École polytechnique fédérale de Lausanne (EPFL)
Lausanne, Switzerland
E-mail: alessandro.caratelli@cern.ch

The GBT-FPGA, part of the GBT (GigaBit Transceiver) project framework, is a VHDL-based core designed to offer a back-end counterpart to the GBTx ASIC, a radiation tolerant 4.8 Gb/s optical transceiver. The GBT-SCA (Slow Control Adapter) radiation tolerant ASIC is also part of the GBT chipset and is used for the slow control in the High Energy Physics experiments. In this context, a new VHDL core named GBT-SC has been designed and released to handle the slow control fields hosted in the serial GBT frame for the GBTx and GBT-SCA. This paper presents the architecture and performance of this new GBT-SC module as well as an outline of recent GBT-FPGA core releases and future plans.

Topical Workshop on Electronics for Particle Physics
11 - 14 September 2017
Santa Cruz, California

[1]Speaker

PoS(TWEPP-17)083

1. Context

The GBT-FPGA IP-core [1] was developed in the GBT framework project [2] to provide a common and centrally supported VHDL core. It belongs to the GBT system presented in Figure 1, which is divided into two parts: the radiation tolerant ASICs, located close to the detector, and the backend-modules implemented in FPGAs (Field Programmable Gate-Arrays). The GBT-FPGA core offers a back-end counterpart to the GBTx, compatible with the GBT frame definition (cf. figure 2) and provides a 4.8Gbps high-speed serial link. As shown in Figure 1, it is used for the timing and trigger distribution (TTC), the data acquisition (DAQ) and the slow control of the On-Detector electronics (SC).

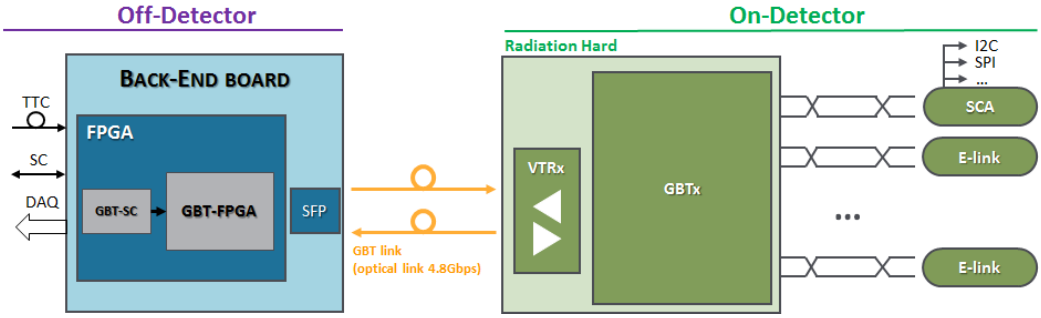

Figure 1: GBT system architecture

The GBT-FPGA project is constantly evolving and the new GBT-SC core has been designed to provide the GBT community with a common way to perform slow control actions. Its principle and performance are described in section 2. In addition, a new optimization of the GBT-FPGA core, used as a proof of concept, has been evaluated and is presented in section 3.

2. Slow control (Internal and External control)

The GBT system defines two types of slow control: the internal control (IC) that allows configuring the GBTx ASIC using the incoming data from the high speed link, and the external control (EC). The latter provides control and monitoring of front-end ASICs over different communication protocol channels (GPIOs, I2Cs, SPIs, JTAG, etc.), all through the GBTx and GBT-SCA [3] chain, as depicted in figure 1.

IC and EC communication is based on HDLC frames sliced in 2-bit packets which are serialized in the 84bits of the GBT frame as described on figure 2. Therefore, the bandwidth dedicated to the slow control is 80Mbps per component. One single GBT link can therefore handle the control of one GBTx (IC) and of one to 41 SCAs (EC) using the frame structure shown in figure 2. Custom fields (dark blue) are used to select the channel and to specify the command to be executed.

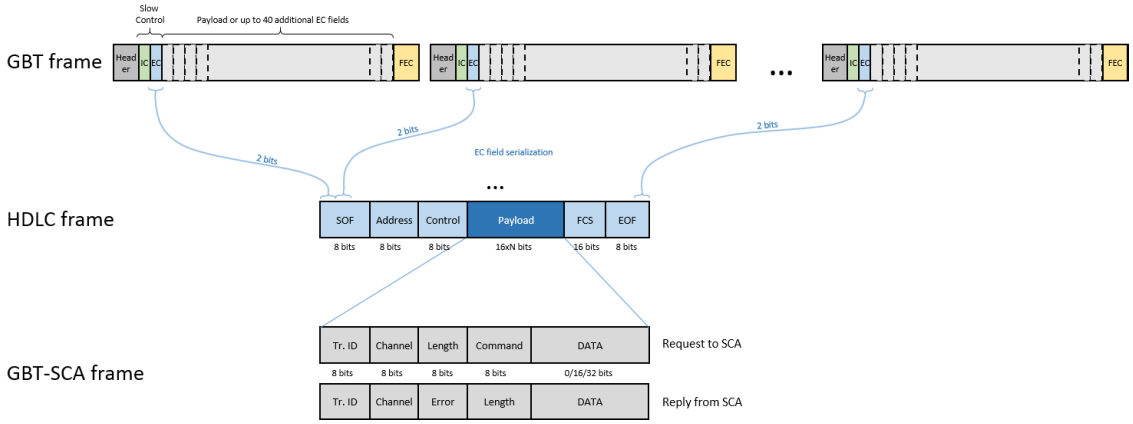

Figure 2: Mapping of the HDLC frame to SCA into the GBT frame

The GBT-SC core has been designed to perform the transmission encoding/serialization and the reception deserialization/decoding of the IC and EC fields and therefore to complement the GBT-FPGA IP.

2.1 GBT-SC IP architecture

The generic GBT-SC core was designed in VHDL to generate the serial stream for both IC and EC types of slow control. However, the module is internally divided into two parts: the SCA-EC IP, which can be multiplied to control up to 41 SCAs, and the GBT-IC IP that is unique for each GBT link.

Figure 3 shows the architecture of the SCA-EC module. In this architecture, the Tx state machine is responsible for the EC frame encoding: generation of the start and the end of frame, encapsulation of the command data, zero insertion as defined by the HDLC standard and CRC computing. An additional bit is available for each SCA link in order to enable/disable the transmission path. On the receiving side, the IP receives the stream from the ASIC and takes care of its deserialization and decoding. The decoded words are saved into a FIFO and finally made available as output registers.

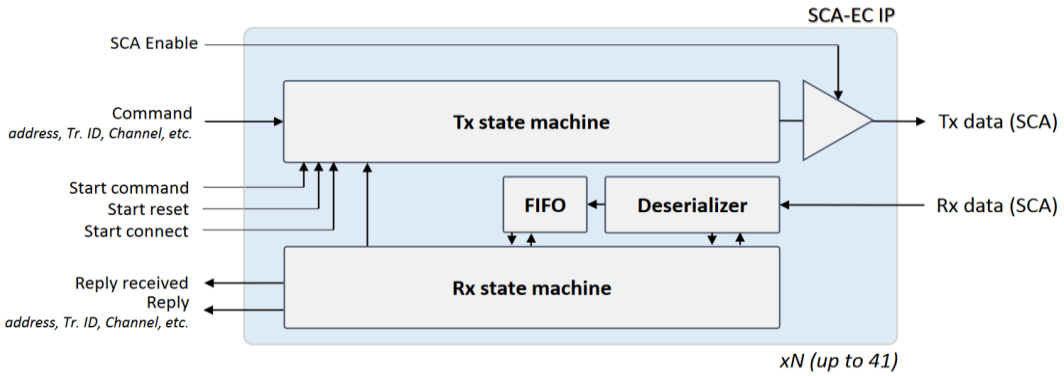

Figure 3: SCA-EC IP architecture

This architecture has the advantage of being light in terms of logic resources in the FPGA, as only the lower layer of the communication protocol is firmware based: all of the commands must be sent one after the other using an external link (e.g: PCIe, Ethernet, etc.). This severely impacts software efficiency though, in particular when many transactions are required to send only a few bytes via the channel interface. It is especially true for protocols like JTAG where up to 13 instructions must be sent to the GBT-SCA to transmit only 128bits to the front-end chip. For this reason, external acceleration modules were designed to improve the global efficiency. These modules are optional: implementing them or not is a trade-off between timing performance and use of resources. The Figure 4 shows the architecture of the GBT-SC IP featuring these acceleration modules.

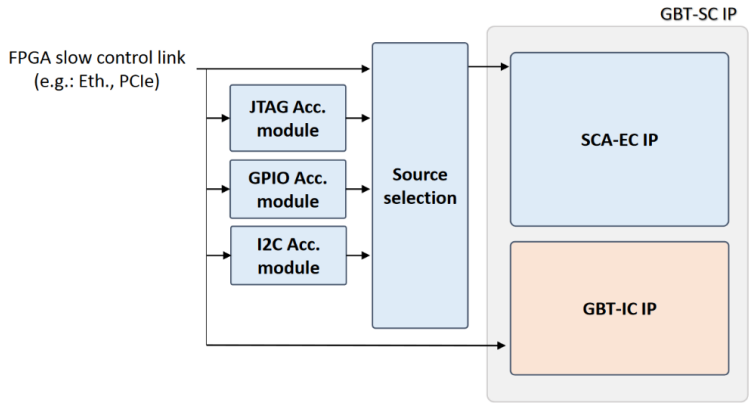

Figure 4: GBT-SC IP system architecture

2.2 Performance (resource and timing)

The system was tested using the MiniDAQ 1 setup from LHCb. It is made of a custom electronic card (AMC40) hosting a Stratix V FPGA implemented to support the GBT-FPGA IP. Additionally, the FPGA can be accessed via a PCIe link (2.5Gbps) coming from a COM Express module located on the test-pad board (AMC-TP). Figure 5 shows the complete test setup that additionally includes the Versatile Link Demo Board (VLDB) used to emulate a front-end board.

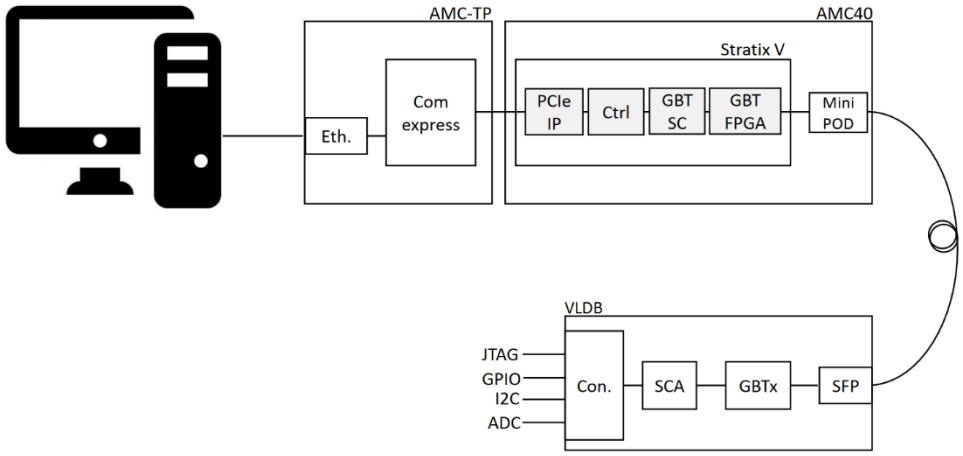

Figure 5: GBT-SC performance measurement setup

The timing performances of all of the channels supported by the SCA have been measured and the impact of the acceleration modules has been evaluated. A gain is systematically observed with a big impact for the JTAG. Figure 6 shows the measurements made for the configuration of different FPGAs with different bitstreams. The programming time is fully proportional with the bitfile size. In order to simplify the test, the measurements were made using a custom implementation of the open source Xilinx Virtual Cable daemon from Xilinx. This solution adds a dead time that can be removed by implementing a JTAG state machine directly into the COM Express module. Nevertheless, the result obtained with this method are already really good and acceptable.

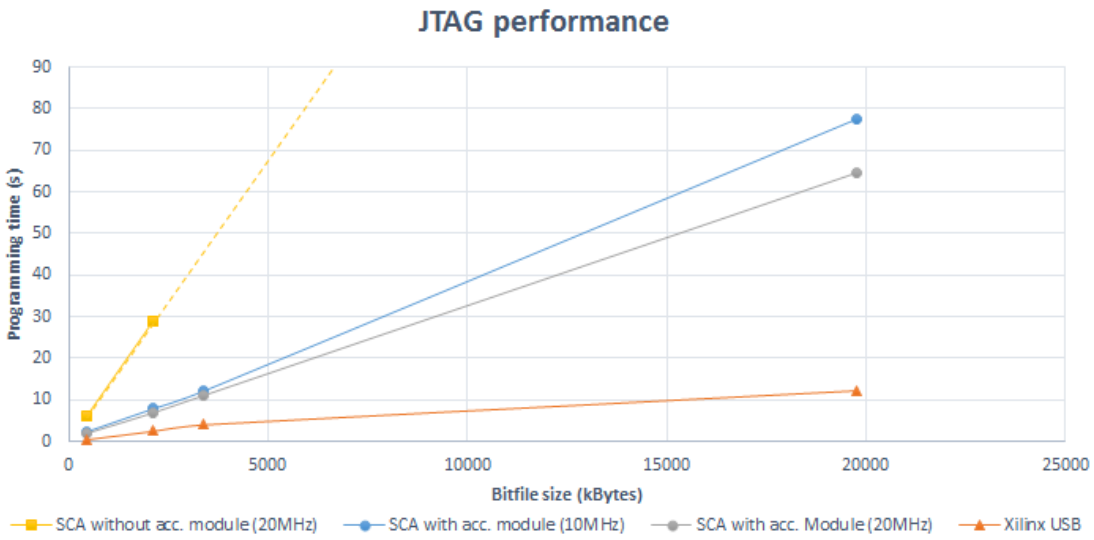

Figure 6: JTAG performance

In terms of resource usage –here given for a Stratix V FPGA- the GBT-FPGA IP core occupies 0.8% per link. A GBT-SC IP (featuring one IC and one EC blocks) represents an

additional 0.3%. Finally, implementing a complementary JTAG acceleration module will require another 0.4%.

3. GBT-FPGA: Clock unification

Currently, the GBT-FPGA IP datapath is clocked on the user side by the LHC bunch crossing clock (BX), at 40.078MHz and internally by the wordclock generated by the transceiver that can be either three or six times the BX frequency depending on the FPGA. This clock domain crossing requires implementing a gearbox with a phase monitoring system. In addition, it decreases the latency performance. For these reasons, the clock domain unification of the GBT-FPGA core was evaluated and implemented as a proof of concept. It consists in removing the gearbox by clocking the full datapath logic with the wordclock. Figure 7 shows measurements made using the KC705 development board from Xilinx, which hosts a Kintex 7 FPGA. After the optimization, the latency has been reduced from 200ns to 182ns without modification of the transceiver frequency (120.2MHz). Going from 120.2MHz to 240.4MHz further reduced this latency down to 105ns. Additionally, the measurement carried out with a climatic chamber and the transceiver configured in loopback mode shows that the latency remains constant with an increase in temperature.

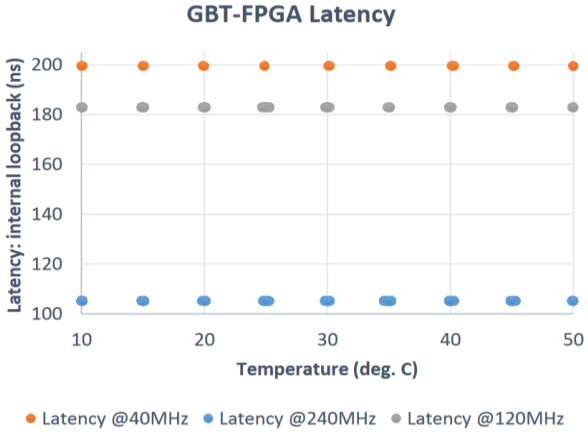

Figure 7: Latency measurement (KC705)

4. Conclusion

The new GBT-SC core designed to handle slow control defined by the GBT system specification has been developed and successfully tested. It showed excellent timing and resource performance. This module is available as a generic VHDL core and can be used with any type of FPGA or with the simulation testbench provided on Gitlab[4]. Additional example designs with the acceleration modules are provided and can be accessed via a dedicated repository.

In parallel, new developments were made for the GBT-FPGA IP in order to validate the concept of clock unification that will be re-used for the upcoming LpGBT-FPGA.

References

[1] CERN EP-ESE-BE, *GBT-FPGA project*, https://espace.cern.ch/GBT-Project/GBT-FPGA/

[2] P. Moreira et al., *The GBT Project*, in proceedings of Topical workshop on electronics for particle physics, TWEPP 2009, Paris, France, 21–25 September 2009, pg. 342

[3] A. Caratelli, S. Bonacini, K. Kloukinas, A. Marchioro, P. Moreira, R. De Oliveira et al., *The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments* JINST 10 C03034.

[4] CERN EP-ESE-BE, *GBT-SC gitlab repository*, https://gitlab.cern.ch/gbtsc-fpga-support/gbt-sc.