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Quality control considerations for the development of the front end hybrid circuits for the CMS Outer Tracker upgrade

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The upgrade of the CMS Outer Tracker for the HL-LHC requires the design of new double-sensor modules. They contain two high-density front end hybrid circuits, equipped with flip-chip ASICs, passives and mechanical structures. First prototype hybrids in a close-to-final form have been ordered from three manufacturers. To qualify these hybrids a test setup was built, which emulates future tracker temperature and humidity conditions, provides temporary interconnection, and implements testing features. The system was automated to minimize the testing time in view of the production phase. Failure modes, deliberately implemented in the produced hybrids, provided feedback on the system's effectiveness.

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1. Introduction

The luminosity increase, planned for LHC Phase 2, results in higher radiation and data rate. A complete replacement of the CMS Outer Tracker is foreseen to cope with these new constraints. The functional building blocks of the future CMS Outer Tracker structure are two types of double-sensor modules. Both types will be produced in different versions that vary in the distance between their sensor planes. Each module contains two high-density front end hybrid circuits. These hybrids host binary readout flip-chip ASICs, which are connected to silicon strip sensors. Additionally, each hybrid is equipped with auxiliary electronic components and mechanical reinforcement structures, which also serve as a cooling interface. In total ten different front end hybrid geometries are foreseen in the design of the future tracker. It is planned to produce as many as thirty thousand pieces [1].

The quality of delivered hybrids must be verified before they are used for module assembly. Testing is crucial in order to ensure a high yield of fully functioning modules during the production phase. Mechanical, electrical and functional test protocols are evolving to address possible failures affecting the hybrid's performance. In the lifetime of the new CMS Outer Tracker, the temperature in the tracking volume will be gradually decreased to below -30°C. A low temperature setup was built to conduct tests in an environment representative of the tracker operating conditions, requiring a specifically designed testing infrastructure. The constructed device cools the hybrid directly via its thermal contacts while protecting it against humidity condensation. A dedicated software was developed to provide an environment control feature integrated with functional test algorithms, both automated to minimize the testing time in view of its usefulness and scalability during the mass-production.

The first prototype front end hybrid variant, which matches the desired, close-to-final geometry, has been produced in 2017. Batches of mechanically compliant pieces were ordered from three manufacturers. Each batch was made and assembled using a different manufacturing process with a unique set of design constraints and achievable product specifications. Deliberately implemented failure modes and an on-board temperature monitoring were used to characterize the test system and the developed functional testing procedures. The performance results are presented in terms of the quality control effectiveness, testing time and hybrid cooling properties. The conclusions drawn from this experience have guided the strategy of the quality verification for the mass production phase of front end hybrids for the CMS Outer Tracker upgrade.

2. Description of the quality control plan for front end hybrids

An assembly of one double-sensor module for the future CMS Outer Tracker will require precise gluing of its components and as many as 4,000 wire bonds to be placed. These two factors are limiting the possibility of rework and especially the chance of exchanging a non-functioning front end hybrid. According to initial specification, one malfunctioning ASIC is enough to reject a whole assembled module. Therefore, to achieve a high yield of modules it is crucial to fully test all the hybrids before they are used for integration. The quality control procedure was divided into two steps: an optical inspection and a set of active tests.

In the current shape the optical inspection of the front end hybrids consists of 23 tests and 10 measurements. The tests cover: visual check of the quality of the solder and adhesive joints, cleanliness of the circuits, flatness of the bond pads, as well as placement and alignment of the components. The measurements include: outer dimensions, thickness of the flex, the bond row straightness, weighing and a set of hybrid-specific measurements. The optical inspection allows for an early detection of non-compliant pieces that would not enable a correct construction of a module or degrade its long-term performance. The optical inspection is done on inactive hybrids, therefore it does not verify electrical performance or the proper functionality, both crucial to qualify a hybrid.

2.1 Description of the active test methods

To fully qualify a hybrid a set of active test methods is executed after the optical inspection. The methods focus on the verification of the proper interconnectivity of the components on the front end hybrid circuit, in particular the flip-chip ASICs. This routine has become especially important after experiencing several assembly problems reported by different manufacturers of the hybrids. The issues concerned almost exclusively the connectivity of the bump bonds to the flexible circuits, originating from a non-flat surface of the flex. The active test methods require the use of a full read-out chain, such that data can be acquired from the front end ASICs. By executing this test routine one also verifies the proper functionality of the hybrid. The active tests are executed in the following order:

1. Power consumption,
2. Slow control interface and configuration registers accessibility,
3. Clock, fast commands and data interfaces verification,
4. Calibration of analogue front end channels and post calibration measurement of channels' activity,
5. Two specific tests for the detection of open and shorted analogue connections.

During the production phase, failing one of the above tests rejects a hybrid and no further steps are executed so as to save time. All of the mentioned active test methods have been described in [2].

A new approach of capacitive charge injection has been implemented for finding open analogue connections. It relies on signal injection strips buried under the wire bond pads directly inside the flexible circuit of the hybrid. This solution eliminates the problems of precise positioning of an external antenna circuit described in [2] thus speeding up the testing procedure. After being used, those signal injection strips need to be grounded to avoid the presence of floating conductors in the close proximity of analogue interconnections. This is performed during the module assembly in the wire bonding step.

Tests specific to the verification of the analogue interconnections require calibration of all front end channels of the hybrid. In the previously implemented procedure the calibration was based on the S-curve scan followed by its midpoint extraction for every individual channel. This was performed to equalize the noise response of the front end. An innovation was introduced to the calibration procedure, which relies on the binary search algorithm. It enables midpoint extraction without the necessity of the S-curve scan. The time gain in the new algorithm is logarithmic. For example, for a 10-bit DAC it requires only 10 data taking iterations instead of full 1024-step S-curve scan. The logic of shorts and opens recognition remained unchanged and is described in [2].

3. Description of the test validation hybrid

A hybrid was designed with deliberately implemented failure modes to verify the accuracy of the proposed test methods. It hosts two functioning ASICs, 7 dummy chips and the charge injection strips buried inside the circuit. It solves the temporary interconnection via a mezzanine connector, or alternatively, a pattern of probe pads such that it can be communicated with in the test setup [3].

Three manufacturers were selected to produce the designed hybrid. Two companies delivered completed circuits, 14 units each. The defects implemented in the hybrid's design are listed below:

- 7 shorts per functioning ASIC between pairs of analogue front end channels,
- 3 shorts per functioning ASIC between a front end channels and GND net,
- 8 opens in one functioning ASIC including:
    - 3 broken traces,
    - 5 missing vias.

4. Results of the active tests

An interface card was designed and produced, which allows data transfers from the functioning front end ASICs to an FPGA board connected via Ethernet link to a PC. A dedicated software controlling data transfers and executing test routines has been written and used for obtaining test results. All of the hybrids from both manufacturers (later referred to as X and Y) have been optically inspected and have undergone the active test routines. These tests were first conducted at room temperature and after that in the cold box.

The acceptance threshold for the current consumption was initially set to 5% from the average value of known good hybrids in both idle and busy state of operation. The shorts' searching algorithm should find 14 shorts per hybrid between analogue channels and 6 shorts of analogue channels to the GND net. The opens detection should expose 11 open connections as it is not able to distinguish between an open connection and a grounded channel. Therefore, in the post-processing of the results one should exclude grounded channels from the list of detected opens. The summary results of the active tests are presented in the Tables **1** and **2**.

Table 1. Summary of the active test results obtained with hybrids from the company X.

ID	Current consumption [AVG: 105.5mA / 151.5mA]	Data links and configuration registers diagnosis	Analogue shorts detection mutual, to GND, [+ additional]	Analogue opens detection implemented, [+ additional]	RESULT
X.1	idle: AVG - 6.73%, busy: AVG - 12.67%	Fast data interface out of order	Fast data interface out of order	Fast data interface out of order	NEG.
X.2	idle: OK, busy: OK	Links: OK, registers: OK	9/14, 4/6, [+ 0/0] too many missing shorts	9/11, [+ 53/0] too many additional opens	NEG.
X.3	idle: AVG + 5.59%, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 1/0]	POS.
X.4	idle: OK, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 8/0]	POS.
X.5	idle: OK, busy: OK	Links: OK, registers: OK	13/14, 6/6, [+ 0/0]	9/11, [+ 3/0]	POS.
X.6	idle: OK, busy: OK	Links: OK, registers: OK	12/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
X.7 to X.14	idle: OK, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.

Two hybrids delivered from company X would be rejected based on the results of the active test methods. One because of suspiciously low current consumption and lack of communication with the ASICs, another because of the extensive number of open analogue connections. Four hybrids presented some minor issues related to a few disconnections in the analogue paths. The assembler of these hybrids, has confirmed its problems with the flip-chip connectivity, which were verified against the X-ray scans. Eight hybrids were performing in a satisfactory manner, having all implemented flaws detectable thus confirming the accuracy of the developed test methods. Two, always the same, opens in the analogue channels cannot be detected due to a design issue. This issue will be solved in the next hybrid designs.

Table 2. Summary of the active test results obtained with hybrids from the company Y.

ID	Current consumption [AVG: 105.4mA / 151.5mA]	Data links and configuration registers diagnosis	Analogue shorts detection mutual, to GND, [+ additional]	Analogue opens detection implemented [+ additional]	RESULT
Y.1	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 1/0]	POS.
Y.2	idle: OK busy: OK	4 R/W/T errors (I^2C)	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
Y.3	idle: OK busy: OK	12 R/W/T errors (I^2C)	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
Y.4 to Y.14	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.

Three hybrids delivered from company Y presented some minor issues. One had a single analogue channel disconnected from the ASIC. Two other hybrids had several read, write or timing errors on the I^2C interface, however all of these errors were recovered in a single transaction retry. These

incidents were associated with a too big pull-up resistance. Eleven hybrids were performing in a satisfactory manner, having all implemented flaws detectable thus confirming the accuracy of the developed test methods. The same two opens, as in the hybrids from the company X, could not be detected for the reason already explained.

Tests conducted in the prototype cold box gave identical results as the room temperature ones, however, the target temperature was not yet achieved. During those tests the active ASICs were at approximately -13°C. The development on this front continues in order to comply with the target cooling conditions planned for the future CMS Outer Tracker.

Total execution of the active test methods took approximately 42 seconds per hybrid. This time does not include manual operations necessary for the placement of the hybrid in the test setup and any other activities related to the preparation of the equipment or cooling. The final hybrids planned for the construction of the upgraded CMS Outer Tracker will host four times more active front end ASICs. It could result in a longer testing time, however the new generation of ASICs will operate with an eight times faster bit transaction and the firmware development group focuses on the optimization of the data flow. Therefore, at the current stage, it is impossible to precisely estimate the testing time per hybrid for the production phase.

5. Conclusion

Approximately 30,000 front end hybrid assemblies are required for the construction of the future CMS Outer Tracker. Several test methods were chosen for the optical inspection and active testing of these hybrids. An uncommon approach has been proposed for testing of the connectivity of the front end ASIC's analogue inputs. This approach is based on two statistical methods, which implement different sources of signal injection to the analogue channels. One method that detects shorted connections relies on the internal pulse injection often named by ASIC designers as a calibration or a test pulse. The other method, for the detection of open connections, utilizes external, capacitively coupled signals. A dedicated hybrid was designed with deliberately implemented failure modes for a validation of the proposed test scheme, in particular these two innovative test methods. A total of 28 units were produced according to the design by two vendors and tested upon reception. The quality control scheme enabled a successful detection of the implemented flaws and additional issues that occurred during the assembly of the circuits.

This experience has guided the future front end hybrid design for testability. It has also confirmed the adequacy of the chosen quality control steps as well as the accuracy of the implemented active test methods.

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