PROCEEDINGS OF SCIENCE

The Development of Front-End Readout Electronics for ProtoDUNE-SP LAr TPC

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As a prototype of Deep Underground Neutrino Experiment far detector, ProtoDUNE single-phase liquid argon Time Projection Chamber will sit in H4 beam line at CERN to study detector response to particles. It consists of 6 full-size Anode Plane Assemblies (APAs) plus 2 Cathode Plane Assemblies (CPAs) to form two 3.6m drift regions with total 15,360 readout channels. To achieve optimal noise performance, readout electronics developed for extremely low temperatures (77K-89K) operation has been studied with an integral design concept of APA, cold electronics, feed-through, plus warm interface electronics with local diagnostic following strict isolation and grounding rules. By the end of September 2017, the first full-size APA has been integrated with readout electronics successfully for the coming cold integration test at CERN.

Topical Workshop on Electronics for Particle Physics
11 - 14 September 2017
Santa Cruz, California

*Speaker.

PoS(TWEPP-17)060

1. Introduction

The Deep Underground Neutrino Experiment (DUNE) is a leading-edge, international experiment for neutrino science and proton decay studies [1]. As a crucial part of the DUNE effort towards the construction, ProtoDUNE single-phase (ProtoDUNE-SP) is a significant experiment in its own right [2]. With a total liquid argon (LAr) mass of 770 tons, it represents the largest monolithic single-phase LAr Time Projection Chamber (TPC) detector to be built to date. The detector is housed in an extension to the EHN1 hall at CERN, aiming to take its first beam data before the LHC long shutdown at the end of 2018. It consists of 6 full-size Anode Plane Assemblies (APAs) plus 2 Cathode Plane Assemblies (CPAs), which gets 2 $\times$ 3.6m drift regions and 15,360 TPC readout channels, as shown in Figure 1. The test-beam program for ProtoDUNE-SP will be a key test of components, construction methods, installation procedures, commissioning, and detector response to particles.

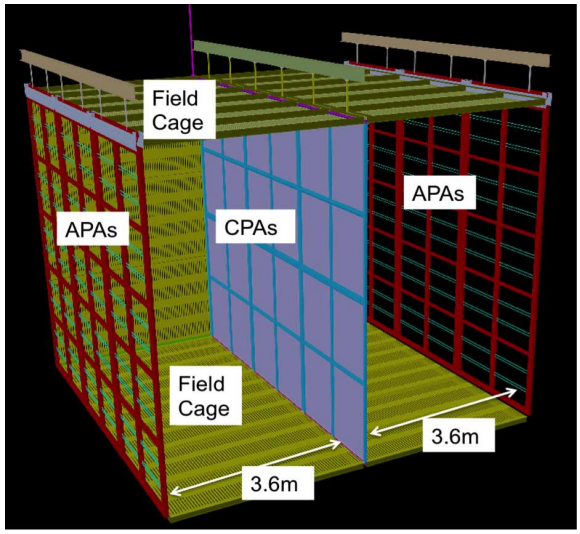

Figure 1: ProtoDUNE-SP LAr TPC with 6 APAs and 2 CPAs to form 2 drift volumes

According to physics simulations, Equivalent Noise Charge (ENC) of DUNE single-phase far detector should be less than 1/9 of the expected worse case instantaneous charge arriving at the APA from a minimum-ionizing particle (MIP), which requires ENC for induction wires to be less than 1000e^-. As an enabling technology for noble liquid detectors in neutrino experiments, readout electronics developed for extremely low temperatures (77K-89K) decouples the electrode and cryostat design from the readout design [3]. With electronics integrated with detector electrodes, the noise is independent of the fiducial volume and much lower than with readout electronics at room temperature.

2. Overview of Front-End Readout Electronics

Front-end (FE) readout electronics designed for ProtoDUNE-SP consists of cold electronics and warm interface electronics, as shown in Figure 2. Cold electronics, which is placed close to the wire electrodes inside the cryostat to minimize the length of signal cables, consists of 120 Front-End Mother Board (FEMB) assemblies to amplify, shape, digitize and transmit 15,360 TPC channels to warm interface electronics through copper cold cables. Warm interface electronics with local diagnostic, which aggregates all the data from cold electronics and interfaces to DAQ system

through up to 10 Gb/s optical links, is installed in the crates on signal feed-through flanges of the cryostat.

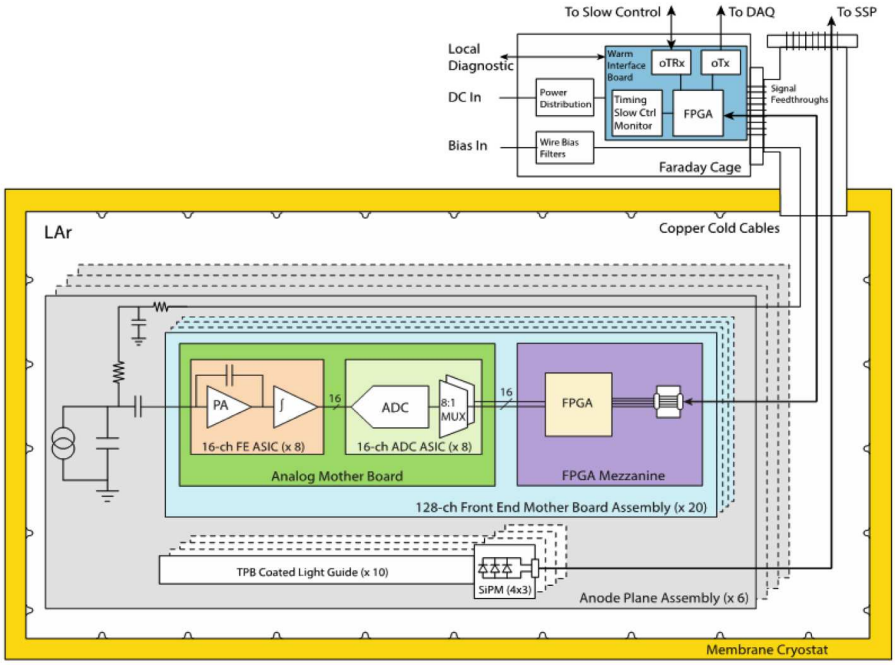

Figure 2: Front-end readout electronics system for ProtoDUNE-SP

3. Cold Electronics

Benefit from the charge carrier mobility in silicon increasing and thermal fluctuations decreasing with kT/e when CMOS devices are operating at 77K-89K temperatures, the noise of cold electronics is less than half as they are at room temperature (300K). However, there nearly wasn't any semiconductor device dedicatedly designed for cryogenic temperature operation [4]. BNL has started cryogenic CMOS ASIC R&D since 2008. After studies of the transistor characteristics and lifetime at cryogenic temperature, the microelectronics group designed an FE ASIC and an ADC ASIC suitable for 77K-300K operation and long lifetime with lower power consumption [5][6]. Meanwhile, various commercial CMOS devices were screened to find survivors at cryogenic temperature. Two CMOS devices, a low voltage regulator from TI and an Altera Cyclone IV FPGA were qualified for cold electronics development. With aforementioned key components, a 128-channel FEMB has been designed as the key building block of the cold electronics system. An FEMB assembly is comprised of an analog motherboard (AM) and an FPGA mezzanine (FM). An AM has 128 channels with 8 FE ASICs and 8 ADC ASICs on board. The FE ASIC has 16 channels of charge amplifier and shaper with programmable gain and filter time constant. The ADC ASIC has 16 channels of 12-bit ADC with 2MHz sampling rate. FM multiplexes and transmits 128 channels of digitized signal through four 1 Gb/s serial copper links to warm interface electronics.

4. Warm Interface Electronics

Warm interface electronics, which is housed in warm interface electronics crates (WIECs) attached directly to the signal feed-through flanges, is the interface between the cold electronics and DAQ system. Each WIEC has one Power and Timing Card (PTC), five Warm Interface Boards

(WIBs) and a passive Power and Timing Backplane (PTB) inside the crate. The PTC provides a bidirectional fiber optical link to the timing system. It is used to fan out clock and control signals to WIBs through PTB. A WIB, which hosts 4 FEMBs, forwards system timing signals to FEMBs and receives the high-speed data from FEMBs simultaneously, it also re-organizes and transmits the data to the DAQ system over fiber optical links. WIB has built-in Gigabit Ethernet port for slow control interface, which can also be used as local diagnostic to read FEMBs out. The cold electronics performance can be studied using the integrated local diagnostic on WIB without DAQ system, which is a crucial tool during the cold electronics installation and checkout tests. As to power distribution, PTC uses DC-DC converters to step down a 48V input to 12V for WIBs, WIB uses on board DC-DC converters to generate low voltages for FEMBs.

5. Integration Test at BNL

LAr TPC uses extremely sensitive front-end electronics to measure the charge from TPC wires. As a necessary but not sufficient condition to achieve a good noise performance, the integral design concept of APA, cold electronics, feed-through and warm interface electronics with local diagnostic following strict isolation and grounding rules must be investigated [7]. Therefore, a 40% APA integration test stand is built at BNL. The APA area, which is ∼45% of DUNE full-size APA (6.0m $\times$ 2.3m), is about 2.8m^2 with 2.8m X-plane collection wires and 4.0m U- and V-plane induction wires. It has 1024 sense wires to be read out by 8 FEMBs. To study grounding and isolation rules for ProtoDUNE-SP, a specific scheme was developed following the experience from ATLAS and MicroBooNE experiments. The common of FE ASIC chips and of the rest of cold readout are connected to the common of FEMB, which is connected to the APA frame over adapter boards. Through cold data and power cables, the common of FEMBs is connected to the flange board embedded in the signal feed-through flange assembly. Any potential ground loops have been removed to make sure the flange is the only place for connection between APA frame and the cold box.

The noise performance of 40% APA submerged in liquid nitrogen is quite promising. The ENC of induction plane (U or V) is 400e$^-$ and of collection plane (X) is ∼340e$^-$ at 1 μs peaking time. Based on the test results, a noise projection is made to predict the noise performance of ProtoDUNE-SP as shown in Figure 3. The noise of ProtoDUNE-SP induction plane is expected to be ∼600e$^-$ and collection plane is ∼500 e$^-$, which meets the design requirements.

6. Readout Electronics Installation for ProtoDUNE-SP at CERN

In order to evaluate full-size APA and cold electronics performance, a cold box was built for integration test at CERN. The integration test stand incorporates a full-size signal feed-through assembly and uses cables and readout electronics identical to the production system. This allows vertical slice test of APA wires and photon detectors on production APA frames. To be emphasized, the integration test stand at CERN follows the same isolation and grounding rules verified by 40% APA test stand at BNL. By the end of September 2017, the first APA of ProtoDUNE-SP was fully instrumented with 20 FEMB assemblies. A checkout test, which uses built-in calibration circuit on FE ASIC to characterize the readout electronics system, has been performed at room temperature. Through averaging calibration response, which is necessary to cope with the environmental pick-up to the unshielded APA, functionality of all readout channels has been verified. The results indicate that all 2,560 FE channels are functioning well, except one channel is not connected to the

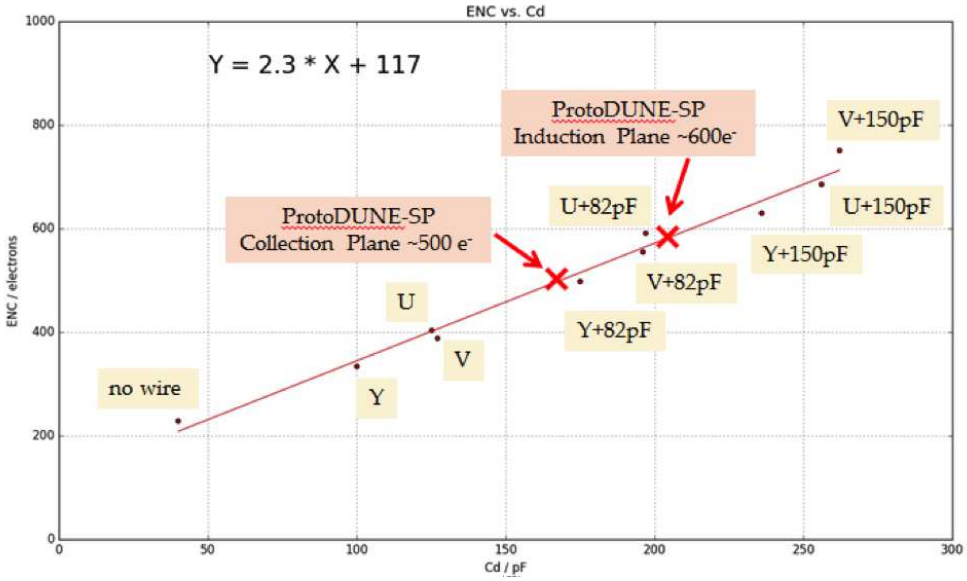

Figure 3: ENC projection for ProtoDUNE-SP based on 40% APA test results

APA properly due to mechanical interface. According to the latest schedule, APA with cold electronics will be moved into the cold box to evaluate detector performance at cryogenic temperature in November.

7. Summary

The ProtoDUNE-SP front-end readout electronics designed for cryogenic temperature (77K-89K) is progressing well. The first full-size APA integrated with cold electronics is ready for the cold test to characterize the noise performance at CERN. It is anticipated that the integration test at CERN will be a critical effort in coming months till the final installation of ProtoDUNE-SP detector is complete.

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