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Serial Powering Optimization for CMS and ATLAS Pixel Detectors within RD53 Collaboration for HL-LHC: System Level Simulations and Testing

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Serial powering is the baseline choice for low mass power distribution for the CMS and ATLAS HL-LHC pixel detectors. Two 2.0 A Shunt-LDO regulators are integrated in a prototype pixel chip implemented in 65-nm CMOS technology and used to provide constant supply voltages to its power domains from a constant input current. Performance results from testing prototype Shunt-LDO regulators are shown, including their behaviour after x-ray irradiation. The system level simulation studies, which had been performed with a detailed regulator design in a serially powered topology, have been validated.

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1. Introduction

The pixel detectors of the ATLAS and CMS experiments of the HL-LHC era have stringent design requirements, including a radiation tolerance of at least 500 Mrad, increased granularity as well as high hit (3 GHz/cm^2) and trigger rates (1 MHz and 12.5 μs latency). Another severe challenge is the reduction of material in the tracker volume in order to maximise physics performance. A new generation pixel chip has been designed in 65-nm CMOS technology within the RD53 collaboration [1] addressing these issues and featuring shunt-LDO regulators (SLDO). The SLDOs are capable of delivering the regulated analog and digital power supplies to the chip with a total current of up to 1.5 A (max. 2.0 A) under normal operating conditions.

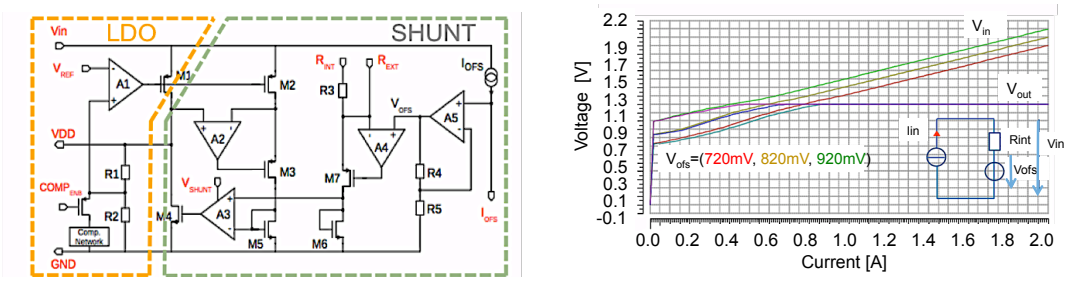

Figure 1: A Simplified schematic of the new version of the SLDO (left) and its characteristic IV curve for three offset voltage values (right).

A serial powering scheme [2], based on this on-chip integrated and radiation hard SLDO, significantly reduces the amount of needed cables as well as the power losses within them and hence the material inside the tracker volume. In a serial power topology, pixel modules, composed of up to four chips, are serially powered by a constant current supply and each pixel chip is powered in parallel. The current injected in the power loop must satisfy the highest possible load current and include an extra headroom to comply with fast dynamic current variations of the digital logic of the chip. Consequently, each serial power chain will require an injected current of up to 8.0 A, out of which 6.0 A would be consumed by the pixel chips and 2.0 A would be the extra current headroom (25%). Since it is crucial that the digital current variations do not affect the sensitive analog front-end part of the chip, two SLDOs are integrated on the chip, one per power domain, and the analog and digital circuitry are in separated deep N-wells for best possible substrate isolation.

2. An improved Shunt-LDO regulator

The SLDO concept [3], first introduced in the FE-I4 chip (130 nm, 0.5 A version), combines a Low Drop-out (LDO) regulator with a shunt. Any excess current injected into the serial power chain will be shunted, while the linear regulator part will provide the required voltage, equal to twice the reference voltage (V_{ref}). The SLDO has been redesigned for the RD53A chip in 65-nm CMOS technology and it is able to carry up to 2.0 A. Two SLDOs of 2.0 A are integrated in the RD53A, one per power domain, powered in parallel. Since a maximum current of 2 A per chip is expected during operation, having two parallel 2.0 A SLDOs in a chip corresponds to a current margin of $\sim$100%.

The resistive behaviour of the SLDO (see right Figure 1) allows for operating multiple SLDOs in parallel, with well-defined current sharing, determined by their effective resistance, which is configurable (R_{int}/R_{ext} in Figure 1). An important and novel SLDO feature is a configurable offset voltage, which allows an optimisation of the power consumption when a chip in a module fails (more details in subsection 3.3). In addition, the SLDO control loop has been improved to assure stability with capacitive loads (due to the increased number of logic gates) and off-chip decoupling capacitors O(μF) are used for stabilising the LDO at the input and the output of the circuit.

System simulations presented in [4] studied the SLDO performance in a serial power topology including the SLDO detailed design, decoupling capacitors, parasitics and dynamic power profiles of the chip's activity. These studies showed that thanks to the presence of multiple decoupling stages (off-chip decoupling capacitors, local decoupling of ∼300 nF for the digital and ∼70 nF for the analog part) and the isolation of the power domains, most of the fast current variations would be absorbed and the noise coupling between the two power domains would be within acceptable levels[1].

3. Testing results of Shunt-LDOs

Prototype SLDO test chips were used to study SLDO characteristics, i.e. the effective resistance, the configurable offset voltage and the noise coupling among SLDOs (parallel and serially powered) as well as the radiation hardness of the SLDO.

3.1 Transient tests

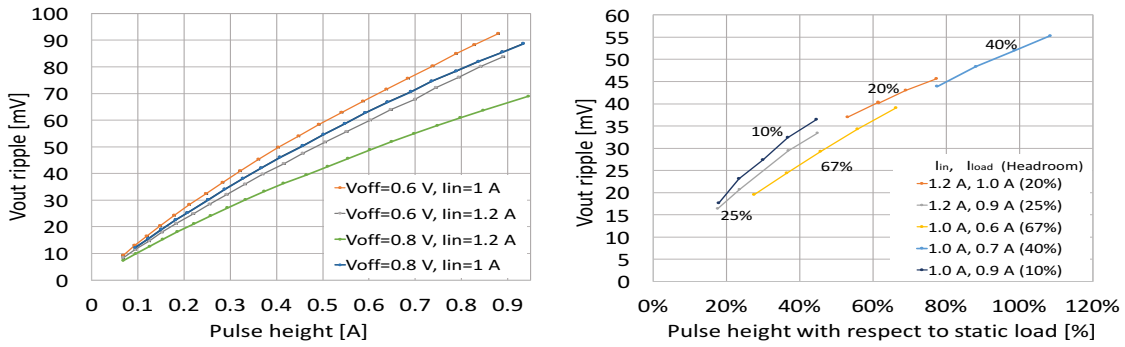

Figure 2: Measurements of output voltage ripple during transient load tests for various combinations of offset voltage and input current (left) and current headroom and static load (right).

During the transient load tests the simulation results were confirmed as the noise coupling of the SLDOs operated in parallel and in series was negligible. The measured output voltage ripple of a SLDO was less than 100 mV for extreme and fast load transients, similar to the ones from the digital activity. In addition, as shown in the left plot of Figure 2, the SLDO transient performance improves when operated with a higher V_{offs}(0.8 V), an effect more pronounced for higher input currents (1.2 A). Therefore, it is recommended to operate the SLDO with a relatively high offset

[1]For a digital power profile for nominal hit and trigger rates: 100 mV transient noise in the output voltage of the digital part, less than 10 mV for the analog part and negligible noise coupling among modules in series.

voltage, combined with a decreased effective resistance (R3, see left plot of Figure 1) to maintain the full nominal range of operation (2 A current). As shown in Figure 2, the output voltage ripple improves when increasing the value of the current headroom. This is due to the higher operating point of the SLDO making it faster. Nevertheless, the improvement is not significant and sufficient to justify a very high extra headroom, taking into consideration the induced increased power losses in the shunt. Therefore, a current headroom of 10% to 25% is suggested as the optimal balance point between transient performance and power penalty.

3.2 Irradiation up to 600 Mrad

During an x-ray irradiation campaign at CERN, two SLDO 2.0 A test-chips were irradiated up to 600 Mrad each at a different temperature (25° C and −10° C)[2]. The measurements for the irradiated cold chip are presented in Figure 3 and show only 8 mV difference in the output voltage, and a slight increase in the input impedance of the chip (slight increase in V_{in}) probably caused by a threshold shift in the circuitry. The results at room temperature were similar. These changes are acceptable and therefore the SLDO is proven to be sufficiently radiation hard for use in the harsh environment of future pixel detectors at HL-LHC.

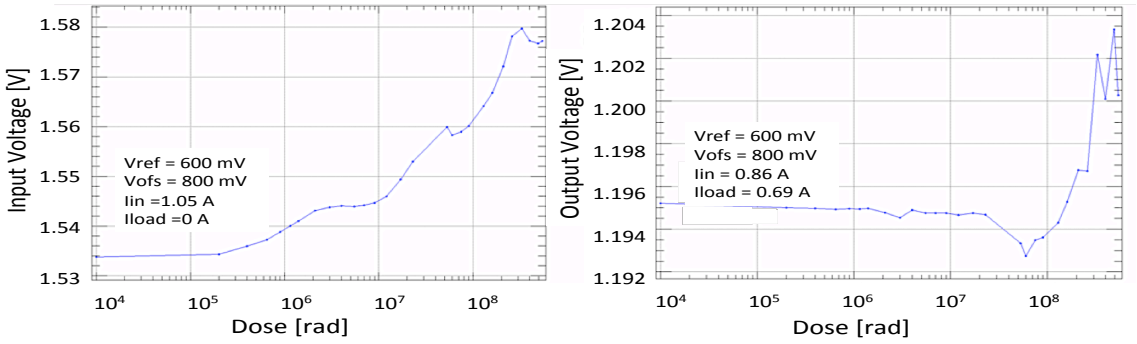

Figure 3: Input (left) and output (right) voltage of the SLDO during irradiation for 600 Mrad.

3.3 Failure scenarios

There are two main failure scenarios to be considered, an open-circuit and a short-circuit. When a chip in a four-chip module acts as an open-circuit (centre of Figure 4), the remaining chips of the module would receive an increased current, shifting to a higher operational point[3] but would remain fully functional, along with the rest of the modules in series. In a short-circuit scenario (right sketch of Figure 4), a chip acting as a short would get a current much higher than 2 A. In this case, the other pixel chips of the module would be underpowered and not functional as the remaining current would not be sufficient for their operation. However, the modules in series would not be affected as the total current in the chain would remain constant. Protecting mechanisms could be considered for these scenarios such as an over-voltage clamp for more extreme open-circuit

[2]The one at room temperature (25° C) was irradiated with a low rate for the first 2 Mrad followed by a rate of ∼3.5 Mrad/h. The other one was cooled down (−10° C) and was irradiated with a constant rate of ∼3.5 Mrad/h.

[3]A high V_{offs} combined with a low R_{eff} allows the remaining chips to be fully functional (V_{in}<2 V) for high input currents.

scenarios or a current-limit mechanism ($I_{short} = I_{limit}$) for the short-circuited chips where the I_{tot}-I_{limit} would be sufficient to operate the neighbouring chips. Preliminary testing in the lab with the setup of Figure 4 has helped understanding these failure modes and more in depth testing with emulated failures is expected to be carried out with RD53A chips.

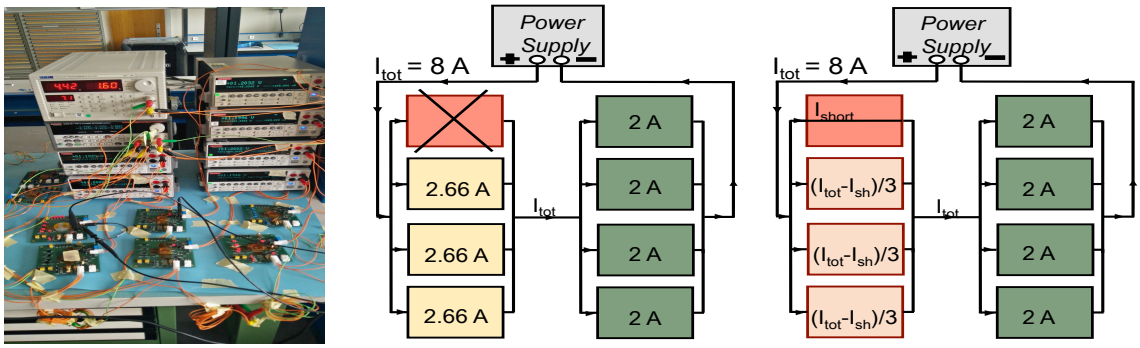

Figure 4: Test setup of serially powered SLDOs (left). Open-circuit (center) and short-circuit (right) failure scenarios.

4. Conclusions

An enhanced radiation hard version of the shunt-LDO regulator in 65-nm CMOS technology for 2 A has been tested. It features a configurable offset voltage, which combined with the configurable resistance, allows for power optimisation of a serial powering scheme. Previous system simulations were confirmed by measurements showing negligible effect of noise coupling in a serial power topology. The transient noise was measured to be within acceptable levels and can be optimised by operating the SLDO with relatively high offset and a current headroom of about 10-25%. Future work will focus on testing RD53A chips with different configurations and emulated failures as well as high voltage distribution studies with chips and sensors.

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