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Manufacturing experience and test results of the PS prototype flexible hybrid circuit of the CMS Tracker Upgrade

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Abstract

The CMS Tracker Phase Two Upgrade for HL-LHC requires High Density Interconnect (HDI) flexible hybrid circuits to build modules with low mass and high granularity. The hybrids are carbon fibre reinforced flexible circuits with flip-chips and passives. Three different manufacturers produced prototype hybrids for the Pixel-Strip type modules. The first part of the publication will focus on the design challenges of this state of the art circuit. Afterwards, the difficulties and experience related to the circuit manufacturing and assembly are presented. The description of quality inspection methods with comprehensive test results will lead to the conclusion.

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1. Introduction

Components for the Compact Muon Solenoid (CMS) Tracker Phase Two Upgrade for the High Luminosity Large Hadron Collider (HL-LHC) are currently under development. Modern HDI circuits are essential to address the requirements imposed by the HL-LHC. The most challenging requirements for the electronics are the 56 Mrad total dose of irradiation [1], reliable operation for 15 years, low power consumption and operation at around -20℃. The upgraded CMS Tracker will use two main types of modules: the Pixel-Strip (PS) modules and the Strip-Strip (2S) modules. The front-end electronics of both types of modules are based on flexible hybrid circuits folded and wire-bonded to the strip sensors and the Macro Pixel ASICs (MPA). The front-end hybrid circuits host the binary readout ASICs and provide the interconnection to the sensors and other system elements. The PS mock-up (PS-MCK) hybrid circuit prototype was designed to exercise and test the flip-chip soldering technology, carbon fibre stiffener lamination, assembly procedures, production testing and module construction. Three manufacturing consortia produced the PS-MCK hybrid circuits using different manufacturing processes and different assembly routines. Each manufacturer had various difficulties during the production (insufficient surface flatness, open and short circuits, thermal expansion coefficient mismatch). The paper will present the cause of difficulties and explain the available solutions in the design and production phases.

2. The PS-MCK hybrid design

The main goal of the PS-MCK circuit is to provide a flex circuit which has a construction and outline that is very similar to the final PS front-end hybrid. A mock-up circuit was made because essential components, such as the Short Strip ASIC (SSA), Macro Pixel ASIC (MPA) and the Concentrator ASIC (CIC), were not available at the time of the production. The hybrid allows the construction of dummy PS module prototypes, provides feedback about the design concept, qualifies future hybrid manufacturers and verifies future hybrid features and test methods [2]. The PS-MCK hybrid is laminated on high modulus carbon fibre laminate stiffeners and folded to fit in the PS module mechanics. The PS-MCK hybrid has approximately the same level of difficulty as the final PS front-end hybrid, in terms of the circuit substrate production and the assembly. Figure 1 shows the required construction of such a hybrid.

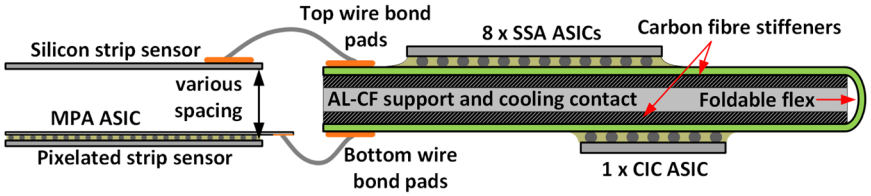

Figure 1 Cross section view of the PS module front-end hybrid construction.

The front-end hybrid circuit prototypes made for the CMS Tracker Upgrade are all using a four layer build-up with 25 µm thick polyimide dielectric layers in order to lower the mass of the circuits and enable the folding. The copper thickness is ranging from 9 µm to 12 µm. The smallest track width and spacing required to interconnect the 250 µm pitch flip-chip ASICs is 40/40 µm respectively. Via in pad technology is applied to save space in the dense regions of the circuits. The laser drilled via diameters range from 25 µm to 50 µm and they are copper filled on the top and bottom layers to increase the reliability of the circuits. The smallest capture pad size is 110 µm. These feature sizes require state of the art HDI production technologies that are challenging for most of the companies in this field.

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The HDI circuit design requires the usage of special features such as: “teardrops”, crosshatched planes, vent holes and very well balanced copper structures. “Teardrops” are stress relief structures used when a thin trace is connected to a relatively large copper structure. The trace is smoothly tapered to the final thickness. Crosshatched planes are required in the flexible zones to keep the circuit flexible and the best practice is to use 45˚angle sections. Vent holes should be placed every millimetre in larger plane areas to improve the adhesion of the adhesive layers. Copper balance is essential to keep the circuits flat during the soldering process. This means that the copper area should be equal on inner layer pairs and outer layer pairs to keep the circuit’s thermal expansion symmetric. Impedance calculations require special attention as well, because traditional calculator tools might not be precise for these feature sizes [3].

3. Implemented functions in the PS-MCK

The flip-chip connectivity, HDI tracks and microvias are the most critical elements in terms of production failures. Various features are implemented in the PS-MCK to verify the quality of the circuits and the flip-chip assembly. A 50 pin mezzanine connector provides data connectivity in parallel with a 60 pin needle probe test socket. Both can be used for interconnection during the circuit testing. Two active CMS Binary Chip V2 (CBC2) chips and 7 dummy flip-chips are mounted on the circuit. The wirebond pads connected to one of the two active chips are fitted with an embedded antenna strip, which can be used to inject a signal and detect interconnectivity failures. Both CBC2 chip analogue interconnections are implemented with on-purpose failures such as: shorted channels, open channels and shorted channels to the ground plane. These failures are used to check the validity of the test methods using the antenna signal. The implemented antenna test structure is illustrated in Figure 2.

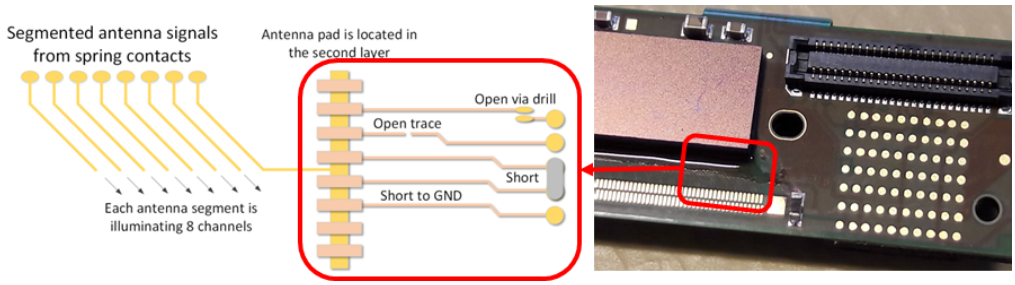

Figure 2 The embedded antenna trace with implemented failures (left) and the means of interconnections on the PS-MCK hybrid (right).

Heating resistors are mounted on the hybrid to provide the equivalent heat load that would be created by the SSA and CIC chips during the operation. A high voltage filtering circuit with the corresponding connectors is placed on the PS-MCK. The effect of the fold over on the differential impedance is tested by impedance test structures. The PS-MCK panel contains a test coupon which is useful to determine the quality and the reliability of the via structures and the flip-chip bonding. Figure 3 shows the top side of the assembled and folded hybrid. Figure 4 shows the bottom side of the assembled and folded hybrid. An aluminium-carbon fibre composite spacer is glued on the bottom to provide cooling contact and support in the module.

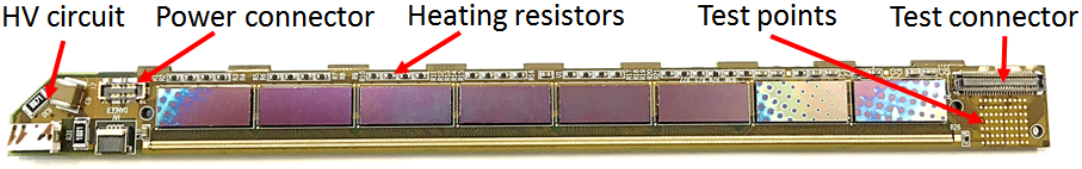

Figure 3 The top side of the PS-MCK hybrid is fitted with several test functions.

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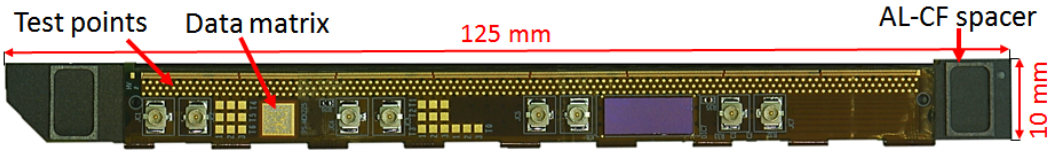

Figure 4 The bottom side of the PS-MCK hybrid is hosting the rest of the test features.

4. Quality test results

The quality of the PS-MCK was tested by the manufacturer and CERN. X-ray, cross-section analysis, scanning acoustic microscopy were applied on a sampling basis at the manufacturer's premises. Visual inspection, weighing and functional testing were carried out on each delivered circuit at CERN [4].

4.1. Checks before the assembly

A quality check of components is essential before assembly. It is advised to check the quality of bumps on flip-chips as defects are often affecting these delicate objects. It is also important to check the parameters of the components and verify that they conform to the specifications. Figure 5 shows examples of defects found during the checks before assembly.

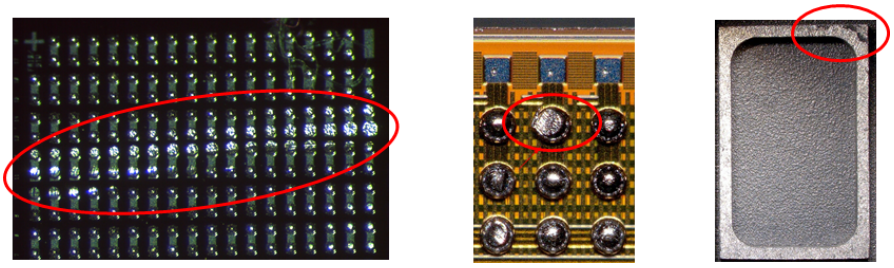

Figure 5 Damaged flip-chips and spacer found by the inspection before assembly.

4.2. Results of production testing

All the three manufacturer consortia were able to deliver functional circuits. The antenna test method was able to detect 6 out of the 8 implemented opens. The short detection method was able to detect all the shorted channels. Both methods showed good reproducibility and precision. The Panasonic 50 pin mezzanine connector and the needle probe tester were also successful to provide interconnection during the functional testing. Details of the test results can be found in [4]. The hybrid assembly was successful because the hybrid geometry followed the design specifications.

5. Problems and solutions

5.1. Solder mask fractures

The PS-MCK is folded sharply with a fold radius of 0.575 mm in order to fit in the PS module design concept. This tight folding requires special flexible solder mask materials. One of the suppliers used Peters Elpemer® SD 2463 FLEX-HF which has a minimum allowed bend radius of 1.5 mm. As a result, cracks were formed in the solder mask and these cracks propagated through the first copper layer. The traces in the first layer were cracked. The solution to this problem is to use a solder mask material that is more flexible, for example the Nippon Polytech Corp. NPR 80. The cracks are illustrated in Figure 6.

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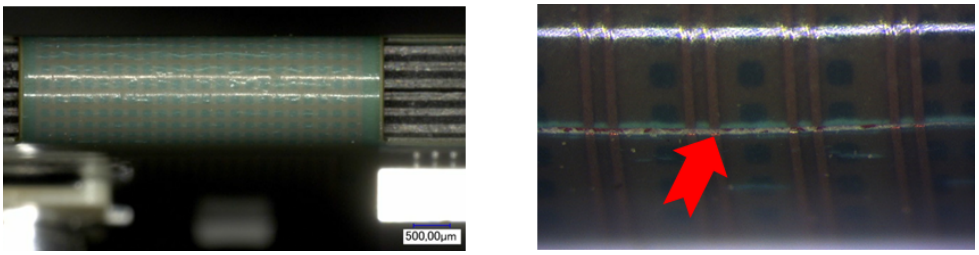

Figure 6 Solder mask cracks formed in the folded region of the PS-MCK.

5.2. Solder mask openings

The flip-chips are using solder mask defined copper land patterns in the case of two suppliers. The ball size of the daisy chain flip-chip varies significantly from the specified value in the datasheet of the component. Due to the manufacturing tolerances of one supplier, the solder mask opening is smaller than the design value. The assembly of the daisy-chain flip-chips is compromised by these mismatches in the case of this supplier. The solution to this problem is to increase the solder mask opening according to the process requirements or to use copper defined land pattern.

5.3. Surface deformation

The PS-MCK hybrids, as all front-end hybrid prototypes for the Phase Two Tracker Upgrade, are laminated on carbon fibre stiffeners with high tensile modulus and thermal conductivity. The hybrid lamination is done using a flexible adhesive layer between the stiffener and the hybrid. During the reflow, delamination can occur and the thermal expansion coefficient mismatch between the circuit and the stiffener leads to warpage. The surface flatness is not satisfactory in the delaminated areas, which compromises the flip-chip soldering. The solution to this problem is still being investigated, but the modification of the surface properties and the usage of a different adhesive are among the possible solutions.

6. Conclusion and future work

The PS-MCK is a successful PS front-end hybrid prototype, with useful test features. The hybrid production revealed several difficulties that the future circuits could face during the production. Solutions were introduced to improve the future production. The test features of the hybrid were used to tune and verify the antenna test method, the short finding algorithm and to prove that the used interconnection methods are applicable for a production level test system. Reliability tests of the assemblies need to be carried out in the near future. Electrical interconnection to the carbon fibre laminates will also be required in order to avoid noise injection into the front-end input channels. Several solutions to this problem are currently being investigated.

References

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