

# Adaption of an FPGA-based Sampling-ADC for the Crystal Barrel Calorimeter

---

**Johannes Müllers\***

*Helmholtz-Institut für Strahlen- und Kernphysik, Bonn University (Germany)*

*E-mail: [muellers@hiskp.uni-bonn.de](mailto:muellers@hiskp.uni-bonn.de)*

**Dr. Pawel Marciniewski**

*Ångströmlaboratoriet, Uppsala Universitet (Sweden)*

*E-mail: [pawel.marciniewski@physics.uu.se](mailto:pawel.marciniewski@physics.uu.se)*

**Timo Poller**

*Helmholtz-Institut für Strahlen- und Kernphysik, Bonn University (Germany)*

*E-mail: [poller@hiskp.uni-bonn.de](mailto:poller@hiskp.uni-bonn.de)*

**Dr. Christoph Schmidt**

*Helmholtz-Institut für Strahlen- und Kernphysik, Bonn University (Germany)*

*E-mail: [schmidt@hiskp.uni-bonn.de](mailto:schmidt@hiskp.uni-bonn.de)*

**Jan Schultes**

*Helmholtz-Institut für Strahlen- und Kernphysik, Bonn University (Germany)*

*E-mail: [schultes@hiskp.uni-bonn.de](mailto:schultes@hiskp.uni-bonn.de)*

**Prof. Dr. Ulrike Thoma**

*Helmholtz-Institut für Strahlen- und Kernphysik, Bonn University (Germany)*

*E-mail: [thoma@hiskp.uni-bonn.de](mailto:thoma@hiskp.uni-bonn.de)*

The digitization stage of the main electromagnetic calorimeter of the CBELSA/TAPS experiment in Bonn (Germany) is being equipped with 80 MS/s, 14 bit sampling-ADCs (SADCs), which were adapted from a prototype for the PANDA experiment. Onboard data processing with FPGAs allows determination of the signal characteristics, reducing the data volume substantially. The optional readout of the unprocessed sampled waveforms allows offline analysis and refinement of the FPGA algorithms. A partial setup has shown promising results during a photoproduction-beamtime. It has been demonstrated that the readout-rate limitation of the current QDC readout can be overcome. The full setup is planned to be commissioned within the next year.

This paper will present an overview of the SADC project. After an introduction of the CBELSA/TAPS experiment, the new SADC readout will be motivated, followed by its technical specifications and the setup in the experiment. An outline of the firmware and findings from first tests conclude the paper.

*Topical Workshop on Electronics for Particle Physics*

*11 - 14 September 2017*

*Santa Cruz, California*

---

\*Speaker.

## 1. CBELSA/TAPS Experiment

The CBELSA/TAPS experiment (fig. 1) at the 3.2 GeV Electron Stretcher Accelerator ELSA [1] in Bonn (Germany) is a baryon spectroscopy experiment, investigating the spectrum and properties of baryon resonances with masses up to 2.5 GeV by performing photoproduction experiments.

The photons are produced via bremsstrahlung and can be linearly/circularly polarized. Furthermore, a frozen spin butanol target provides longitudinally/transversally polarized nucleons, yielding access to double polarization observables, which are of utmost importance for extraction of resonances with partial wave analysis. The main electromagnetic calorimeter of the CBELSA/TAPS experiment is the Crystal Barrel detector, consisting of 1320 CsI(Tl) scintillator crystals with a radiation length of  $16.1 X_0$ . With the forward calorimeter TAPS it covers almost  $4\pi$  solid angle. The whole setup is ideally suited to measure the decays of neutral mesons into photon final states.

The Crystal Barrel detector has recently been equipped with a new Avalanche-Photodiode readout [2] to obtain full trigger capability through a faster signal with better SNR. The experiment will have a first production beamtime in December 2017. Within the scope of this modification, also parts of the readout and processing electronics have been or will be replaced. One of them is the analog processing and digitization stage of the Crystal Barrel calorimeter readout.

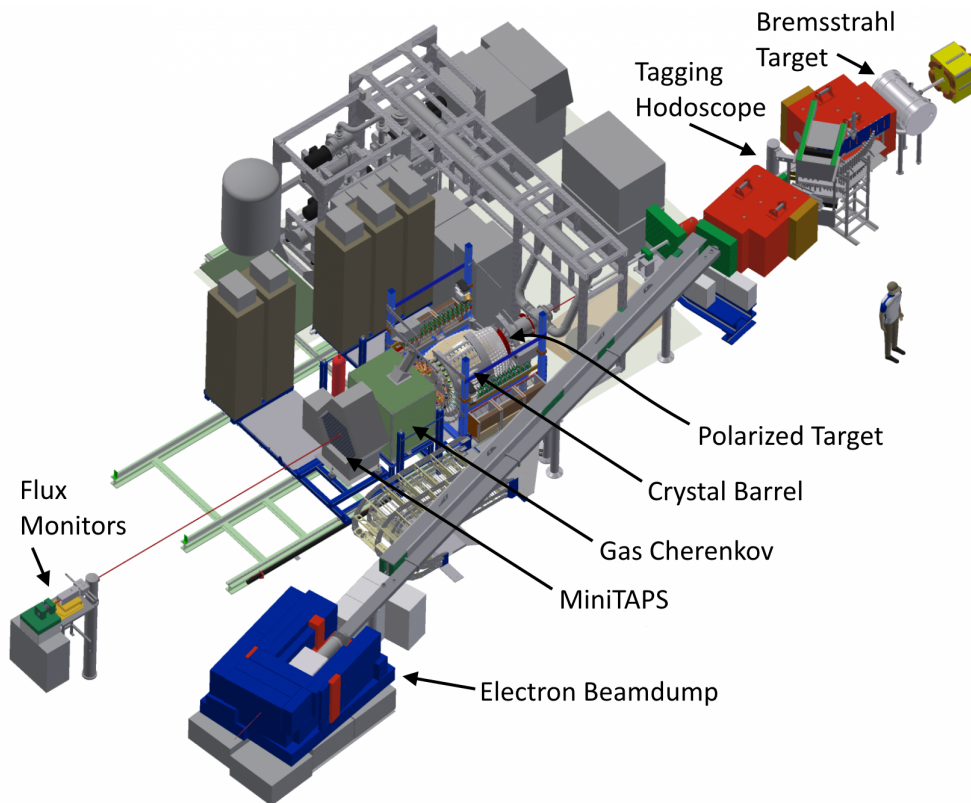


Figure 1: Setup of the CBELSA/TAPS experiment. Electrons from ELSA enter from the right. They are converted to energy-tagged photons, which impinge on the target in the center of the Crystal Barrel calorimeter. The final state particles are charge-tagged and measured in the Crystal Barrel detector or the forward BaF<sub>2</sub> calorimeter MiniTAPS.

## 2. New Sampling-ADC Readout for the Crystal Barrel Calorimeter

Presently, the Crystal Barrel calorimeter is being read out by the integrating Fastbus ADC LECROY 1885F (QDC). The analog signals are processed by an  $(RC-CR)^3$  shaper, resulting in a FWHM of approximately  $4\ \mu\text{s}$ . The shaper allows adjustment of two pole-zero compensation circuits to minimize undershoots, as well as adjustment of the baseline.

In the LECROY ADC, 96 channels are multiplexed to a single 12 bit sub-range ADC, which, due to an 8:1 dual-range circuit, yields a 15 bit resolution. The full setup of 16 LECROY ADCs is read out with Fastbus-VME bridges to be processed on two VME CPUs, which act as local event builders. The achieved energy resolution of 2.5 % at 1 GeV, as well as the readout rate, were considered to be sufficient. Yet, several points for optimization can be identified:

**Pile-Up Recovery** Due to the integrating nature of the LECROY ADC, pile-up events can neither be recognized nor corrected. It has been observed that the rate of pile-up events is non negligible in the experiment (depending on beam, radiator, and target configuration.).

**Readout Rate** Several systems in the experiment have been upgraded over the course of the years, hence is conceivable that the LECROY ADC readout will eventually become the limiting factor in the data acquisition. With a cumulated digitization and transfer time of more than  $400\ \mu\text{s}$ , the effective readout rate lies well below 2 kHz.

**Running Baseline** An event-based pedestal correction is not possible. Baselines can only be obtained at the begin of a data-taking run.

**Maintainability** As the digitizers are more than 15 years old, maintaining the system will become increasingly difficult. Additionally, it has been observed that the  $(RC-CR)^3$  shapers have arrived at the ascending branch of the bathtub curve, indicating increasing risk of failures.

In previous years, studies have been conducted, aiming to equip the Crystal Barrel calorimeter with commercially available sampling-ADCs using the VME standard (e.g. SIS 3320-250). Each of them was discarded in the end due to similar reasons:

- (1) The costs were too high due to a low channel density.
- (2) The resolution of the dual-range QDC could not be obtained with a single-range readout, doubling the necessary budget.
- (3) The firmwares of the modules were closed-source and hence did not allow the development of custom, optimized algorithms.

A promising opportunity opened up when the development of a custom sampling-ADC for the PANDA electromagnetic calorimeter (cf. [3] chapter 6.2) commenced. A preliminary 16-channel 14 bit@125 MS/s prototype has been evaluated, and first firmwares specifically designed for the Crystal Barrel Calorimeter were developed and tested. In 2014, the design sources of a subsequent 64-channel design (see fig. 2) with 14 bit@80 MS/s were offered for custom modification in a cooperation between the CBELSA/TAPS and PANDA collaborations.

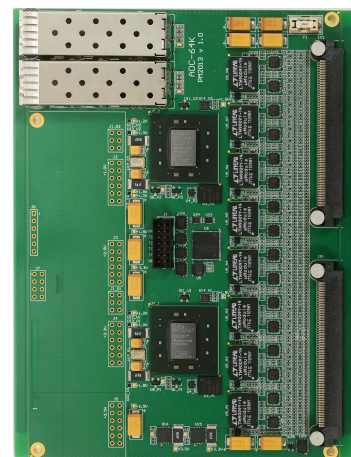


Figure 2: PANDA SADC prototype (2013).

### Technical Specifications of the Sampling-ADC

The core of the original PANDA design has only been changed insignificantly, hence the technical specifications are mostly valid for both designs. The analog data is buffered by low-power dual op-amps, offering the possibility to implement AC coupling, low-pass filtering, and dual-range routing. Signals are digitized by eight LINEAR TECHNOLOGIES LTM9009-11 (14 bit@80 MS/s) octal pipeline-ADCs, and transferred to two KINTEX 7 160T FPGAs with 320 MHz DDR data links. Each FPGA is connected to an SFP cage, supporting up to 5 GB/s link speed. A low-noise clock jitter cleaner with PLL generates clock signals for each ADC chip, as well as base clocks for the FPGAs and the transceivers. Through an arbitration circuit it is possible to lock the phase to the RX datapath of either transceiver. The board requires a separate power supply and consumes  $\approx 22$  W. Most voltages on the board pass through further high PSRR linear regulators; no residues of switching regulators were observed in the analyzed data.

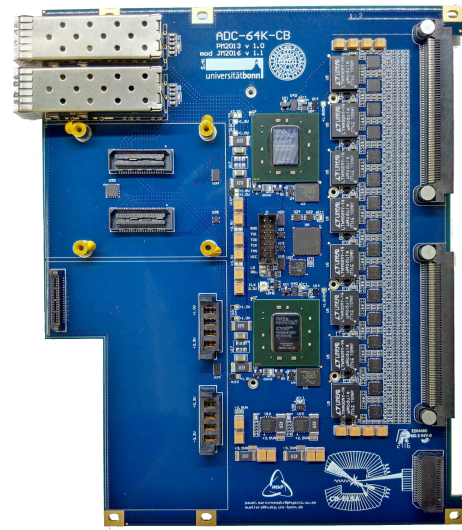


Figure 3: CB-SADC prototype (2016).

**Modifications of the Original Design** The form-factor of the CB-SADC (fig. 3,4) has been changed to fit in a NIM cassette with a low noise switching power supply, the analog input cards, and an interface for trigger/slowcontrol distribution. The power supply achieves a residual ripple of  $<3$  mV. It can be controlled using PMBUS, allowing monitoring and remote power cycling.

**Modular Analog Input Card** Signals enter through high-density 16-pair S/U/FTP cables using MRJ21-XG connectors. AC-coupling and low pass filters have been verified in SPICE and provide optimal shaping and anti-aliasing. I<sup>2</sup>C controllable pole-zero compensation and low-noise baseline-shifting allow for convenient calibrations and utilization of the full input range.

**Setup** For the readout of the whole calorimeter, two NIM crates will be equipped with 24 SADCs, yielding 1536 channels, enough for the maximum of 1380 signals from the calorimeter, as well as 60 fast energy-sum signals. The full dynamic range of each channel is 2.5 GeV with a detection threshold for pulses down to at least 1 MeV. The data is transferred from each SADC with two 1Gbit/s UDP/IP copper links to ethernet switches with 10Gbit/s uplinks. In the FPGA, de-randomizing event-buffers, as well as buffers for burst transfers of UDP packets, yield a very low dead time. Further event-buffering is done in conjunction with a Linux server system, which also acts as local event-builder for the DAQ.

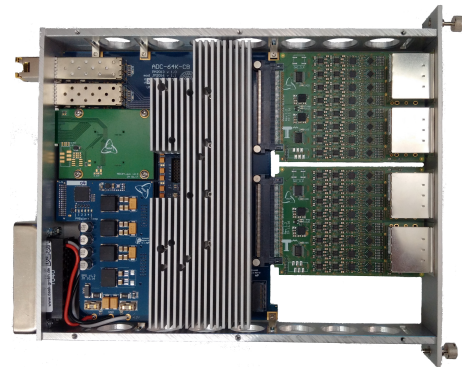


Figure 4: CB-SADC prototype in NIM cassette, with power supply, aluminum heatspreader, and analog input cards.



**Firmware** A custom firmware has been developed, based on the existing PANDA firmware for lab tests. As the frequency contributions of the processed CsI(Tl) scintillator crystal signals barely extends above 1MHz, it is by design oversampled by a factor of 40. This allows intensive decimation and digital filtering, leveraging FIR filters implemented in the DSP cores of the FPGA. The waveform data is further reduced by means of so-called feature-extraction algorithms: a digital constant fraction discriminator is used to generate timestamps with sub-sampling interpolation. A peak finding algorithm, as well as a fixed window integration, are used to determine the deposited energy. Algorithms for pile-up detection ensure the data quality. Further developments may even allow pile-up reconstruction with FPGA algorithms, until then, tagged events are analyzed offline.

**First Tests** A preliminary setup with 6 of 24 SADCs has been operated during test beamtimes in October 2016 and April/September 2017. The quality of the data has proven to be at least competitive to the existing QDC readout. Data analysis has shown the expected signatures of  $\pi^0$  and  $\eta$ -mesons. The possibility of the oscilloscope-like access to all signals has been valuable for detector diagnosis during the beamtimes. The readout-rate is limited mainly by the UDP/IP implementation and the necessary custom software-handshake to ensure data integrity. Still, a readout rate of more than 10 kHz has been obtained already, with room for further optimizations.

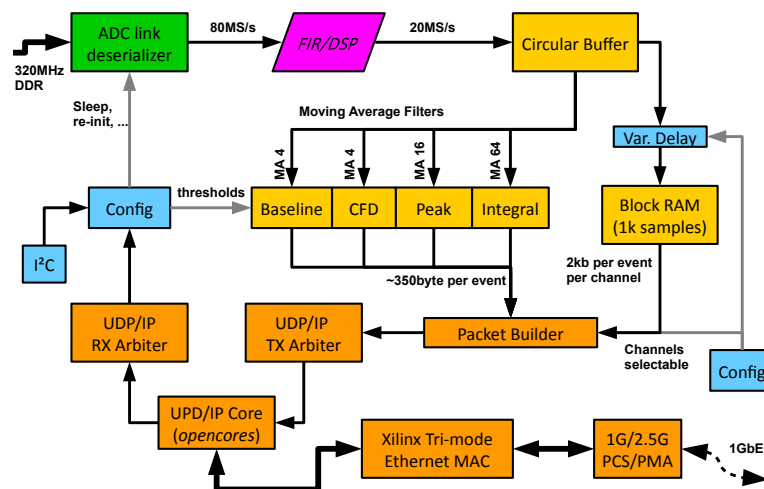


Figure 5: Structure of the UDP/IP-based firmware with feature-extraction.

**Acknowledgements** The speaker would like to thank Dr. Pawel Marciniewski, who is the developer of the PANDA SADC. His design sources and his constant support make this project possible.

## References

- [1] Hillert, W. *The Bonn Electron Stretcher Accelerator ELSA: Past and future*. European Physical Journal A(28):139-148 (2006)
- [2] M. Urban, Ch. Honisch, M. Steinacher. *The New APD Based Readout for the Crystal Barrel Calorimeter*. Journal of Physics: Conference Series, Volume 587, conference 1 (2015)
- [3] PANDA Collaboration. *PANDA TDR (Technical Design Report)*. [https://panda.gsi.de/oldwww/archive/public/panda\_tdr EMC.pdf] (2008)