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Monolithic Pixel Development in 180 nm CMOS for the Outer Pixel Layers in the ATLAS Experiment

T. Kugathasan*[a], R. Bates[c], C. Buttar[c], I. Berdalovic[a], B. Blochet[a], R. Cardella[a], M. Dalla[d], N. Egidos Plaja[a], T. Hemperek[b], J. W. van Hoorne[a], D. Maneuski[c], C. A. Marin Tobon[a], K. Moustakas[b], H. Mugnier[a], L. Musa[a], H. Pernegger[a], P. Riedler[a], C. Riegel[a,e], J. Rousset [a], C. Sbarra[d], D. Schaefer[a], E. J. Schioppa[a], A. Sharma[f], W. Snoeys[a], C. Solans Sanchez[a], T. Wang[b] and N. Wermes[b]

[a] *CERN Experimental Physics Department, CH-1211 Genève 23, Switzerland*
[b] *Physikalisches Institut, Rheinische Friedrich-Wilhelms Universität Bonn 53115 Bonn, Germany*
[c] *SUPA School of Physics and Astronomy, University of Glasgow Glasgow G12 8QQ, United Kingdom*
[d] *Università Bologna e INFN 40127 Bologna, Italy*
[e] *University of Wuppertal Gaußstraße 20, Wuppertal, Germany*
[f] *University of Oxford Oxford OX1 3PA, United Kingdom*

E-mail: thanushan.kugathasan@cern.ch

The ATLAS experiment at CERN plans to upgrade its Inner Tracking System for the High-Luminosity LHC in 2026. After the ALPIDE monolithic sensor for the ALICE ITS was successfully implemented in a 180 nm CMOS Imaging Sensor technology, the process was modified to combine full sensor depletion with a low sensor capacitance ($\approx$ 2.5fF), for increased radiation tolerance and low analog power consumption. Efficiency and charge collection time were measured with comparisons before and after irradiation. This paper summarises the measurements and the ATLAS-specific development towards full-reticle size CMOS sensors and modules in this modified technology.

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*Speaker.

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1. Introduction

The Inner Tracking system (ITk) of the ATLAS detector [1] will be upgraded in 2026 for the High-Luminosity Large Hadron Collider. Monolithic active pixel sensors (MAPS) are being proposed as an alternative to hybrid sensors for the outer layers of the ITk Pixel Detector. The reason is that MAPS can be produced in commercial CMOS technology and offer higher resolution and lower material budget in the vertex detector with a significant cost advantage with respect hybrid sensors. ALICE is the first experiment at the LHC implementing a large silicon tracker with MAPS [2]. The ALPIDE monolithic sensor implemented in a 180 nm CMOS Imaging Sensor technology features a high resistivity epi-layer (>1 kΩ·cm) with possibility to apply reverse bias (-6V). However, the sensor depletion volume is limited to the region around the collection electrode and signal charge generated outside the depleted area is still collected primarily by diffusion. The required tolerance to non-ionizing energy loss (NIEL) in the outer ATLAS pixel layers is 1.5×10^{15}1 MeV n_{eq}/cm^2, two orders of magnitude higher than the ALICE Inner Tracking System (ITS). This requires a drift field and hence depletion over the full sensitive layer to reduce charge collection time and reduce signal loss probability due to charge trapping. Moreover, a short charge collection time, combined with a fast front-end, is fundamental to separate hits from consecutive bunch crossings (25 ns).

2. Process modification for increased radiation tolerance

In the MAPS used for ALPIDE implementation [2] the charge generated by the energy deposition of an ionizing particle is collected by an n-well diode implemented on a high resistivity p-epitaxial layer with a typical thickness of about 25 μm. Both NMOS and PMOS transistors can be implemented in the pixel, as a deep-p-well shields all n-wells containing circuitry to avoid charge collection competition. The depletion starts at the junction of the collection electrode and expands into the p-epitaxial layer with increasing reverse bias. The lateral depletion under the deep-p-well is limited, as there is no potential gradient in the horizontal direction. For use in high radiation environments like the ATLAS ITk, a process modification to obtain full depletion has been developed in collaboration with the foundry [3], based on a low dose deep n-type implant in the epitaxial layer. In this case, the sensor junction is planar and extends over the full pixel width. Since depletion starts at the junction, it immediately extends over the full width of the pixel. By applying sufficient reverse substrate bias, the depletion will extend to the n-well collection electrode. This allows to obtain full depletion of the epitaxial layer and charge collection by drift, while maintaining a small collection electrode with a small sensing node capacitance ($\approx$ 2.5 fF), essential for a low power pixel design. The circuit layout is the same in both processes and this allows for direct comparison.

The Investigator chip is a sensor characterization device designed in the framework of the monolithic sensor development for ALICE ITS [4]. It implements 134 pixel sub-matrices of different pixel size and electrode geometry. Each sub-matrix contains 8 $\times$ 8 pixels surrounded by dummy pixels. All 64 pixels sensing nodes transient analog signals can be measured simultaneously. This allows for a detailed characterization of the charge collection time and signal amplitude. Investigator chips have been produced in the standard and modified process to study charge col-

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lection properties and detection efficiency at different radiation levels. Measurements have been performed on 20 μm $\times$ 20 μm and 50 μm $\times$ 50 μm pixels using ^{90}Sr source [5] [6]. Sensors produced in the standard process and irradiated with a fluence above 10^{14} 1 MeV n_{eq}/cm^2 show a large signal degradation, insufficient for a proper particle detection. Sensors produced in the modified process remained functional up to 10^{15} 1 MeV n_{eq}/cm^2, showing an improvement in tolerance to non-ionizing energy loss by at least an order of magnitude. Full depletion of the epitaxial layer is achieved and detection efficiency results from test beam are also promising.

3. Large scale demonstrators

The increased non-ionizing radiation tolerance for sensors manufactured using the modified process opened the way to the design of two large scale demonstrators to match ATLAS specifications for outer pixel layers: MALTA and TJ-Monopix. Both demonstrators implement a charge sensitive front-end with in-pixel discrimination which exploits the low sensor capacitance to reduce noise and analogue power. The demonstrators implement different readout architectures, with the common requirement to cope with the expected hit rate between 0.4 and 2 MHz/mm^2.

3.1 MALTA - High speed asynchronous matrix readout for ATLAS

The MALTA chip implements a novel asynchronous readout scheme to reduce digital power consumption and increase the hit rate capability in the matrix. The matrix contains 512×512 pixels with a 36.4 μm pitch. Figure 1 shows the pixel and the chip layout. The in-pixel circuit that performs amplification and discrimination is based on ALPIDE front-end [7]. The power consumption has been set to 1 μW to get a time response $<$ 20ns. This translates into a matrix analog power density $P_{analog} = 75\ mW/cm^2$. From parasitic extracted simulations the front end is expected to have an Equivalent Noise Charge of 7 e^-, with a threshold setting of 300 e^-. A channel-to-channel rms variation of 10 e^- is expected, and in-pixel threshold tuning is not needed.

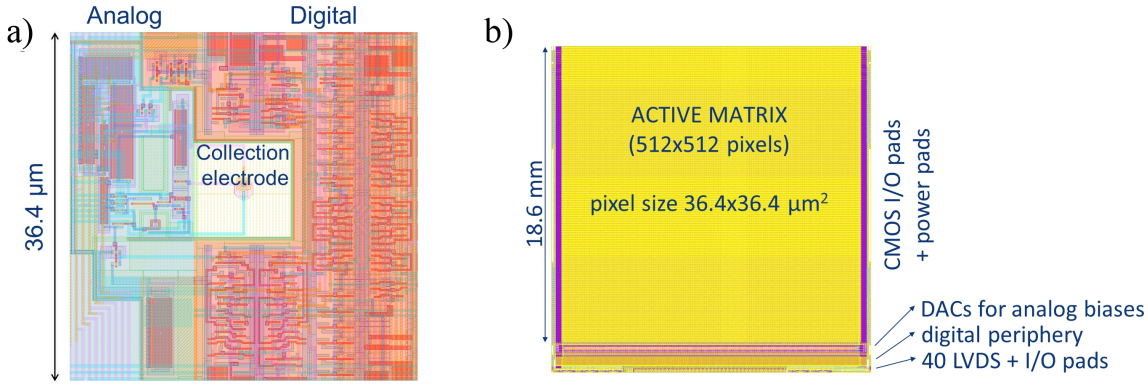

Figure 1: a) Pixel layout b) MALTA layout

The power to distribute a CMOS clock over the matrix can be calculated as $P_{clk} = N_{dc} \cdot E_{lt} \cdot f_c$. Where $N_{dc} = 137$ is the number of double columns in 1 cm, assuming one clock line per double column. $E_{lt} = 10.4\ pJ$ is toggle energy of 1 cm line at 1.8 V power supply. $f_c = 40\ MHz$ is the clock frequency synchronized to the bunch crossing. This results in $P_{clk} = 57\ mW/cm^2$, comparable to

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the analog power consumption $P_{analog} = 75mW/cm^2$. MALTA implements a fully asynchronous readout without clock distribution over the matrix. This allows a digital power reduction and removes the risks of crosstalk, as there is no continuous switching CMOS signal in the matrix. Each double column is subdivided into 64 pixel groups with 16 pixels. The 64 groups are subdivided in two sets of 32 groups, read out separately to minimise any hit loss due to simultaneous signals on the double column bus. The output of each pixel discriminator generates a hit signal pulse of programmable width (0.5 ns to 2 ns). Each of the 16 pixels in the group has a dedicated 1 bit output line to send the hit information, thus allowing for the hit pixel identification within a group. An additional 1 bit line, common to all pixels, is used as reference signal. The group address is encoded on a 5 bit bus with the same timing of the reference pulse. Table 1 reports the expected pixel hit rates and the equivalent matrix readout power. The hit rate values are for hybrid pixels, and are taken as an approximation by excess. Investigator chip measurements show that in our MAPS the average number of pixels hit for a particle hit is smaller than hybrid pixels [6]. The power per bit toggling is calculated assuming an address line toggle energy of 6.5 pJ/cm. The average bit toggling per pixel hit is 4.5 : 1 for the reference bit, 1 bit out of 16 bit for the pixel position and 2.5 bit on the 5 bit address bus. For the outer layers (2,3,4) the required read-out power is one order of magnitude lower than the power for the clock distribution over the matrix (P_{clk}).

	Pixel hit rate		Power/bit/cm^2 (H=2 cm)	Matrix readout power
Layer	hit/BC/mm^2	Mhit/mm^2	mW/cm^2	mW/cm^2
0	0.68	27.2	17.7	79.6
1	0.21	8.4	5.4	24.6
2	0.043	1.72	1.1	5.0
3	0.029	1.16	0.8	3.4
4	0.021	0.84	0.5	2.5

Table 1: Matrix hit rate and readout power for a column height H = 2 cm.

For each double column, hit information is transferred asynchronously to the periphery over two 22 bit address busses with the maximum latency of 5 ns. At the periphery a 2 bit time-stamp information is added to each hit signal for later processing. A merger circuit combines the information on two separate busses in to a single one. An arbitration circuit time-sorts the pulses, delaying one of the two signals if simultaneous, thus avoiding conflicts on the bus. The delay is encoded with additional 3 bits for later correction. The arbitration and merging process is repeated on 9 levels to merge the signals of all double-columns in a single data bus. This prototype does not implement on chip synchronization and serialization. The asynchronous hit signal is transmitted off chip on a 40 bit parallel bus, where each output is driven by a pseudo-LVDS driver. In case of a single serial output transmission the expected peak rate for the innermost layer would be 5 Gbps. In view of this, the pseudo-LVDS driver is designed to operate up to 5 Gbps with a maximum power consumption of 30 mW. MALTA also allows a chip-to-chip data transmission scheme. It has 40 CMOS receivers to get the data from the previous chip, a dedicated arbitration and merging layer to combine it with the signal of the local matrix and the possibility to send the data to the next chip via CMOS drivers. For this purpose 4 bits for chip identification are added to the hit information.

3.2 TJ-Monopix

The TJ-Monopix chip implements a synchronous readout scheme based on the well-established

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column drain readout architecture [8]. The chip size is ≈ 1 cm $\times$ 2 cm, it contains a pixel matrix of 224 $\times$ 448 pixels with a size of 36 μm $\times$ 40 μm. The pixel binary front-end is similar to the one implemented on MALTA. The main difference is that the front-end pulse duration is not clipped and the width of the digital pulse at the discriminator output (Time over Threshold), allows to obtain coarse analog information. A Gray counter running at 40 MHz generates the time stamp that is distributed over the matrix. The comparator leading edge and trailing edge time stamp are written into the two in-pixel RAM cells to record the hit time and pulse width. The pixel readout is based on a token propagation scheme, where the topmost pixel has the highest priority. The periphery circuit controls the readout, receives the matrix data and transmits it to the serial output link.

4. Summary

Monolithic pixel sensors are being considered as an alternative to hybrid pixel sensors for the outer layers of the ATLAS ITk Pixel Detector, where the expected hit rate is < 2 MHz/mm^2. A process modification of a 180 nm CMOS Imaging Sensor technology conserves the low sensor capacitance, but allows full depletion of the sensitive layer. Measurements confirmed an improvement in the radiation tolerance by at least an order of magnitude up to 10^{15} n_{eq}/cm^2. After this two large scale demonstrators were designed and submitted on a dedicated engineering run: MALTA contains a 512$\times$512 pixel matrix of 36.4 μm pitch featuring a 1 μW frontend with in-pixel discrimination based on ALPIDE. In simulation the time response is < 20 ns and the Equivalent Noise Charge is 7 e^-. A fully asynchronous readout without clock distribution over the matrix reduces digital power in the matrix below 10 mW/cm^2. The chip includes LVDS and CMOS drivers to transmit data respectively off-chip and between chips. TJ-Monopix uses a very similar front-end additionally providing Time over Threshold information, but it is based on the well-established synchronous column drain readout. The two chips will be characterized in early 2018.

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