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Developments of Two High-speed Dual-channel VCSEL Driver ASICs

Wei Zhou[1]

Department of Physics, Central China Normal University，Department of Physics, Southern Methodist University
Wuhan, Hubei 430079, P.R. China
E-mail: weizhou@smu.edu

Xiangming Sun[2]**, Le Xiao, Guangming Huang**
Department of Physics, Central China Normal University
Wuhan, Hubei 430079, P.R. China
E-mail: xmsun@phy.ccnu.edu.cn;lexiao@mails.ccnu.edu.cn;
gmhuang@phy.ccnu.edu.cn

Di Guo, Quan Sun, Datao Gong, Chonghan Liu, Tiankuan Liu, Jingbo Ye
Department of Physics, Southern Methodist University
Dallas, Texas 75275, USA
E-mail: dig@smu.edu;quans@smu.edu;dgong@smu.edu;kentl@smu.edu;
tliu@smu.edu;yejb@smu.edu

We present two designs of a dual-channel VCSEL driver ASIC, LOCld130 and LOCld65, for detector front-end readout via optical links. Each channel of the driver is designed to operate up to 5.12 Gbps or 14 Gbps respectively. They are implemented in commercial 130-nm and 65-nm CMOS technologies. Techniques that are adopted to extend the bandwidth are multiple stages, shared inductive peaking, active feedback and passive R-C. In the typical case the 5.12-Gbps driver dissipates 56 mW/channel (VCSEL included) and the 14-Gbps 58 mW/channel. LOCld65 will be tested in November 2017 and LOCld130 will be submitted for fabrication in the spring of 2018.

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[1]Speaker
[2]Corresponding Author

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1. Introduction

Optical link, a high speed data transmission system has been extensively used in readout systems of high energy physics experiments for decades, benefiting from its high bandwidth and low power consumption. Based on years of R&D, we have designed the dual-channel VCSEL driver, LOCld [1] in a commercial 250-nm Silicon-on-Sapphire CMOS technology as the baseline choice for the ATLAS Liquid-Argon-Calorimeter trigger upgrade [2], as shown in Figure 1. We design LOCld130 as a drop-in backup to LOCld in a commercial-130 nm CMOS technology. We also develop LOCld65 using the same 65-nm technology with which lpGBT [3] is being developed. lpGBT is the serializer-deserializer (SerDes) ASIC developed chiefly for detector upgrades for the HL-LHC. The serializer in lpGBT operates at 5.12 or 10.48 Gbps and the deserializer at 2.56 Gbps. While the predecessor of lpGBT, the GBTx SerDes has a matching optical transceiver (VTRx) developed through the Versatile Link (VL) common project, the optical module being investigated in the VL+ common project will be based on array optics with an array VCSEL driver that has a different driving mechanism and is not suitable for single channel transceivers. Both LOCld130 and LOCld65 are dual-channel VCSEL drivers, but each channel in the ASIC is individually powered, making them suitable for applications in dual-channel optical transmitters such as MTx and VTTx or in transceivers such as MTRx and VTRx [4]. LOCld65 is to provide a perfect match with to lpGBT when the application does not call for array optics, and to benefit from the current development of optical modules of MTx and VTTx.

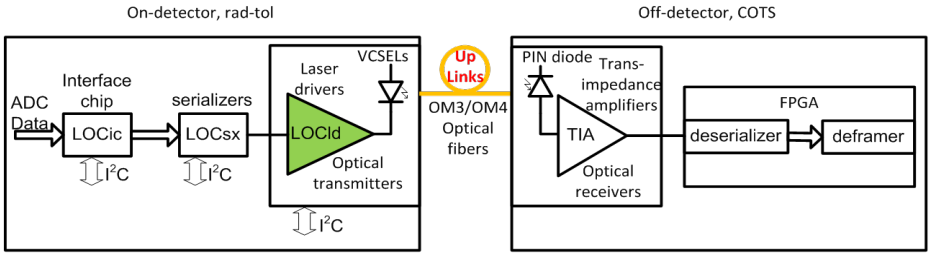


Figure 1: Optical link for the ATLAS liquid Argon calorimeter upgrade.

2. Designs

2.1 LOCld130

Although LOCld130 is a drop-in backup of LOCld, it has a simpler channel structure, lower power consumption, and fewer external interfaces. The analog core of LOCld130 has two parts: a two-stage limiting amplifier (LA) and a high-current differential driver. The minimum input signal to LOCld130 is 200 mV_{P-P} and the data rate is up to 5.12 Gbps. The power supply for LOCld130 is 1.5 V. We design the output signal of the LA with a swing of 1 V_{P-P}, 2/3 of the power supply voltage. This way the LA will fully steer the last stage bias current from one arm of the differential pair to the other one to maximize electro-optical efficiency. In the LA design shown in Figure 2, we choose a two-stage amplifier to optimize the gain as well as the bandwidth, and a 3.2-nH peaking inductor shared between the two stages, boosting the bandwidth of LA more than 3.5 GHz [5]. The bias current of each stage is 1.5 mA and 3 mA respectively. In the post-layout simulation, we use 1.5-nH inductors and a VCSEL equivalent

model [6] to simulate the bonding wires inductance and VCSEL. An eye diagram of the current to the laser, through the whole channel post-layout simulation with PRBS7 input, is shown in Figure 3.

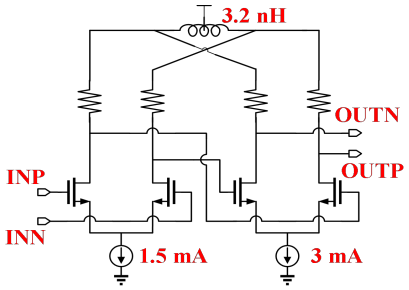


Figure 2: The schematic of the LA for LOCld130.

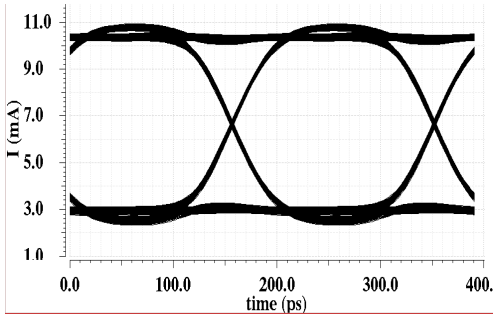


Figure 3: Typical eye diagram of LOCld130 at 5.12 Gpbs.

2.2 LOCld65

We also employ a full differential structure in LOCld65, similar to the design of LOCld130, as depicted in Figure 4. However LOCld65 is required to work under more rigorous conditions. The input signal is assumed to be 100 mV_{P-P}, and the data rate is 14 Gbps. In the design we also consider the high frequency loss in the input channel (PCB trace, bonding wire and the ESD diode). Shown in Figure 5(a), we design the first stage of the amplifier to be a continuous-time equalizer (CTLE) [7] to compensate the potential high-frequency signal loss. The peaking strength and the DC gain can be adjusted by tuning the resistor, depicted in Figure 6(a). We employ a four-stage LA as pre-driver shown in figure 5(b) [5]. Each of two successive gain cells shares one inductor to improve the bandwidth and to reduce chip area. The gain and bandwidth of the four-stage amplifier significantly depend on the process variation. For example, in the fast corner, the bandwidth of the amplifier is higher but the gain is smaller than typical case. To keep balance between the bandwidth and gain for all the process corner, we use an active-feedback-cell between the stages to adjust the gain and the bandwidth. By programming the feedback tail current, the total gain of the limiting amplifier is always greater than 18 dB and the bandwidth is higher than 10 GHz, depicted in Figure 6(b). The schematic of the output stage is shown in Figure 5(c). The output stage also employs the CTLE technique to compensate for channel loss. The amplifier's bias current is programmable with I^2C, offering a modulation current from 2 mA to 8 mA for the laser diode. Shown in Figure 7 is the eye diagram of the laser current, post-layout simulation with PRBS7 input.

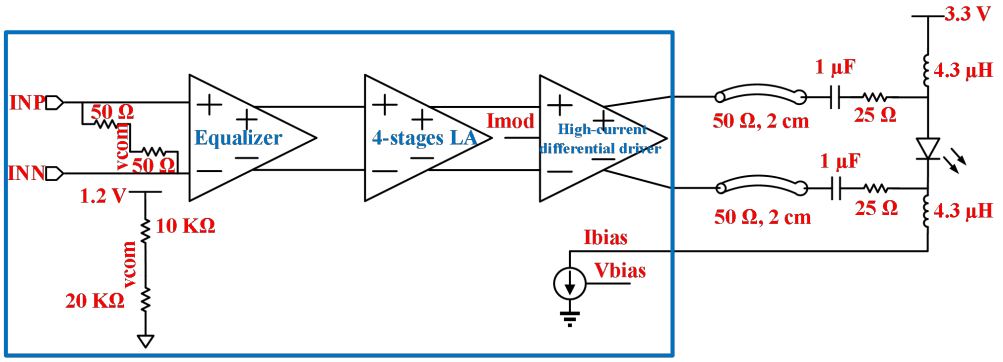
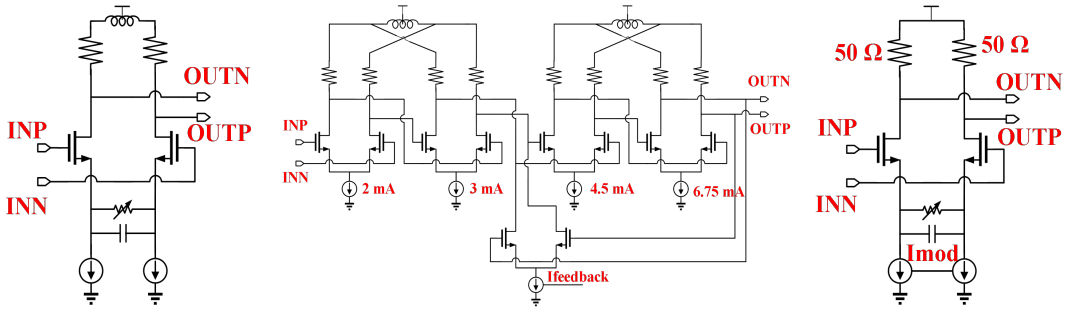
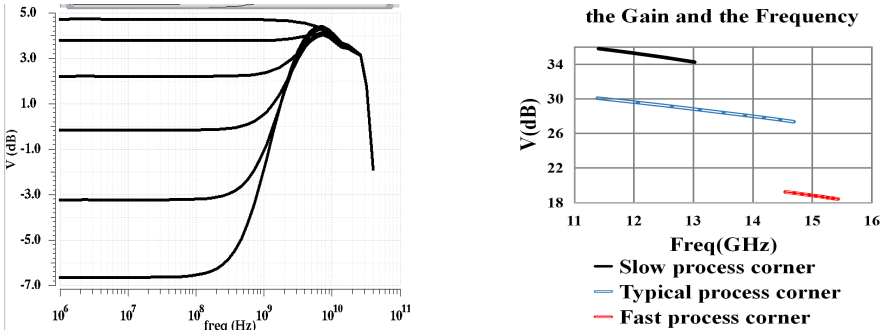


Figure 4: Block diagram of LOCld65 channel.



(a) CTLE (b) Four-stage LA (c) Output stage

Figure 5: The schematic of each part in LOCld65 channel.



(a) (b)

Figure 6: Simulated amplitude-frequency response curve of CTLE and four-stage LA.

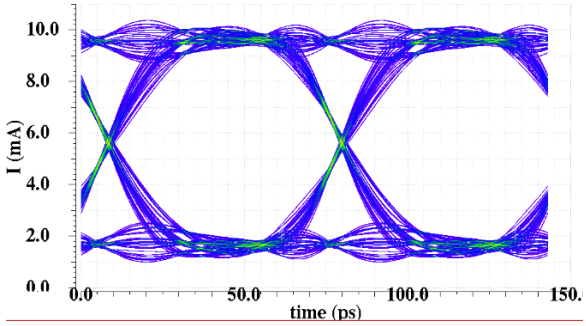


Figure 7: Typical eye diagram of LOCld65 at 14 Gpbs.

2.3 Conclusion

We designed two high-speed Dual-channel VCSEL Driver ASICs, LOCld130 and LOCld65, using commercial 130-nm and 65-nm CMOS processes. LOCld130 is a 5.12 Gbps VCSEL driver ASIC designed as a drop-in backup to LOCld. The total power consumption of LOCld130 is 112 mW (56 mW/channel) including the VCSELs. LOCld65 runs at 14 Gbps with a power consumption of 116 mW (58 mW/channel), VCSEL included. LOCld65 was submitted for fabrication in May 20th 2017. We expect to start the evaluation of this ASIC in November 2017. We also plan to submit LOCld130 for fabrication in the spring of 2018.

Acknowledgments

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