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Characterization Measurement Results of MuTRiG - A Silicon Photomultiplier Readout ASIC with High Timing Precision and High Event Rate Capability

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The MuTRiG chip, which is dedicated to the Mu3e experiment, is a 32 channels mixed-signal Silicon Photomultiplier readout ASIC with high timing precision and high event rate capability designed and fabricated in UMC 180 nm CMOS technology. It combines the excellent timing performance of the fully differential analog front-ends and the 50 ps time binning TDCs with a high event rate capability from a dedicated on-chip digital logic circuit and a gigabit LVDS serial data link. The design of the chip and the results from the characterization measurements will be presented.

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1. Introduction

Mu3e experiment [1] is a novel experiment searching for charged lepton flavour violating decay of $\mu \to eee$ with a sensitivity of $< 10^{-16}$. In order to detect the signal with the desired sensitivity, the background has to be suppressed to a level below 10^{-16}, which requires a good momentum, vertex and timing resolution from the detectors. Additionally, in order to observe 1×10^{17} muon decays in a measurement time of around one year, the experiment will be running at a muon stopping rate of more than 10^9 Hz, putting another challenge to the detectors and electronics.

The Mu3e detector in the phase I configuration is shown in Fig. 1. It comprises of the tracking detector and the timing detector. The tracking detector is made up of four silicon pixel layers around the target in the center station and two silicon pixel layers in both upstream and downstream re-curl stations. The silicon pixel layers are built from High-Voltage Monolithic Active Pixel Sensors (HV-MAPS) [2], providing excellent vertex and momentum measurements. The timing detector consists of the scintillating fibre detector [3] in the center station and the scintillating tile detector [4] in the re-curl stations. Silicon Photomultiplier (SiPM) is used as photon sensor in both timing detector systems. The timing detector adds precise timing information to the reconstructed tracks. A good timing resolution of 500 ps (σ) and 100 ps (σ) is required for the scintillating fibre detector and the scintillating tile detector respectively. In addition, a high event rate up to 1 MHz per SiPM channel is expected for the scintillating fibre detector.

MuTRiG is a 32 channels mixed-signal SiPM readout Application Specific Integrated Circuit (ASIC) designed and fabricated in in UMC 180 nm CMOS technology. It's developed for precise timing and high event rate applications and dedicated to the readout of the Mu3e fibre detector and the Mu3e tile detector to achieve the required timing resolution and in the same time to sustain the high event rate in the scintillating fibre detector.

2. MuTRiG ASIC Description

The diagram of one MuTRiG channel is shown in Fig 2. The front-end (FE) part of each channel is designed in a fully differential structure to suppress the common-mode noise from both outside sources and the digital activities on the chip. The input signals taken by the input stage of the channel are discriminated by two different thresholds in two branches: a low threshold for the time of arrival information using leading edge discrimination and a high threshold for energy

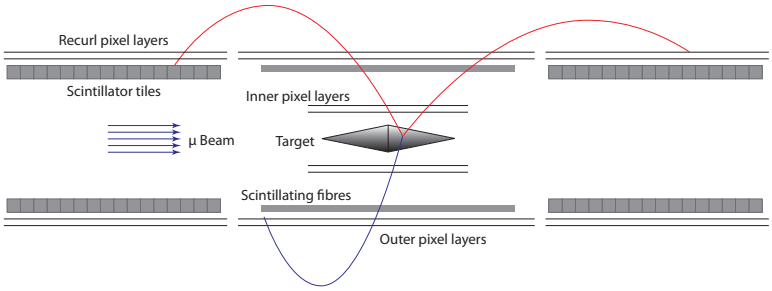

Figure 1: Schematic of Mu3e detector system in the phase I configuration. The electron and two positron tracks from a typical signal are shown as the blue and red curves.[1]

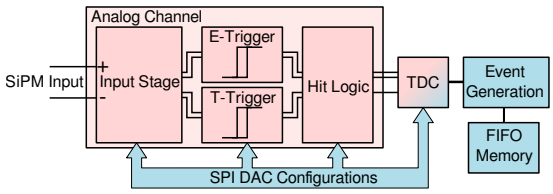

Figure 2: Channel diagram of the MuTRiG chip.

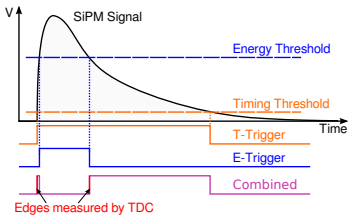

Figure 3: Trigger principle of the MuTRiG front-end.[5]

information based on a linearized Time-over-Threshold (ToT) method. As shown in Fig. 3, the time of arrival and the energy information are encoded into two rising edges of a combined signal in the hit logic unit.

The rising edges of the combined signal are digitized by the TDC on each channel. The TDC module was developed at ZITI Heidelberg and has been implemented in PETA [6] and STiC [7] ASICs. All the TDC channels obtain the common time stamps from a global time base unit, where a Phase Lock Loop (PLL) locks a 16-stage Voltage Controlled Oscillator (VCO) to a 625 MHz external reference clock. The output of the VCO drives a 15 bit counter implemented by Linear Feedback Shift Register (LFSR), providing coarse counter values with time binning of 1.6 ns. Each coarse counter bin is subdivided by 32 possible VCO states into 50 ps fine counter bins. The TDC channel records the coarse counter value and the states of the VCO as the time stamp data for each rising edge of the mentioned combined signal.

The time stamps of the two rising edges for the same event are combined into one event data with the on-chip digital logic circuit. The event data from all the channels are buffered and sent out in frames via a 1.25 Gbps Low-Voltage Differential Signaling (LVDS) serial data link. An external 625 MHz clock is used for the serial data link and for generating the 125 MHz system clock. 8b/10b encoding is also implemented to keep the DC-balance of the LVDS link. In order to increase the event rate capability of the MuTRiG chip, the output event structure can be switched from the standard event structure of 48 bits, with which both time stamps of an event will be sent out, to a short event structure of 27 bits, where only the time stamp of the arrival time information and 1 bit energy flag of the event will be sent out.

3. Characterization Measurement Results

The front-end jitter has been measured by charge injection over a 33 pF capacitor. The jitter of the time difference between the marker signal from the arbitrary waveform generator and the MuTRiG timing trigger signal is measured using a high bandwidth oscilloscope. As shown in Fig. 4, jitter as a function of the injected charge is evaluated for 5 different cases, where the following conditions are applied consecutively: 1) Only front-end part of the chip is active; 2) FPGA is connected, but no clock is generated for the MuTRiG chip; 3) PLL reference clock for TDCs on the MuTRiG chip is generated, but the PLL is powered off; 4) Power on the on chip PLL; 5) The serial data link clock is generated. For the front-end-only case, the obtained time jitter is < 20 ps for charges > 350 fC ($\sim$charge of single-photon event for a 2×10^6 gain SiPM). The jitter increases by connecting FPGA and generating clocks for the chip. Especially the generation of the

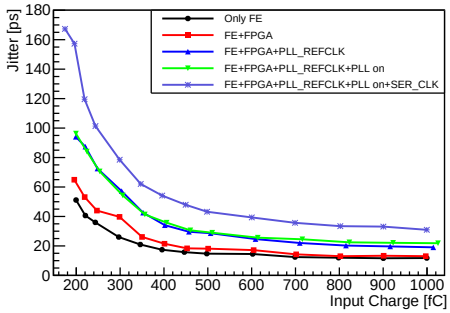

Figure 4: MuTRiG front-end jitter measurement result by injecting charge over a 33 pF capacitor.

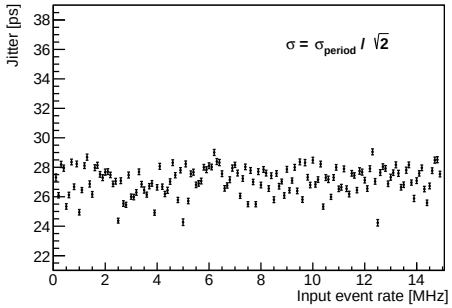

Figure 5: MuTRiG Full chain jitter measurement result for input signal up to 15 MHz.

PLL reference clock and serial data link clock has big impact to the jitter performance. While the jitter stays almost unchanged by turning on the on-chip PLL, indicating that the degradation of the timing performance mainly come from the PCB design, not from the digital activities on the chip. In total the front-end jitter increases by ~ 20 ps for ~ 1 pC input signals.

MuTRiG full chain jitter is characterized by measuring the period jitter of the input pulses with the front-end, TDC and the digital part of the chip. The input charges are 1 pC and the timing threshold has been optimized for these inputs. Since the period is the subtraction of two measured time stamps with the same jitter, the full chain timing jitter is calculated by the standard deviation of the measured periods divided by $\sqrt{2}$. A full chain timing jitter of < 30 ps is measured for input signal up to 15 MHz and no degradation due to input event rate is observed, as shown in Fig. 5.

The event rate limit of the chip is measured by injecting test pulses to multiple channels and measuring the output event rate for a serial data link bit rate of 1.25 Gbps. Fig. 6 shows the event rate measurement results for the standard (left) and short (right) event structure configurations. For the standard event structure configuration of 48 bits, the output event rate is limited to 20.24 MHz (on average 632 kHz/channel) by the bit rate of the serial data link. The maximum event rate for the 27 bits short event configuration is 25 MHz (781 kHz/channel), $1/5$ of the system clock frequency (125 MHz). The bottleneck comes from the on-chip digital logic circuit, which needs 5 system clock cycles to process a hit event. In the next tape-out the digital logic circuit will be improved and the maximum event rate is expected to be ~ 35 MHz (~ 1.1 MHz/channel), limited by the bit rate of the data link.

The Bit Error Rate (BER) of the serial data link is measured for a bit rate of 1.25 Gbps. The data frames are filled with Pseudo-Random Bit Sequence (PRBS) patterns in the measurements. The PRBS patterns and Cyclic Redundancy Check (CRC) information of each data frame are checked at FPGA. No error is detected for a running time of more than 37 hours, giving a BER upper limit of 5.9×10^{-15}.

4. Conclusion

This paper presents the characterization measurement results of the MuTRiG chip, which is a 32-channel mixed-signal SiPM readout ASIC with high timing precision and high event rate capability.

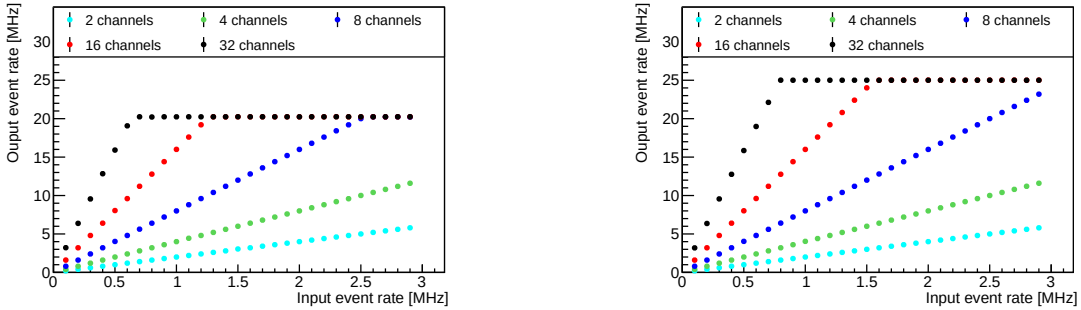

Figure 6: Event rate capability measurement results for standard output event structure configuration (left) and short output event structure configuration (right).

The front-end jitter is measured by injecting charge over a 33 pF capacitor. A < 20 ps jitter has been obtained for input charges > 350 fC. Mainly due to the design of the PCB used in the measurements, a degradation of ~ 20 ps for 1 pC signals has been observed when the readout FPGA is connected and both the PLL reference clock and the serial data link clock are sent to the chip.

The full chain jitter has been characterized by measuring the period jitter of the input signals. A jitter of < 30 ps has been obtained for input signal frequency up to 15 MHz. No degradation due to high input rate is observed.

For the serial data link rate of 1.25 Gbps, the maximum event rate of the chip is 20.24 MHz (on average 632 kHz/channel) for the standard event structure configuration. For the short event structure configuration, the output event rate of the chip is limited to 25 MHz (781 kHz/channel), $1/5$ of the system clock, due to the bottleneck from the on-chip digital logic circuit. The digital logic circuit will be improved in the next tape-out and the maximum event rate is expected to be ~ 35 MHz (~ 1.1 MHz/channel).

The BER of the serial data link is measured to be $< 5.90 \times 10^{-15}$ for the bit rate of 1.25 Gbps.

References

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