PROCEEDINGS OF SCIENCE

"ALTIROC0, a 20 pico-second time resolution ASIC for the ATLAS High Granularity Timing Detector (HGTD)"

C. de La Taille[1]
OMEGA/CNRS/Ecole Polytechnique
Ecole Polytechnique - Drahi-X Novation Center
Avenue Coriolis
91128 PALAISEAU CEDEX
FRANCE
E-mail: taille@in2p3.fr

Other Authors

S. Callier, S. Conforti, P. Dinaucourt, G. Martin-Chassard, N. Seguin-Moreau
OMEGA/CNRS/Ecole Polytechnique
E-mail: nsmoreau@in2p3.fr

C. Agapopoulou, N. Makovec, L. Serin, S. Simion
LAL/CNRS/Université Paris Sud
Laboratoire de l'Accélérateur Linéaire (LAL)
Université Paris-Sud
91405 ORSAY CEDEX
FRANCE
E-mail: serin@lal.in2p3.fr

ALTIROC0 is an 8-channel ASIC prototype designed to readout 1x1 or 2x2 mm^2 50 µm thick Low Gain Avalanche Diodes (LGAD) of the ATLAS High Granularity Timing Detector (HGTD). The targeted combined time resolution of the sensor and the readout electronics is 30 ps for one MIP. Each analog channel of the ASIC must exhibit an extremely low jitter to ensure this challenging time resolution, while keeping a low power consumption of 2 mW/channel. A "Time Over Threshold" and a "Constant Fraction Discriminator" architecture are integrated to correct for the time walk.
Test bench measurements performed on the ASIC received in April 2017 are presented.

Topical Workshop on Electronics for Particle Physics
11 - 14 September 2017
Santa Cruz, California

[1]Speaker

PoS(TWEPP-17)006

1. Introduction

The expected increase of the pile-up at the high luminosity phase of the LHC due to the 200 interactions per bunch crossing will have a severe impact on the physics [1]. A High Granularity Timing Detector (HGTD) is proposed in front of the ATLAS Liquid Argon End-Cap calorimeters for pile-up mitigation especially for jets and electron isolation. Four layers of very thin Low Gain Avalanche Diodes (LGAD), with a pad size of 1.3 x 1.3 mm^2, are foreseen. This detector is expected to provide a precise timing information for charged particles with a time resolution of about 30 pico-seconds for one MIP, combining the 4 layers after irradiation. It will also be used to provide a luminosity measurement at 40 MHz by counting the number of hits.

The sensors will be read-out by a dedicated front-end ASIC called ALTIROC (ATLAS LGAD Timing Integrated Read-Out Chip), that will be bump-bonded on the sensors. A first prototype comprising only the analog part of this ASIC has been designed in CMOS 130 nm technology to cope with the high radiation and time resolution requirements, while keeping a power dissipation lower than 2 mW/pixel for a complete readout channel.

2. ALTIROC0 architecture

2.1 ASIC requirements

The requirements of the final ASIC (ALTIROC) are listed in Table 1.

Pad size	***1.3 x 1.3 mm²***
Detector capacitance	***3.4 pF***
TID and neutron fluence	Inner region: **4.5 MGy, 4.5 x 10 ¹⁵ n/cm²** Outer region: **2.1 MGy, 4.0 x 10 ¹⁵ n/cm²**
Number of channels/ASIC	**225**
Minimum threshold	**5 fC (=0.5 MIP at LGAD gain = 20)**
Dynamic range	20 MIPs
Preamplifier-Discri jitter at Gain=20	**< 20 ps**
Time Walk contribution	**< 10 ps**
TDC bin	20 ps (TOA) and 40 ps (TOT)
TDC range	2.5 ns (TOA) and 9 ns (TOT)
Number of bits/hit	7 for TOA and 9 for TOT
Luminosity counters per ASIC	7 bits (sum) + 5 bits (outside window)
Total power per area (ASIC)	**< 200 mW/cm² (< 800 mW)**
elink driver bandwidth	320 Mb/s, 640 Mb/s and 1.28 Gb/s

Table 1: ALTIROC final ASIC requirements

In particular, the ASIC must withstand high radiation levels with a maximum TID of 4.5 MGy at small radius and neutron fluence of 4.5 x 10^{15} n/cm^2. The inner part of the detector, from r=120 mm to 300mm, is expected to be changed at half lifetime of the HL-LHC. Each channel will read out 1.3x1.3 mm^2 sensor pads, corresponding to a detector capacitance of 3.4 pF. The targeted time resolution is 30 ps *rms* for one MIP with 4 layers after irradiation. To

achieve such a performance, the jitter must be better than 20 ps in order to be smaller than the dispersion due to the Landau fluctuation in the energy deposit, which limits the time resolution to 25 ps. As for the time walk contribution, it must be corrected with an accuracy leading to a residual contribution better than 10 ps *rms* for signals ranging from 1 MIP to 10-20 MIPs, which corresponds to 10 to 100-200 fC with an LGAD gain equal to 20. The power dissipation of a complete pixel readout must be limited to 2 mW, split in 1 mW for the analog part and 1 mW for the Time to Digital Convertors (TDC) and digital processing.

2.2 Analog front end of ALTIROC0

ALTIROC0 is a first ASIC prototype designed in CMOS 130 nm that integrates only the analog front end, made of a broadband preamplifier followed by a discriminator (Figure 1).

The jitter due to electronics noise is given by the rise time divided by the signal to noise ratio. To obtain high speed, the input preamplifier is built around a common source configuration. It was optimized for a 2 pF detector capacitance corresponding to an earlier 1 x 1 mm^2 sensor prototype. Its bandwidth is tunable between 300 MHz and 500 MHz using a variable pole capacitance and its noise has been minimized to 1.2 nV/√Hz at 200 uA drain current to ensure a large Signal over Noise ratio and therefore a jitter smaller than 20 ps *rms*.

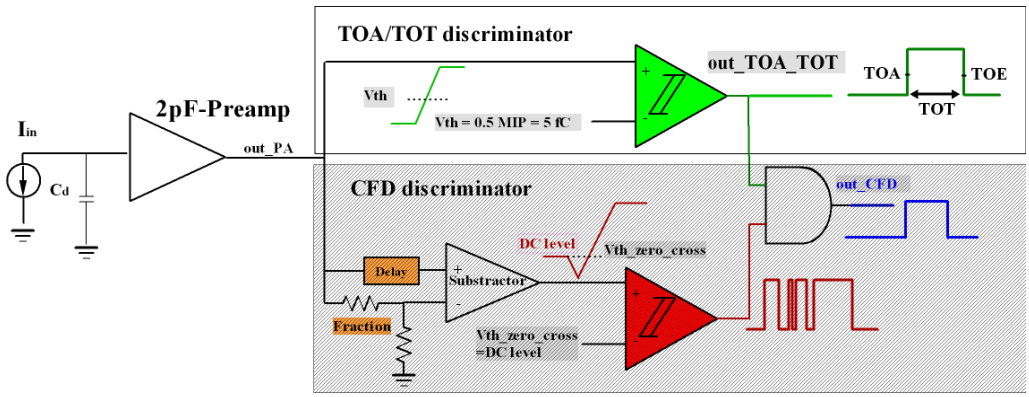

Figure 1: ALTIROC0 Front End synoptic

Two time-walk correction architectures, both built around leading edge discriminators, have been integrated to correct for the Time Walk of approximately 1 ns :

- A Time Over Threshold (TOT) architecture, that enables offline time walk correction using the width of the discriminator (TOT), which is proportional to the amplitude
- A Constant Fraction Discriminator (CFD), which is in theory insensitive to the amplitude variations if the pulse shape remains constant and so, allowing online time walk correction.

The chip area is 3.4 mm x 3.4 mm to enable its bump-bonding to an array of 2x2 channels with four 1 x 1 mm^2 LGAD sensor pixels.

3. ALTIROC0 measurements

3.1 ALTIROC0 prototype

This first ASIC prototype integrates four channels to readout four 1x1 mm^2 LGAD pixels. The dies were received in April 2017. A testboard has been designed to allow measurements of either an ASIC alone, wire bonded on the printed circuit board, or a flip chip made of an ASIC bump-bonded to a 4 pixel sensor.

3.2 ALTIROC0 jitter measurements

Only the TOT architecture was tested so far (Figure 1). The rising edge of the discriminator corresponds to the Time Of Arrival (TOA). Its position and its jitter were measured for input charges ranging from 8 fC up to 160 fC with a threshold set at 5 fC. Various capacitors (Cd) were soldered on the test board to simulate the sensor. A parasitic capacitance, estimated to 1.3 pF, should actually be added to the soldered detector capacitance, which corresponds to the capacitance of the preamp input protection diode (≈ 0.7 pF) and to the capacitance of the printed circuit board line (≈ 0.6 pF) that connects the input preamp to the detector capacitor foot print. Figure 2 shows the results with a 2 pF detector capacitor as it corresponds to the expected capacitance of a 1x1 mm^2 LGAD pixel. The rise time of the preamplifier has been estimated by measuring the time walk. To do so, the position of the TOA has been measured for input charges going from 8 fC up to 160 fC. The time walk amounts to 1 ns, corresponding to a preamp bandwidth of 450 MHz that is in good agreement with post layout simulations.

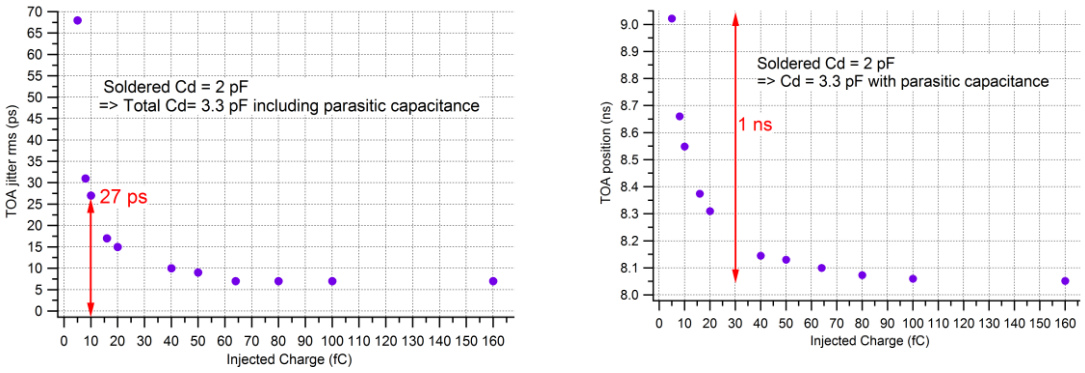

Figure 2: TOA jitter rms and position vs the injected charge with Cd=2 pF (actual Cd=3.3 pF)

Table 2 summarizes the jitter performance obtained for an injected charge of 10 fC (corresponding to 1 MIP) and for various detector capacitors. The threshold was set at 5 fC. As expected, the measured jitter scales almost linearly with the capacitance. In particular, the jitter measured when a 2 pF capacitor is soldered on the test board is 27 ps, which is slightly larger than the requirement, but this could certainly be improved by increasing the current in the preamp to reduce the noise.

Cd	Actual Cd	Jitter @ 10 fC
0 pF	1.3 pF	14 ps
1 pF	2.3 pF	20 ps
2 pF	3.3 pF	27 ps
3 pF	4.3 pF	40 ps

Table 2: jitter for various Cd

The measured power consumption of the preamp and of the discriminator is respectively 440 µW and 360 µW, which meets the requirement of a power consumption of less than 1 mW/channel.

Test beam measurements were performed at CERN mid-September using this test board and an ALTIROC0 ASIC bump-bonded to a four 1 x 1 mm^2 LGAD sensor. Data analysis is ongoing and first results are quite promising

4. Conclusion

Test bench measurements of ALTIROC0 show a jitter better than 30 ps *rms* for an actual detector capacitance of 3.4 pF and an injected charge of 10 fC corresponding to 1 MIP with an LGAD gain of 20. The power consumption of the analog part is 800 µW, which is smaller than the requirement of 1 mW/channel. A next version of the ASIC, ALTIROC1, with 16 or 25 complete readout channels, is foreseen. Each channel will integrate the front end followed by two 20 ps-bin Time-to-Digital-Converters for the TOT and TOA digitization and a memory to store the data.

5. Acknowledgement

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

6. References

[1] : ATLAS Phase-II Upgrade Scoping Document, CERN-LHCC-2015-020. LHCC-G-166, CERN, 2015, https://cds.cern.ch/record/2055248