PROCEEDINGS OF SCIENCE

Development of a Large Pixel Chip Demonstrator in RD53 for ATLAS and CMS Upgrades

Elia Conti* **on behalf of the RD53 Collaboration**†
CERN
E-mail: elia.conti@cern.ch

RD53A is a large scale 65 nm CMOS pixel demonstrator chip that has been developed by the RD53 collaboration for very high rate (3 GHz/cm^2) and very high radiation levels (500 Mrad, possibly 1 Grad) for ATLAS and CMS phase 2 upgrades. It features serial powering operation and design variations in the analog and digital pixel matrix for different testing purposes. The design and verification of RD53A are described together with an outline of the plans to develop final pixel chips for the two experiments.

Topical Workshop on Electronics for Particle Physics
11 - 14 September 2017
Santa Cruz, California

*Speaker.

†The RD53 Collaboration:

M.B.Barbero[a], D.Fougeron[a], S.Godiot[a], M.Menouni[a], P.Pangaud[a], A.Rozanov[a], P.Breugnon[a], M.Bomben[b], G.Calderini[b], F.Crescioli[b], O.Le Dortz[b], G.Marchiori[b], D.Dzahini[c], F.E.Rarbi[c], R.Gaglione[d], T.Hemperek[e], F.Hügging[e], H.Krüger[e], P.Rymaszewski[e], M.Vogt[e], T.Wang[e], N.Wermes[e], M.Karagounis[f], F.Ciciriello[g], F.Corsi[g], C.Marzocca[g], G.De Robertis[h], F.Loddo[h], F.Licciulli[h], A.Andreazza[i], V.Liberali[i], A.Stabile[i], L.Frontini[i], N.Bacchetta[j], M.Bagatin[j,k], D.Bisello[j,k], S.Gerardin[j,k], S.Mattiazzo[j,k], A.Paccagnella[j,k], D.Vogrig[j,k], S.Bonaldo[j,k], F.De Canio[l], L.Gaioni[l], M.Manghisoni[l], V.Re[l], E.Riceputi[l], G.Traversi[l], L.Ratti[m], C.Vacchi[m], K.Androsov[n], R.Beccherle[n], G.Magazzu[n], M.Minuti[n], F.Morsani[n], F.Palla[n], S.Poulios[n], G.M.Bilei[o], M.Menichelli[o], P.Placidi[o,p], S.Marconi[o,p,x], G. Dellacasa[q], N.Demaria[q], G.Mazza[q], A.Rivetti[q], M.D.Da Rocha Rolo[q], E.Monteil[q], L.Pacher[q], A.Paternò[q,r], D.Gajanana[s], V.Gromov[s], B.van Eijk[s], R.Kluit[s], A.Vitkovskiy[s], T.Benka[t], M.Havranek[t], Z.Janoska[t], M.Marcisovsky[t], G.Neue[t], L.Tomasek[t], V.Kafka[u], V.Vrba[u], I.Vila[v], E.M.S.Jimenez[v], E.Lopez-Morillo[w], F.R.Palomo[w], F.Muñoz[w], D.Abbaneo[x], J.Christiansen[x], S.Orfanelli[x], L.M.Jara Casas[x], E.Conti[x], S.Bell[y], M.L.Prydderch[y], S.Thomas[y], D.C.Christian[z], G.Deptuch[z], F.Fahim[z], J.Hoff[z], T.Zimmermann[z], S.Miryala[z], M.Garcia-Sciveres[z1], D.Gnani[z1], A.Krieger[z1], K.Papadopoulou[z1], T.Heim[z1], R.Carney[z1], B.Nachman[z1], C.Renteira[z1], V.Wallangen[z1], M.Hoeferkamp[z2], S.Seidel[z2].

a) *Aix Marseille Université, CNRS/IN2P3, CPPM, Marseille, France*; b) *Laboratoire de Physique Nucléaire et de Hautes Energies (LPNHE) Paris, France*; c) *Laboratoire de Physique Subatomique et de Cosmologie (LPSC), Grenoble, France*; d) *Laboratoire d'Annecy-le-Vieux de Physique des Particules (LAPP), Annecy-le-Vieux, France*; e) *Physikalisches Institut, Bonn, Germany*; f) *Fachhochschule Dortmund, Germany*; g) *Politecnico di Bari, Italy*; h) *INFN Sezione di Bari, Italy*; i) *INFN Sezione di Milano and Università degli Studi di Milano, Italy*; j) *INFN Sezione di Padova, Italy*; k) *Università di Padova, Italy*; l) *INFN Sezione di Pavia and Università di Bergamo, Italy*; m) *INFN Sezione di Pavia and Università di Pavia, Italy*; n) *INFN Sezione di Pisa, Italy*; o) *INFN Sezione di Perugia, Italy*; p) *Department of Engineering, Università di Perugia, Italy*; q) *INFN Sezione di Torino, Italy*; r) *Politecnico of Torino, Italy*; s) *National Institute for Subatomic Physics (NIKHEF), Amsterdam, Netherlands*; t) *Faculty of Nuclear Sciences and Physical Engineering of the Czech Technical University (FNSPE-CTU)*; u) *Institute of Physics of the Academy of Sciences of the Czech Republic (IP-ASCR)*; v) *Instituto de Fisica de Cantabria (IFCA, CSIC-UC), Santander, Spain*; w) *Electronic Engineering Dept, School of Engineering, Sevilla University, Spain*; x) *European Organization for Nuclear Research (CERN), Geneva, Switzerland*; y) *Science and Technology Facilities Council, Rutherford Appleton Laboratory, Chilton, Didcot, United Kingdom*; z) *Fermi National Accelerator Laboratory (FNAL), Batavia, USA*; z1) *Lawrence Berkeley National Laboratory (LBNL), Berkeley, USA*; z2) *University of New Mexico (UNM), Albuquerque, USA*;

PoS(TWEPP-17)005

1. Introduction

The next generation of hybrid pixel detectors for the phase-2 upgrade of ATLAS and CMS experiments at HL-HLC (planned for 2024-26) sets unprecedented design requirements, including high granularity (small pixels with either 50×50 or 25×100 μm^2), large chips (∼2×2 cm^2), high occupancy, with a corresponding estimated 3 GHz/cm^2 hit rate, and extreme radiation tolerance up to 1 Grad of Total Ionizing Dose (TID). The RD53 collaboration addresses these issues by proposing a 65 nm baseline technology. The main activities of the collaboration over the years have included *i)* an extensive radiation testing aimed to determine how best to obtain sufficient radiation hardness [1, 2], *ii)* the development of tools and methodology for efficiently designing large complex mixed signal chips, *iii)* the implementation and test of various test structures, building blocks (Intellectual Properties, IPs) and small pixel arrays and *iv)* the design and characterization of a full scale demonstrator pixel chip, called RD53A, which is the object of the presented work.

2. Specifications and floorplan

As shown in Table 1, the goal of the RD53A chip is to demonstrate in a large format integrated circuit the suitability of the chosen 65 nm technology for the HL-LHC upgrades of ATLAS and CMS in terms of radiation tolerance, stable low threshold operation and high hit and trigger rate capabilities. RD53A is not intended to be a final production chip for use by the experiments, as it contains design variations for testing purposes, making the pixel matrix non-uniform. It is, however, meant to form the basis for their design, as it is intended to be easily scalable and tailored according to the experiment specifications.

Figure 1 (a) reports the chip floorplan. RD53A has a size of 20×11.8 mm^2 and is fabricated on a shared engineering wafer run. The sensitive area of the chip consists of an array of 192×400 pixels of 50×50 μm^2. The periphery is placed at the bottom of the chip and contains all the global circuitry needed for biasing, configuration, monitoring and readout: all the analog building blocks are contained in a macroblock called Analog Chip Bottom and are surrounded by all the synthesized logic blocks, grouped in the Digital Chip Bottom. The wire bonding pads are organized as a single row at the bottom chip edge.

RD53A is designed to operate with serial powering, that has been identified as a viable scheme to supply the inner tracker with the required power within an acceptable material budget and power losses in cables. For supporting such an operation special voltage regulators called Shunt-LDOs [3] are used, which combine a Low Drop-Out linear voltage regulator with a shunt regulator.

Table 1: Main specifications of RD53A chip.

Specification	Value	Comments
Hit rate	3 GHz/cm^2	-
Trigger rate	1 MHz max	-
Trigger latency	12.5 μs	-
Hit loss	$\leq$ 1%	at max hit rate
Detection threshold	< 600 e$^-$	-
In-time threshold	< 1200 e$^-$	-
Radiation tolerance (TID)	500 Mrad (1×10^{16} 1 Mev eq. n/cm^2)	replacement after ∼5 years operation
Radiation tolerance (SEU)	< 0.05/h/chip	at 1.5 GHz/cm^2 particle flux

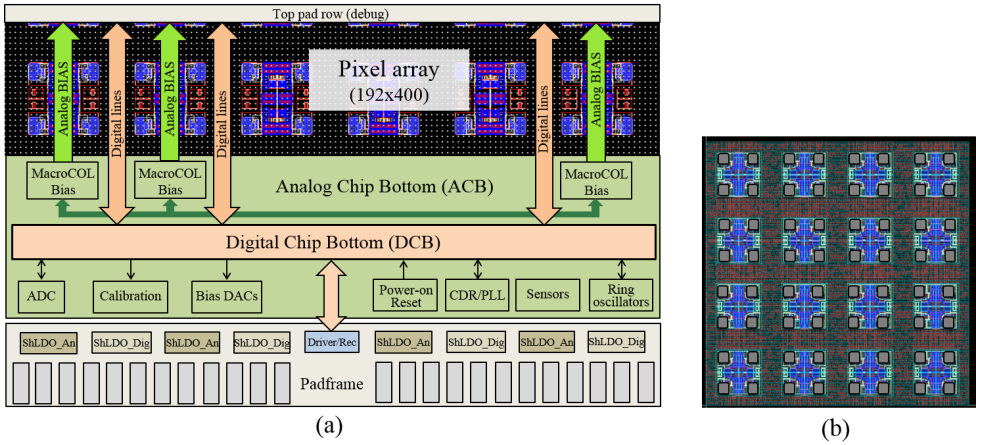

Figure 1: (a) RD53A floorplan, functional view; (b) Pixel core floorplan.

3. Pixel Matrix

The RD53A pixel matrix is built up of cores of 8×8 pixels. As shown in Figure 1 (b), the floorplan of the pixels within a core is such that the analog front ends (FEs) of groups of four pixels are placed next to each other, forming so called analog quads or analog islands; each quad is then surrounded by digital synthesized logic.

RD53A contains three different analog FE designs allowing for detailed performance comparison (Figure 2): the Differential FE uses a differential gain stage in front of the discriminator and implements a threshold by unbalancing the two branches; the Linear FE implements a linear pulse amplification in front of the discriminator, which compares the pulse to a threshold voltage; the Synchronous FE uses a baseline auto-zeroing scheme that requires periodic acquisition of a baseline instead of pixel-by-pixel threshold trimming. Common to all FEs is the calibration injection circuit, which allows both to generate two consecutive signals of same polarity and to inject different charges in neighboring pixels at same time. The designs feature same layout area and bump bond pads, making them easily interchangeable on the pixel matrix layout. The bias distribution follows the same organization for all three FE flavors.

The digital logic in a core is synthesized as one single circuit and handles all processing of the binary outputs, including masking, digital injection, Time over Threshold (ToT) counting, storage of ToT values, latency timing, triggering and readout. Each core contains multiple pixel regions, which share data buffering logic. This section has been optimized extensively: digital buffering architectures at behavioral and RTL level have been simulated using a dedicated environment called VEPIX53 [4], which was also reused for extensive functional verification. The environment supports the injection of both internally generated, realistic-looking clusters of hits at the HL-LHC rates and physics Monte Carlo data.

Two different, optimized readout architectures have been implemented in RD53A for the pixel regions, featuring comparable performance: the Centralized Buffering Architecture (CBA) and Distributed Buffering Architecture (DBA). The former features a pixel region size of 4×4 pixels, while the latter is 1×4. In both cases, hit time information is stored by region; ToT information, on the other hand, is stored by pixel in the DBA, while in the CBA there is a shared memory.

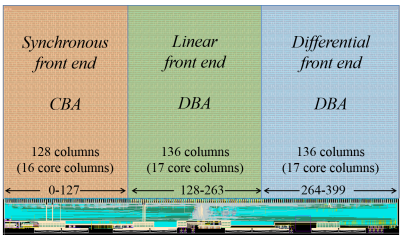

Figure 2: Arrangement of analog FE flavors and digital buffering architectures in RD53A layout.

4. Chip Periphery

The Digital Chip Bottom (schematized in Figure 3) contains all the blocks in charge of control and processing and consists of high level description code synthesized together during top level integration. RD53A is fully controlled with a serial 160 Mbps input stream using a custom protocol, which encodes clock and commands on a single link. The protocol consists of a continuous stream of 16-bit frames, is DC-balanced with short run length and has built-in framing and error detection. All pixel data, configuration data and messages are output on 1 to 4 parallel lanes (programmable) at 1.28 Gbps nominal bandwidth. The encoding used is the Xilinx Aurora 64b/66b protocol.

Global configuration registers are synthesized in the Digital Chip Bottom, featuring 9-bit address and 16-bit data, and are protected from Single Event Upsets (SEUs) using triple modular redundancy. Each pixel, on the other hand, contains up to 8 local configuration bits implemented with standard latches; long term SEU protection is obtained through trickle configuration, i.e. all configuration can be refreshed during operation by continually writing data in between triggers.

The Analog Chip Bottom contains all analog IPs, is assembled in analog environment and simulated with analog and mixed-signal simulator. It provides current reference to DACs, global analog FE bias, calibration circuit voltage levels and it also monitors temperature, total dose, currents/voltages in different parts of the chip by means of a 12-bit ADC. All the analog building blocks, including the FEs, were previously simulated using a dedicated radiation simulation model, prototyped, tested and characterized in radiation environment at least up to 500 Mrad TID [5].

5. Functional Verification

As mentioned in Section 3, the functional verification of RD53A has taken place using the VEPIX53 environment, which puts into practice some of the advanced features provided by SystemVerilog and the Universal Verification Methodology (UVM) library such as the generation of constrained-random inputs, output prediction, automatic checking and coverage collection.

The adopted approach for the functional verification of RD53A consists of both constrained-random and directed testing. The former is based on the generation of inputs, either internal or from Monte Carlo data, in agreement with the HL-LHC operating conditions, and was applied mainly for verifying the triggered hit data path, from the pixel array to the Aurora output. The latter instead was used for addressing single specific functions in the chip periphery.

For the final debug of the chip, regressions containing a set of the most relevant functional tests were run at both Register Transfer Level (RTL) and gate level at every design iteration until receiving an all-pass result.

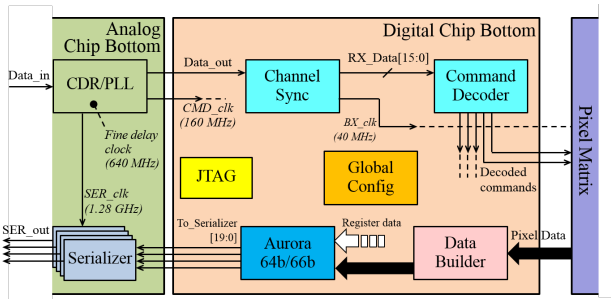

Figure 3: Block diagram of RD53A digital chip bottom.

6. Conclusion

The goal of the RD53A chip is to demonstrate the feasibility of 65 nm technology with respect to the challenging requirements set by the future HL-LHC experiment upgrades. The guidelines elaborated by RD53 over the years (radiation tolerance, digital architecture, floorplan, serial powering, verification) have been put into practice for the chip design using the developed, prototyped and tested IP library. This results in the co-existence on the same chip of different analog FE flavors and digital pixel array architectures. RD53A has been submitted on a shared engineering run with expected delivery in November 2017; the preparation for chip testing is ongoing.

The RD53 Collaboration has formally proposed to make the final ATLAS and CMS pixel readout chips. The future developments related to them include the selection of a single analog FE variant, an increase of the pixel array size and the inclusion of additional functionality according to experiment specifications. Further optimizations, finally, will be done with respect to power consumption, digital architecture, and SEU immunity.

References

[1] F. Faccio, S. Michelis, D. Cornale, A. Paccagnella, S. Gerardin, *Radiation-induced short channel (RISCE) and narrow channel (RINCE) effects in 65 and 130 nm MOSFETs*, IEEE Trans. Nucl. Sci., vol. 62, no.6, pp. 2933-2940, (2015).

[2] L.M. Jara Casas et al., *Characterization of radiation effects in 65 nm digital circuits with the DRAD digital radiation test chip*, Journal of Instrumentation, vol. 12, no. 02, p. C02039 (2017).

[3] S. Marconi, S. Orfanelli, M. Karagounis, T. Hemperek, J. Christiansen, P. Placidi, *Advanced power analysis methodology targeted to the optimization of a digital pixel readout chip design and its critical serial powering system*, Journal of Instrumentation, vol. 12, no. 02, p. C02017 (2017).

[4] S. Marconi, E. Conti, P. Placidi, J. Christiansen, T. Hemperek, *The RD53 Collaboration's SystemVerilog-UVM Simulation Framework and its General Applicability to Design of Advanced Pixel Readout Chips*, Journal of Instrumentation, vol. 9, no. 10, p. P10005 (2014).

[5] L. Pacher et al., *Results from CHIPIX-FE0, a Small-Scale Prototype of a New Generation Pixel Readout ASIC in 65 nm CMOS for HL-LHC*, Proceeding of the 2017 Topical Workshop on Electronics for Particle Physics (TWEPP). To be published at *http://pos.sissa.it/*