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LHCb vertex locator upgrade: front-end electronics and firmware.

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The LHCb Experiment will be upgraded to a trigger-less system reading out the full detector at 40 MHz event rate with all selection algorithms executed in a CPU farm. The upgraded Vertex Locator (VELO) will be a hybrid pixel detector read out by the "VeloPix" ASIC with on-chip zero-suppression. The upgrade of the LHCb experiment will be installed during the shut-down LS2 of LHC in 2019-2020. It will transform the experiment into a trigger-less system reading out the full detector at 40 MHz event rate. The VELO surrounding the interaction region is used to reconstruct primary and secondary decay vertices and measure the flight distance of long-lived particles. The highest occupancy ASICs will have pixel-hit rates above 900 Mhit/s and produce an output data rate of over 15 Gbit/s, adding up to 2.9 Tbit/s of data for the 41 M pixels of the whole VELO.

This poster presents the architecture and design of the VELO on-detector electronics, describing each component and its relation to the LHCb common frame. The main components are: the VeloPix ASIC at 5 mm from the beam in a secondary vacuum tank and exposed to an extremely high inhomogeneous radiation environment, the Opto- and Power Board (OPB) outside of the vacuum, but still in a high radiation environment, the LHCb readout (TELL40) and front-end control (SOL40) boards, placed in a radiation free environment. The whole system is currently being integrated, validated and tested. The results and experience gained from these test are presented.

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1. LHCb upgrade

LHCb [1] is an experiment dedicated to search for new physics by studying CP violation and rare decays of b and c quarks.
The upgrade of the LHCb experiment, planned for 2019, will enable the detector to run at luminosities greater than $2 \times 10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and explore New Physics effects in the beauty and charm sector with unprecedented precision. To achieve this, the entire readout will be transformed into a triggerless system operating at 40 MHz, where the event selection algorithms will be executed by high-level software in the CPU farm.

2. VELO Upgrade

The upgraded silicon vertex detector (VELO) [2] must be lightweight, radiation hard, vacuum compatible, and has to drive data out with a maximum throughput of 5 Tbit/s. This challenge will be met with a new VELO design based on hybrid silicon pixel detectors, positioned within 5 mm of the LHC colliding beams. The sensors have 55 μm square pixels as well as the VeloPix ASIC, which is being developed for the readout based on the Timepix/Medipix family of chips. The hottest ASIC will have to cope with integrated hit rates of up to 900 MHz which translates to a bandwidth of more than 15 Gbit/s. Work has been done to optimize the sensor guard ring design to cope with the irradiation levels, which are highly non-uniform and reach 8e15 MeV $\mathrm{n_{eq}}/\mathrm{cm}^2$ at the innermost region. The material budget is optimized with the use of evaporative CO_2 coolant circulating in microchannels within a thin silicon substrate. Some of the most important challenges of VELO upgrade are listed below:

- 41M pixels on 624 VeloPix ASICs, arranged on 208 silicon sensor tiles and 52 modules.
- Active area of $0.12\,\mathrm{m}^2$ with a pixel resolution of 55 $\mu\mathrm{m}^2$
- Trigger-less data driven binary readout at 40 MHz with an output of $\sim$2.9 Tbit/s.
- 4 MGy of highly non uniform radiation with a sensor high voltage tolerance of 1000V.

3. VELO on-detector electronics

VELO upgrade will require 52 stations as described in Figure 1. Each one is composed of a VELO module 3.1, Flex tapes 3.2, Vacuum Feedthrough 3.3 and Opto-Power Board 3.4

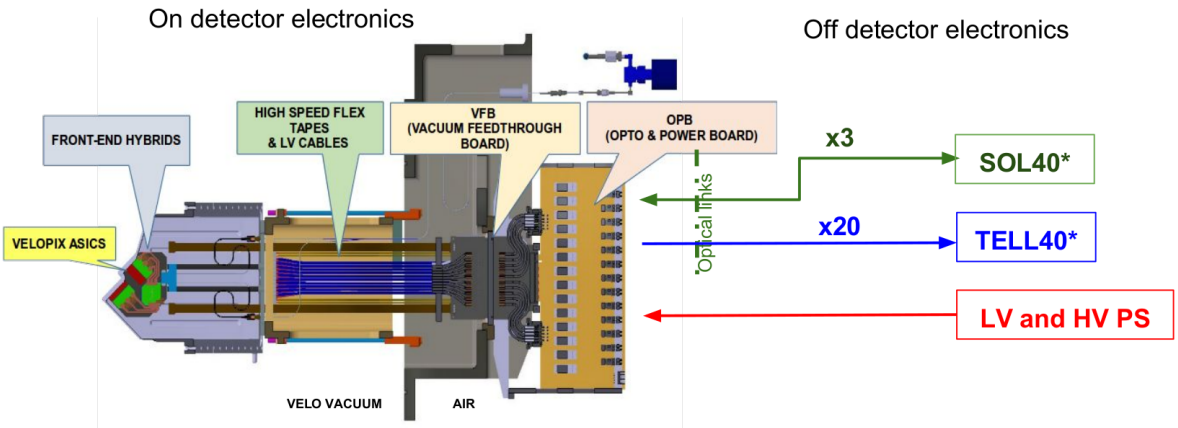

Figure 1: LHCb VELO electronics overview

3.1 VELO module

The module concept consists of a carbon-fibre structure supporting a silicon microchannel substrate. Stress-relieved CO_2 cooling pipes route the CO_2 to and from the cooling connector which is soldered to the silicon substrate. The module has four silicon sensors, read out by and bump-bonded to twelve VeloPix ASICs. The ASICs are glued directly onto the microchannel substrate. Discrete electronics, including a GBTX chip [3] for slow control, along with power, bias and readout circuitry will be arranged on a kapton hybrid. When the VELO is closed, the sensors of opposing detector halves form a diamond shape with the beam passing through the center (see figure 3.1).

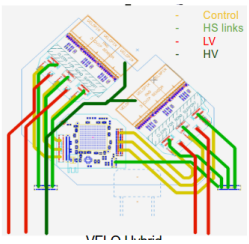

Figure 2: VELO Hybrid

A module of the upgraded VELO is composed of 2 hybrids (see Figure 3.1), as the one shown below, one per side of the silicon substrate.

- 2 VELO tiles (silicon sensors bump bonded to a row of 3 VeloPix ASICs, see Table 1).
- 1 GBTX board, which controls 6 VeloPix ASICs directly from the e-ports.

20 high speed links come out of VELO module using VELO Gigabit Wireline Transceiver (GWT) serialiser at 5.12 Gbit/s. This serialiser has been specifically designed for VELO in order to reduce the power consumption of VeloPix ASICs.

VeloPix ASIC specifications
Technology 130 nm CMOS produced in TSMC foundry
256×256 pixels with pixel size of 55×55 μm^2
Radiation hardness: 4 MGy. Triplicated voting registers
Low power consumption < 1 W/cm^2
Hit peak rate of 900 MHits/s/ASIC
Binary data driven readout at 40 MHz
Maximun output data rate of 20.48 Gbit/s

Table 1: VeloPix ASIC

3.2 Flex tapes

Two different flex tapes of 56 cm have been produced, at CERN and industry, and successfully tested.

- The industrial tape has 180 µm traces, 200 µm gap and it is made of 175 thick µ m Pyralux AP plus dielectric.
- The CERN tape is similar but with identical trace and gap sizes 200 µm.

The first measurements of those tapes gives as a result that the two tapes have similar transmission losses, but the characteristic impedance is around 20% lower on the CERN one.

3.3 Vacuum feedthrough

The Vacuum Feedthrough Board (VFB) is responsible for bringing the electrical connection in and out of the vacuum tank, such as: High speed control and readout signals, analog monitoring signals and high and low voltage power supplies.

3.4 Opto Power Board

The Opto Power Board (OPB) is connected to the VFB outside the vacuum tank. It is responsible for distributing the low voltage power supply over the ASICs and acting as a link between electrical signals of the fron-end and the optical fibers of the back-end electronics.

4. VELO off-detector electronics

The LHCb upgrade uses a common board for all the off-detector electronics. The board, called PCIe40, is based on the Altera Arria 10 FPGA and the role of the boards in the experiment (SOL40 or TELL40) are determined only by the programmed firmware. For testing purposes the different functionalities are combined into a single system called MiniDaq. A LHCb-wide firmware framework has been stablised for common development while each subdetector is in charge of their specific functionalities. The first version of MiniDaq has been used to test first subdetector prototypes.

- The SOL40 boards distribute control signals to the front-end chips and is in charge of keeping the whole experiment synchronous. As a single SOL40 provides a maximun of 48 control links, a total of 4 SOL40 boards are needed for controlling the 156 links of the whole VELO. The LHCb common SOL40 common firmware was modified in order to cope with the VELO requirements, controling the VeloPix ASICs directly from the GBTX e-ports.
- The TELL40 boards are responsible for the high speed data acquisition with a maximum data rate of 100 Gbit/s, making it possible to read out a complete VELO module with 20 GWT links. Therefore a total amount of 52 TELL40 boards will be needed for VELO upgrade. The LHCb common TELL40 firmware had to be almost completely redesigned in order to comply with the VELO requirements: specific data transmission protocol (GWT isntead of GBT) and arrival of data out of time order.

5. Testing of electronics for VELO upgrade

Two different setups, with different testing purposes are being used for validating VELO upgrade hardware. The SPIDR setup, widely used to test TimePix/MediPix family ASICs, is devoted to characterise the heart of the VELO detector, the VeloPix ASIC and consist of a carrier board + Xilinx VC707 evaluation board. The system provides a basic readout without the LHCb specific data formating. In parallel to SPIDR system, the actual LHCb VELO daq system is being developed. This MiniDAQ, based on a prototype of the final FPGA and DAQ board, is currently used to validate the different components of the final readout chain described on sections 3 and 4.

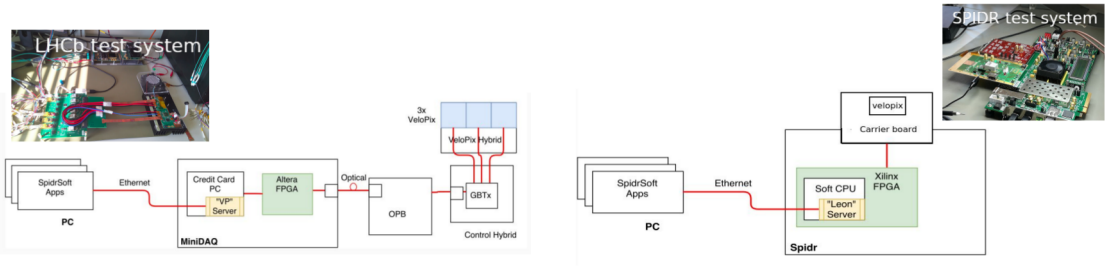

Figure 3: LHCb test system vs SPIDR system

5.1 VeloPix ASIC

A first version of the VeloPix has been produced in July 2016 and thoroughly tested since then, providing input for a second version already produced and under test now. The digital and analog functionalities have been validated according to specifications at room and operational temperatures -40 °C. The chip was successfully operated with Total Ionizing Dose (TID) up to 4 MGy. No change in digital power consumption was observed, nor a drift in analog parameters like thresholds, noise or DAC values. What we found in the first version and will be corrected in the second one:

- An excess of jitter on the GWT high speed serial link increase the data transmission error rate.
- Single Event Latch-up (SEL) and Single Event Upsets (SEU) in the line receiver of the reset pin were found at heavy ion beam tests.

5.2 High speed links

VELO front-end electronics uses two different protocols for the high speed links, CERN standard GBT and VELO specific GWT.

- Front-end GBT links are used for the slow control (ECS) and timing and fast control (TFC) of a hybrid @ 4.8 Gbit/s. In order to allow the electrical signal to travel along the OPB + VFB + 50 cm flex cable, CERN standard GBLD (GigaBit Laser Driver) ASIC is being used as a line driver giving good quality signal at the end of the path. However a Continuous Time Linear Equalizer (CTLE) will be implemented on the receiving end of the links to further improve the quality of the signal.
- The GWT links have been tested with output patterns like Pseudo-Random Binary Sequence (PRBS15, PRBS31) and scrambled data. The observed excess jitter on the clock in the VeloPix ASIC in combination with the frequency dependent attenuation of the flex cables causes the eye diagrams to close, thereby giving rise to a too high Bit Error Rate (BER). By introducing a CTLE circuit, the BER can be improved from 1e-7 to 1e-15.

5.3 VELO on-detector electronics verification

Off-detector and on-detector electronic prototypes are currently under test. In order to facilitate the VELO hardware validation we migrated the well stablished SPIDR communication libraries to the MiniDAQ system. The VELO TELL40 firmware was thoroughly simulated and can be implemented in the MiniDAQ. Currently one full VELO slide is under test using VELO SOL40 firmware and very soon using as well the VELO TELL40 firmware.

6. Summary and Outlook

The on-detector electronics of the VELO upgraded have been successfully validated, and a pre-series of module production started. In parallel, we are working on the data acquisition firmware, with the purpose of getting data from VeloPix ASIC via MiniDAQ. Last but not least, all the off-detector firmware is being migrated from the test FPGA (MiniDAQ1) to final one.

7. Acknowledgements

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