PROCEEDINGS OF SCIENCE

The VeloPix ASIC test results

Edgar Lemos Cid[1], Pablo Vazquez Regueiro on behalf of the LHCb Collaboration
Universidade de Santiago de Compostela
Dpto de Fisica de Particulas, Facultade de Fisica, Calle Xosé María Suárez Núñez, s/n. Campus Vida,C.P.: 15782, Santiago de Compostela, A Coruña, Spain
E-mail: edgar.lemos@usc.es

LHCb is a dedicated experiment searching for new physics by studying CP violation and rare decays of b and c quarks. The LHCb silicon vertex detector (VELO) is a crucial component of the experiment. The detector provides precision space points close to the interaction point and thus used to reconstruct b decay vertices, in both the trigger and offline track reconstruction as well as being an important part of the tracking system. In order to match the upgraded LHCb readout system, which aims at a trigger-free read-out of the entire detector at the bunch-crossing rate of 40 MHz, all silicon modules and electronics must be replaced. The upgraded VELO will be a hybrid pixel detector (55x55 um pitch), read out by the VeloPix ASIC derived from the Timepix3. The sensors and ASICs will approach the interaction point to within 5.1 mm and be exposed to a radiation dose of up to 370 Mrad. The hottest ASICs must sustain pixel hit rates of more than 900 Mhits/s and produce an output data rate of over 15 Gbit/s, adding up to 2.8 Tbit/s of data for the whole VELO.

This paper will present an overview of the tests performed on the first version of the VeloPix, issues found and solutions. All digital and analogue functionality has been validated and conforms to specifications. Low temperature operation was verified and tests with a probecard were successful. Total Ionising Dose irradiations have been carried out with irradiation up to 400 Mrad which resulted in no change in digital power consumption and no drift in analogue parameters. Two test beams have been carried out. One to cross-check the synchronization, high rate capabilities and tracking performance using 5 VeloPix planes in a telescope at rates up to 300 Mtracks/s. Another one for time-walk studies using the Timepix3 telescope. Jitter on the clock that is used for the 4.8 Gbits/s serialiser generates erroneous packets, which can be reduced by adding decoupling outside of the chip and tuning the internal clock phase. Four sessions of Single Event Effects testing have been carried out in the Heavy ion facility in Louvain-la-Neuve. We found unexpected Single Event Latch-up (SEL), large cross section for the reset circuit and some small design flaws. To solve/mitigate SEE and jitter issues a second version of the VeloPix will be submitted. This poster will describe the architecture of the VeloPix chip, the test results and design changes that have been implemented.

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1. Introduction

VeloPix is the main part of the new VELO detector. This new detector will have 624 application-specific integrated circuits (Velopix ASICs) connected to 208 silicon sensors in 26 detector planes, having 41 Mpixels in total and producing a peak data rate of 2.8 Tbit/s. The VeloPix design and development have been explained in [1-2].

This paper presents the main test performed for the VeloPix during a long campain in the end of 2016 and in the year 2017. Moreover, the problems of the VeloPix one have been analized and solved. New VeloPix two has been send to production with this improvements and now it is been tested.

2. Measurement system

Most of the measurement tests have been carried out with the Speedy PIxel Detector Readout (SPIDR)-readout system, figure 1. This system uses a vc707 evaluation board which firmware has been development in Nikhef for the Medipix and Timepix family. Moreover, it uses a comercial 4 port SFP board and a custom VeloPix carried board designed and mounted in the University of Santiago de Compostela. This system is capable of operate and power a single VeloPix. It could readout the VeloPix at full speed of 20.48 Gbps with the four Velopix GWT links active.

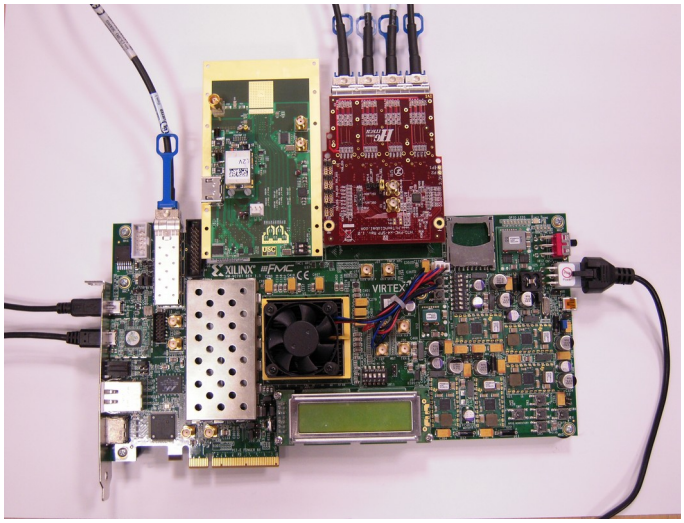

Figure 1: VeloPix readout system.

3. Analog and digital funtionality test

First of all, we had power up the velopix and checked that the power consumption corresponds with the design value. Then, we got and set the diferent registers of the VeloPix. After that, we scanned all the DAC and we carried out a thershold scan and a noise scan [3]. So, all the digital and analoge funtionallity has been validated. Moreover, we have validated the chip at low temperature (-40 ºC) and we carried out the first test in the wafer probe card; now, it is used for the Velopix two testing, figure 2.

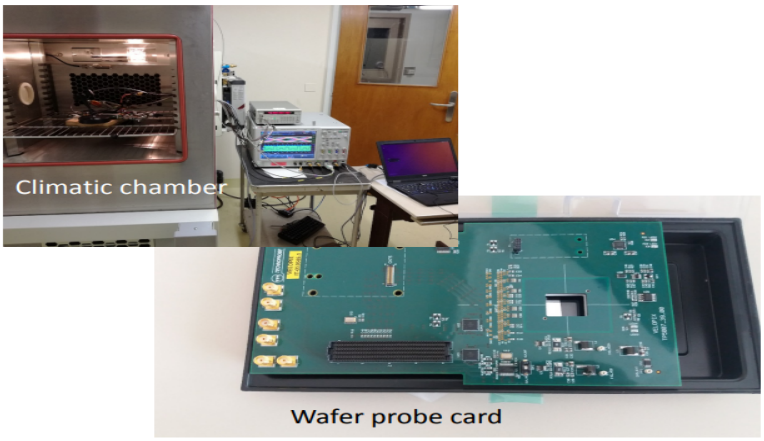

Figure 2: Climatic chamber and wafer probe card.

4. High Speed Test

One of the main challenges and improvements of the VeloPix from the Timepix 3 is the habity of reading up to 900 Mhits/s. This has been implemented using a GWT serializer [4]. During the test campain, we have found out an excesive jitter on this GWT due the too much cycle-to-cycle period variation of the internal 320 MHz. This jitter depends on power distribution around the chip and if the matrix is on or off, figure 3. The rate can be lowered (to almost zero) by tuning an internal clock phase. We have undestood the origin of the probem that is the Vcc and GND bouncing and some solutions have been proposed and designed in the VeloPix two. We have added extra on-chip decoupling, splitting the internal supply in the ePLL and smaller and slower the clock buffers to smaller current peaks, spread in time and small penalty in clock skew, hence time-walk.

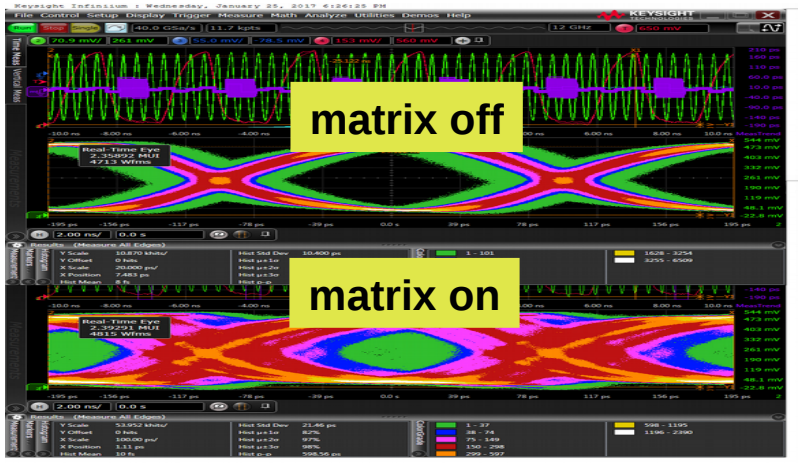

Figure 3: High speed eye diagram.

5. Total Ionizing Dose test

The Total Ionizing Dose tests have been carried with the X-ray machine at Glasgow university in december 2016. We have irradited the VeloPix asic up to 400 Mrad, that is the radiation expected at the end of the VeloPix detector. We have not seen changes in digital power

consumption and no drift in the analoge parameters like the Pixel threshold, noise and global DACs. In figure 4, we represent the value of the treshold with diferent radiation dose.

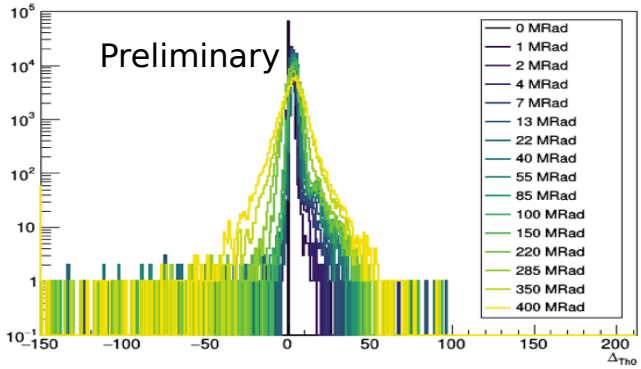

Figure 4: Threshold value with diferent radiation dose.

6. Beam test

To test the VeloPix at the maximum rate posible in the current facilities we carried out a test beam campain in the Fermilab facility. We reached rates up to 300 Mtracks/s using a telescole with 5 planes of VeloPix, figure 5. In figure 6, we plot the first hitmap of the test and the preliminary residual distribution in the horizontal direction.

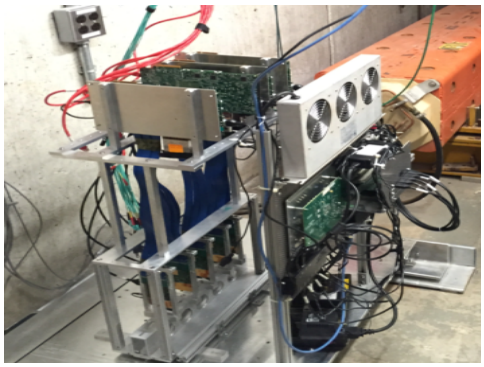

Figure 5: Telescope with 5 VeloPix planes.

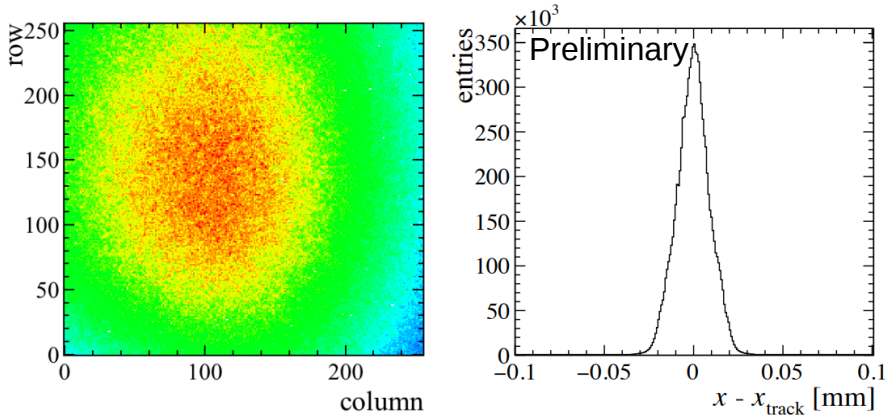

Figure 6: Hitmap (left) and residual distribution in the horizontal direction (right).

7. Single Event Efect tests

Four test sessions at HIF in Louvain-Le-Neuve (figure 7) have been carried in the year 2017. The aim of the tests was to determine the cross-section for the single event upsets (bit-flips) in the diferent triplicated and not triplicated registers. For that propose, we shoot the chip with heavy ions of various type and angles. We have found some issues that are Single Event Latch-up (SEL), large cross-section for the SLVS receiver and few small design flaws with the state machines.

The SEL is a (local) short circuit on the power lines due to high n-well and p-substrate resistance. In our case, the current rise 30 mA per SEL. The recover of the chip is only possible by power cycling. SEL ocurrs only in the pixel matrix because it uses a custom high density library and it avoids the reading back of the data from the internal shift register (read of config settings). SEL is temperature dependant and not happens bellow -10ºC. SEL has been confirmed by injection of laser light at the Montpellier facility (figure 8). We solve this problem in Velopix two using new n-well and p-substrate contacts placed closer to p+ and n+ implants of the CMOS.

After covered the matrix to get rigid of SEL (figure 8 left), we observed frecuent resets of the chip. We knew that the distribution and logic of the reset signals are triplicated, but there is only one receiver line and this happens to have a quite large crossection that give single event transients. After confirmed this fault with the laser facility, we decided to triplicate all the SLVS receivers.

Then, we covered the matrix and the SLVS receiver part of the chip (figure 8 right) and we tested the prerifery and the high speed transmision lines. This test shows up that the state machine of the fifos are not correct and sometimes the output links transmit the same data at high speed all the time.

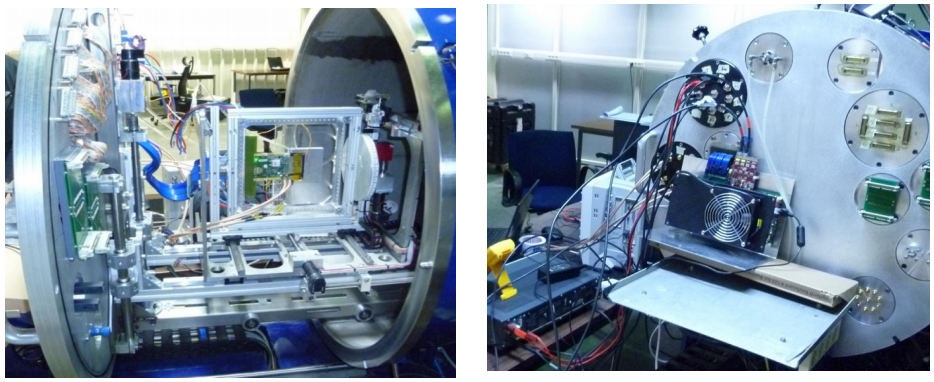

Figure 7: HIF in Louvain-le-Neuve.

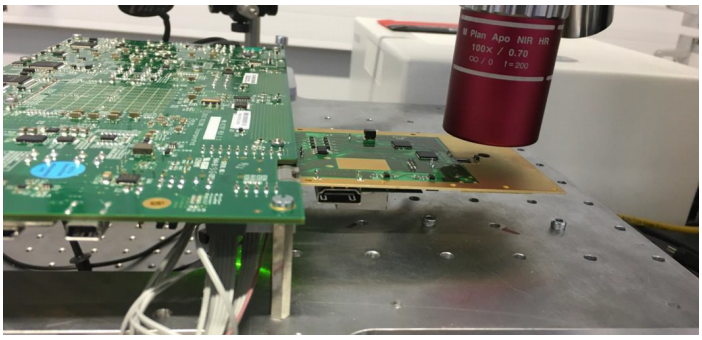

Figure 8: Montpellier laser facility.

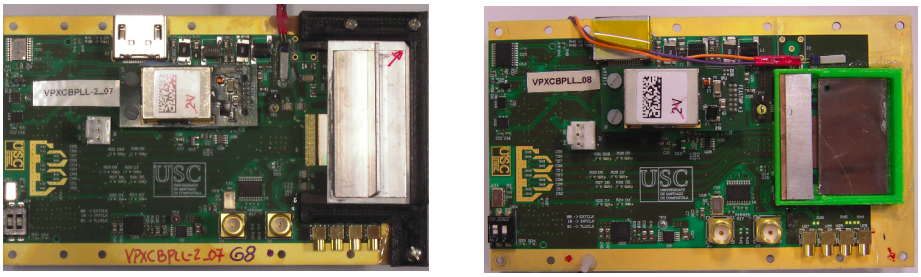

Figure 8: Matrix cover (left) and; SLVS and Matix cover (rigth) realized in the University of Santiago de Compostela.

8. Conclusions

Large campain of VeloPix one testing has been carried out over the end of the year 2016 and in the year 2017. We carefully tested all the design goals of the chip and founded some issues that need to be solved. So, the chip has been redesigned with the new improvements. We receive the Velopix two in November 2017.

References

[1] M. van Beuzekom et al., "Velopix ASIC development for LHCb VELO upgrade", Nucl. Instrum. Meth. A 731 (2013) 92.

[2] T. Poikela et al, "VeloPix: the pixel ASIC for the LHCb upgrade", 2015 JINST 10 C01057.

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[4] V. Gromov et al., Development of a low power 5.12 GBPS data serializer and wireline transmitter circuit for the VeloPix chip, 2015 JINST 10 C01054.