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Overview and perspectives of depleted CMOS sensors for high radiation environments

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To cope with increased radiation levels expected at the HL-LHC new approaches are being investigated using monolithic CMOS pixel detectors where readout electronics and depleted charge collection layer are combined. Those devices rely on radiation hard process technology, multiple nested wells, high resistivity substrates and ability to apply high voltage bias to achieve significant depletion depths. They can be thinned and backside processed for biasing. Since 2014, members of more than 20 groups in ATLAS are collaborating in CMOS pixel R&D in an ATLAS Demonstrator program pursuing sensor design and characterization with the goal to demonstrate that depleted CMOS pixels are suited for high rate, fast timing and high radiation operation at LHC. Many CMOS technology vendors have been approached in this effort. This contribution introduces challenges for the usage of CMOS pixel detectors at HL-LHC and gives a summary of different concepts and the current state of designs of depleted CMOS prototypes.

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1. Introduction

Pixel detectors play an essential role in particle physics experiments as they allow precision track reconstruction in a very compact way and they exhibit rapid development from the progresses in the microelectronics industry.

At present most of the large-scale pixel detectors operating in high-energy physics are based on hybrid approach, where the sensor is produced on a dedicated sensor grade silicon material, while the separate pixel readout chip is manufactured using standard CMOS process (Figure 1). Hybrid pixel detectors allow independent optimization for both sensor and readout chip. The main disadvantage is the complicated process of assembly (bump & flip-chip technology). This is the driving factor in the cost for large-area detectors.

In silicon detectors, the signal charge is generated over the full thickness of the sensor. All released charge carriers, dominantly from depleted areas, drift to the collection electrodes. This induces a current pulse on the pixel sensor electrodes, which is processed by the pixel readout chip. The signal magnitude decreases with increasing radiation damage to the detector.

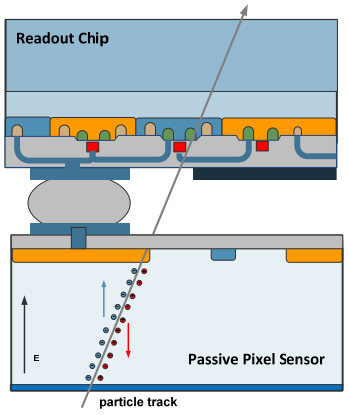

Figure 1 A cross-section through a typical hybrid pixel sensor with fully depleted silicon planar sensor and readout.

Monolithic Active Pixel Sensors (MAPS) have been proposed and developed since the late 1990s [1, 2]. MAPS consist of substrate wafers with an epitaxial (epi) layer (thickness 10-15 µm) with the electronics layer on top. In these devices, charge is collected by slow diffusion rather than by drift in a directed electric field (see Figure 2a). This kind of detector can be very thin, resulting in a sensor material budget an order of magnitude below that of hybrid pixel detectors. Due to the thin un-depleted epi-layer and often incomplete charge collection, the signal is typically small (~1000 e^-). Also, the readout is usually slow, resulting in low readout frame rates. The radiation tolerance is much below that required at the LHC. Nevertheless, MAPS detectors have matured in recent years and are currently used in pixel vertex detectors at the STAR Experiment at the RHIC collider (Brookhaven, USA) [3] and to be used at the ALICE experiment at LHC [4].

The significant progress made in recent years in the field of monolithic active pixels sensors makes them a possible alternative to hybrid pixel detectors. Especially the last development of depleted MAPS (DMAPS) detectors which have shown substantial improves in the radiation tolerance. In these devices the entire CMOS pixel electronics is placed inside an isolated well. By applying reverse bias it is possible to create a depletion depth of a few to hundreds of µm. Charge collection occurs mostly by drift (in the depleted area). The prototype device has been proven to stand much higher radiation fluences than classical MAPS detectors and up to about 10^{15} n_{eq}/cm^2 which is required for outer layers of the proton-proton experiments at the LHC application.

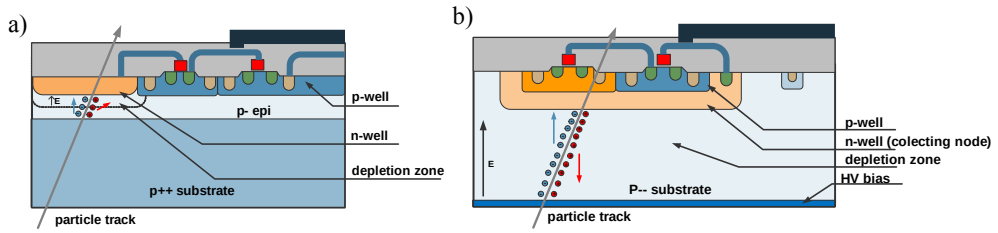

Figure 2 A cross-section through monolithic active sensors a) classical (epi-based) where charge is collected in thin epi layer mostly by drift b) DMAPS where charge is collected in the depleted bulk by drift

2. Charge collection in the presence of trapping

The particle detector environment often puts harsh requirements on the radiation hardness of the detector components. The tracking devices are exposed to large fluences of radiation which damage the detector, after which the detector must retain a minimum signal to noise ratio for efficient particle detection. The main effects due to radiation damage are surface damage and bulk damage.

Surface damage in silicon is due to the ionization energy loss of charged particles or X-ray photons. This causes charges traps to build up in the SiO_2 and at the $Si\text{-}SiO_2$ interface causing transistors threshold shift and increase in leakage current. Usually, a threshold shift increases with the gate oxide thickness. For a thin gate oxide (<3-5nm), the threshold change is tolerable due to tunneling effects for expected LHC doses [5]. The transistor leakage current depends on technology, design, and radiation dose. In cases when radiation-induced leakage current becomes a problem, it can be mitigated by proper design [6]. The surface damage effects in the sensor like breakdown voltage, sensor leakage current and pixel isolation are typically smaller than the one induced by bulk damage or can be mitigated by proper design in case of an LHC-like radiation environment.

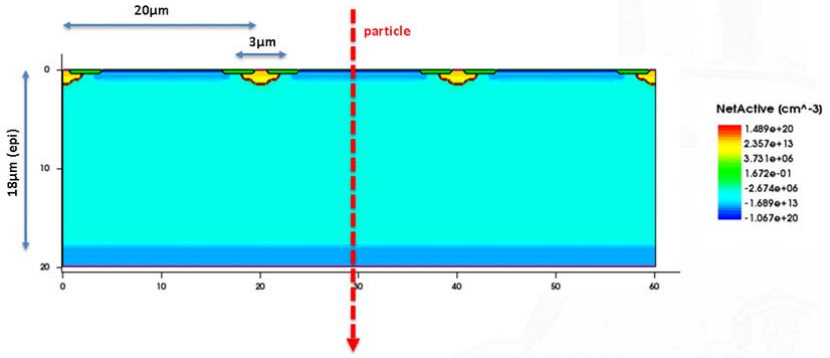

Figure 3 A cross-section through a silicon detector with epitaxial layer (18µm). A track of a particle marked as red dashed arrow. A fill factor of 3/20µm is assumed. Color code is active doping concentration.

Bulk damage has the greatest impact on sensor performance. Bulk damage is caused by the interaction of particles with the nuclei of the lattice atoms [7]. Main visible effects are an increase of a leakage current (increase in noise), a change in effective doping concentration, a decrease in the amount of collected charge due to the charge carrier trapping, and the reduction of the carriers' mobility. These effects lead to a reduction of the signal and an increase in noise.

Figure 4 shows results of simple TCAD simulation of the simple detector from Figure 3. The radiation effects are modeled according to [8]. Initial DMAPS designs (HV-MAPS [9]) were using high voltage bias and low resistive silicon material as a sensor. As one can see from the simulation, the best charge collection can be found in case of high-resistive material and

high voltage bias. Another critical factor is the gap between collection electrodes. As the distance between electrodes increases the electric field between the pixels decreases, resulting in charge loss.

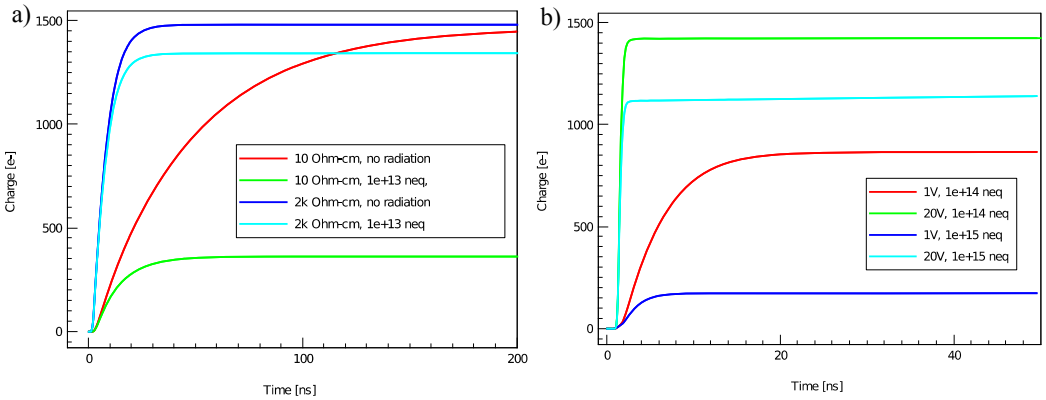

Figure 4 Charge collection for different doses of radiation for a) different initial substrate wafer resistivity and 1V bias, b) different bias voltage and 2 kOhm-cm wafer resistivity.

3. Design approaches

Two main sensor design concepts can be distinguished for n-on-p CMOS sensor designs. Figure 5a shows one with processing logic inside the collection node (deep n-well). This configuration from the sensor perspective is very similar to standard planar sensors, allow for small gaps between collection nodes and bias of the sensor with high-voltage (>100V). This results in good radiation tolerance. The downside is an increase in input capacitance by the parasitic capacitance (C_{PW}) between the collection node and the logic ground (p-well) as well as typically larger pixel size due to required isolations. In the second approach (Figure 5b) the logic is located outside the collection node. This provides very low input capacitance, but has limited sensor bias and the distance between collection node is dependent on the amount of logic in the pixel. Various modifications to those two main approaches have been investigated, some of which have been, implemented and are presented in next section.

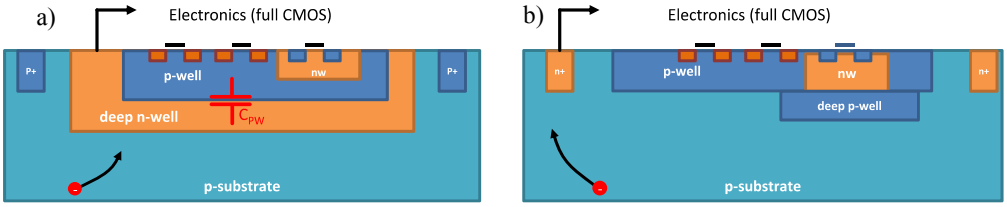

Figure 5 A structure of mayor CMOS sensor types a) then logic is inside collecting well and b) where it is located next to it

From the readout perspective, a crucial factor is the input capacitance. As we have seen, this can be very different depending on pixel sensor designs (from few fF to hundreds of fF). Figure 6 shows a typical silicon pixel detector readout configuration with an input collection node (diode), parasitic capacitances D_d, and C_{PW}, and a charge sensitive amplifier with feedback capacitance C_f. In a simple case the dominant (thermal) equivalent noise charge (ENC) necessary for achieving a good signal-to-noise ratio and rise time (τ_{CSA}), essential to get correct timing, can be expressed as:

$$\mathrm{ENC}_{\mathrm{therm}}^2 \propto \frac{4}{3}\frac{\mathrm{kT}}{\mathrm{g_m}}\frac{\mathrm{C_d^2}}{\tau}$$

$$\tau_{CSA} \propto \frac{1}{g_m}\frac{C_d}{C_f}$$

where k is the Boltzmann constant T temperature, g_m is the transconductance of the input transistor, and τ is the shaping time of the amplifier. One can see that total input capacitance C_d plays a major role. A typical way to compensate for a large capacitance is to increase the transconductance g_m, at a cost of an increased power consumption.

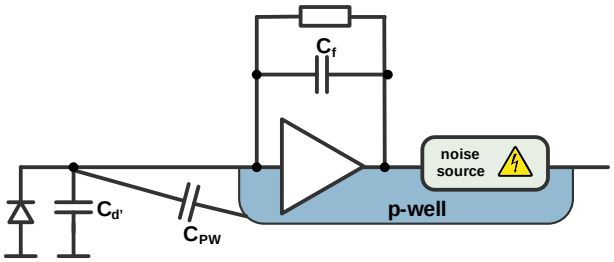

Figure 6 A typical silicon pixel detector readout configuration with parasitic input capacitances an potential noise source (digital switching) coupled to input.

In case of a design were logic is located inside the collecting node, (Figure 5a) another critical factor is the possible noise coupling (electronic crosstalks) between the activity logic ground (deep p-well) and the input (deep n-well) due to the parasitic capacitance C_{PW} which couples the electronic ground and the most sensitive input node directly.

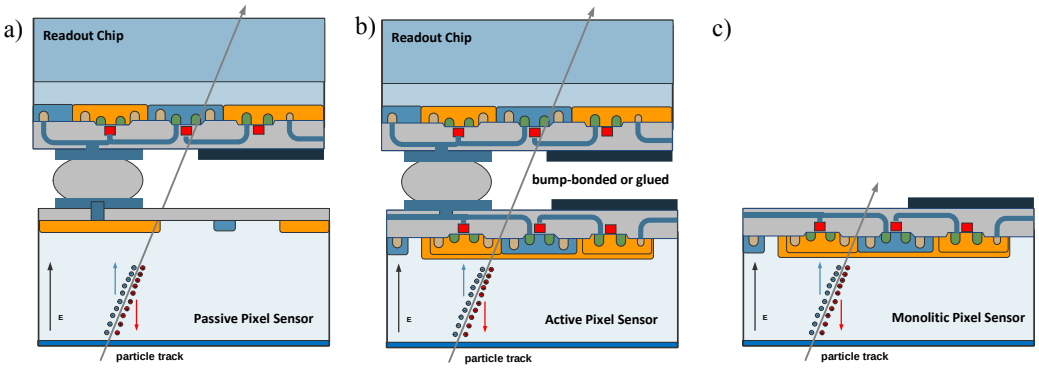

Figure 7 Different application of DMAPS detectors as a a) standard hybrid passive sensors b) as active sensors connected by bumps or capacity capable using glue c) fully monolithic devices.

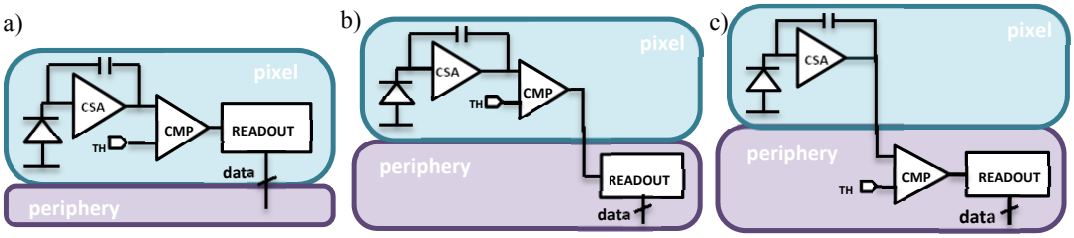

Figure 8 Different readout organization schemes of DMAPS devices a) full pixel readout integrated inside the active pixel are b) where the digital hit information is sent processed in the periphery and c) where only the amplifier is part of the pixel.

Due to process limitations, not all technologies allow for full isolation of the logic inside the pixel. Achieve high logic density in fully monolithic design can be difficult, requires extra space for isolation structures and very careful design. Currently, DMPAS devices are produced with the 130-180nm process and do not offer required logic density which is available in modern

CMOS processes (<=65nm) because of the cost of needed process adoptions. For those reasons as well as to speed up prototyping (no need for full readout), many developments have been designed for hybridization to form so-called CMOS Active Hybrid devices. In this case, those devices can be connected by bump-bonding or by a form of capacity coupled devices *[10]* using glue. Figure 7 shows different possible usages cases for DMAPS devices. Due to a similar limitation, different readout organizations have been persuaded. Figure 8a shows a fully monolithic readout in pixel readout channel where entire pixel processing including an amplifier, comparator, and readout logic is located inside pixel cell. This approach is most area and design (low digital noise) demanding. For this reason, a split design when only part of the pixel is located at the chip periphery and not in the active area has often been used (Figure 8b/c). In the case of the active hybrid approach, the connection to the readout chip is typically made after the comparator, and the periphery is on the second readout chip.

4. Example Implementations

In recent years, many prototypes in different technologies have been fabricated as an attempt to develop a radiation tolerant monolithic sensors. First devices where logic is located inside the collecting well [9] ware produced using standard CMOS wafer material (low resistivity), had moderate sensor bias (>100V), and had somewhat simple data processing. The complexity of these sensors has gradually developed. They have started to utilize high-resistivity wafers, allow for a higher bias voltage and backside processing. These advancements have resulted in a monolithic device with many performance parameters similar to hybrid devices. Conversely, epi-based MAPS devices have managed to improve the production process substantially and have increased radiation tolerance while keeping most of its advantages including low noise and power consumption. A separate set of devices based on SOI technology also show, promising results in the field of radiation hard detectors.

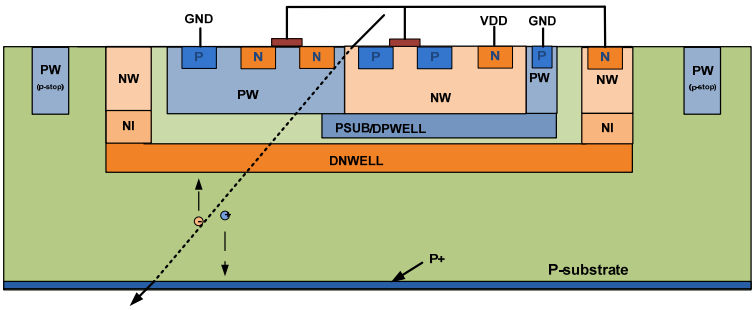

Figure 9 Cross-section through the implant structure of a DMAPS A sensor technology in LF15A technology.

4.1 Logic inside the collecting well (large fill-factor)

Figure 9 shows a typical cross-section of a depleted DMAPS sensor where the readout logic is located inside the charge collection node (in this case LFoundry 150nm process). The collecting node is a combination of NW/NI/DNWELL implantations and also isolates the logic located inside it. The internal NW is separated from the collecting node by a PSUB implant that allows unrestricted use of both n-MOS and p-MOS transistor types (a feature which was not available in early prototypes). Between the collecting electrodes, a PW implant acts as a p-stop to stops the accumulation layer in the oxide caused by radiation. The entire design is typically surrounded by the guard rings, and the whole peripheral logic is located in a DNWELL. This allows bias to be applied to the sensor without damaging the transistors.

A substantial amount of development for this types of devices has been done with AMS 350nm and 180nm technologies having various applications in mind. The most recent of them are the MuPix7/MuPix8 devices intended to be used at a Mu3e experiment at PSI [11]. Although

these devices are not expected to be exposed to extensive radiation, they need to be thin (low material), fully monolithic and fast. Figure 10 shows the layout of the MuPix7 design and test beam results which show very good particle time stamping performance below 11ns and high particle detection efficiency (>99%). Further improvements are expected for the large-scale MuPix8 sensor by increasing wafer substrate resistivity from 20 Ohm-cm to 80 Ohm-cm and other design improvements.

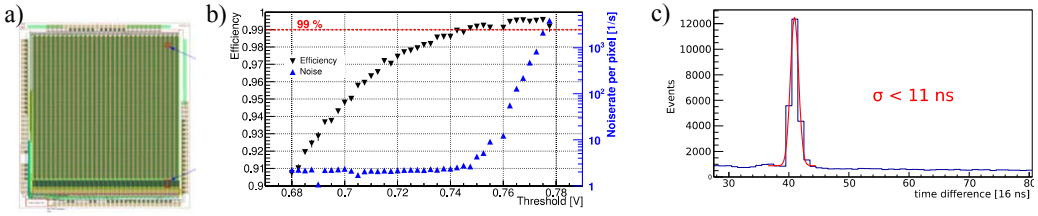

Figure 10 Layout of a) the MuPix7 chip and its measured performance b) hit detection efficiency and c) time stamping resolution (from [12]).

The development targeting LHC application went through many iterations for both strip and pixel layers. Notably, the series of CCPD [13] devices which were first to investigate the possibility to use glue instead of bumps for inter-chip communication and most recently development of large area monolithic device ATLASPIX. A substantial number of devices and measurements with various configurations have been performed showing good efficiency and timing. An example can be seen in the Figure 11where good detection efficiency and timing resolution can be observed even after a fluence of $5x10^{15}n_{eq}/cm^2$. In the process, many improvements have been employed leading the to the development of large monolithic devices in AMS technology that are being currently designed and measured.

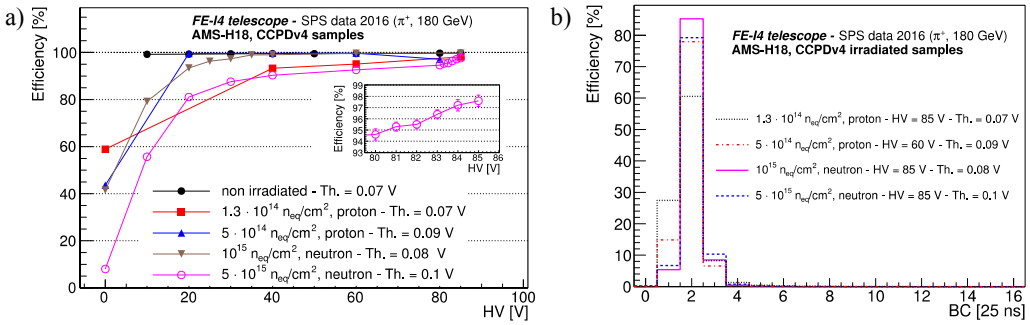

Figure 11 The measurement results of CCPDv4 devices a) track detection efficiency for different neutron dose, threshold and bias b) time stamping resolution (from [14])

A similar design approach has also been followed in LFoundry 150nm process that from the beginning provided a high-resistive substrate (>2kOhm-cm) and full logic isolation in the pixel. The sensor performance has been evaluated by producing an n-on-p passive sensor that was bump-bonded to an FE-I4 readout chip [15] currently used at the ATLAS experiment. By using CMOS processes, an AC coupling can be integrated into a small pixel. Figure 12 shows the measured efficiency for 300µm and 100µm sensors for different level of radiation damage in a function of bias. The efficiency is comparable to existing passive sensors at ATLAS or even better in case of the AC coupled version (no charge losses due to bias structures in the sensor).

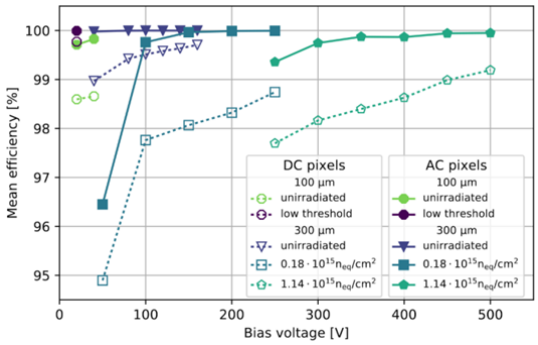

Figure 12 Particle tracking efficiency of the passive sensor in LFoundry 150nm technology for different thickness and radiation fluence in a function of bias voltage. The readout chip is FE-I4 tuned to typical ~3000e- threshold (from [16]).

A series of active CMOS devices targeting the LHC experiment have been developed in LFoundry technology starting with active hybrid devices (CCPD-LF, LF-Cpix [17, 18]) followed by a large entirely monolithic device (LF-Monopix). Figure 13a shows a layout view of LF-Monopix which is a 1x1cm^2 fully monolithic device with readout architecture very similar to used in the ATLAS FE-I3 readout chip [19] that is fully functional and is being currently characterized [20]. Figure 13b/c shows measurements on LFoudry based devices indicating that a large depletion depth (>100µm) is achieved even after fluence of 2x10^{15}n$_{eq}$/cm^2 and the process is suitable as a detector in high radiation environments.

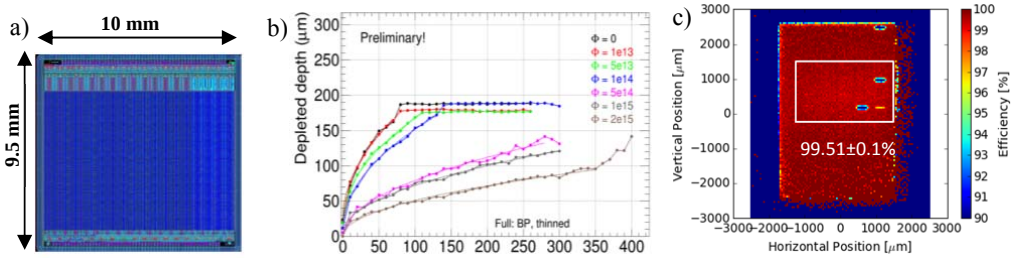

Figure 13 The layout of a) the LF-Monopix chip and b) depletion depth for different fluenced as a function of bias measured with the edge-TCT method for 200µm sensor [21] c) the track efficiency map for an unirradiated LF-Cpix device [22].

4.2 Logic outside collecting well (small fill-factor)

The devices with logic located outside the collecting node were mostly investigated using TowerJazz 180nm technology and ESPROS 150nm technology. Both share similar logic isolation strategies where a DPWELL is used to isolate NW but they use different sensor materials (see Figure 14). Both of these approaches provide very small input capacitance which leads to possibly low noise, low power designs and low sensor bias (~6V).

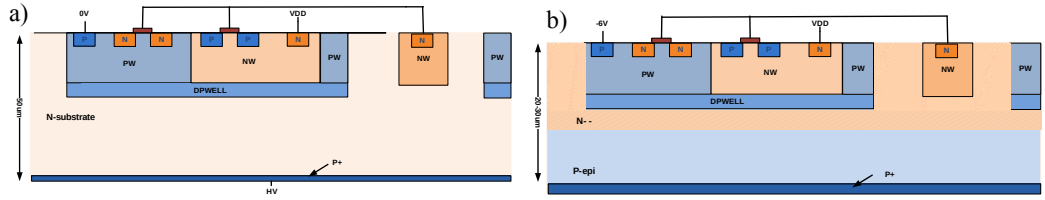

Figure 14 A cross-section through a) ESPROS Photonics process and b) improved TowerJazz process.

In case of the ESPROS process, the sensor consists of a 50µm, thin, high-resistive n-type where the collecting node is the ohmic side of the diode. Prototype devices in this technology [23, 24] have shown full depletion and good performance with low radiation doses

but a sharp decrease in detection efficiency above a fluence of 10^{14} n_{eq}/cm^2. This may be improved by design changes.

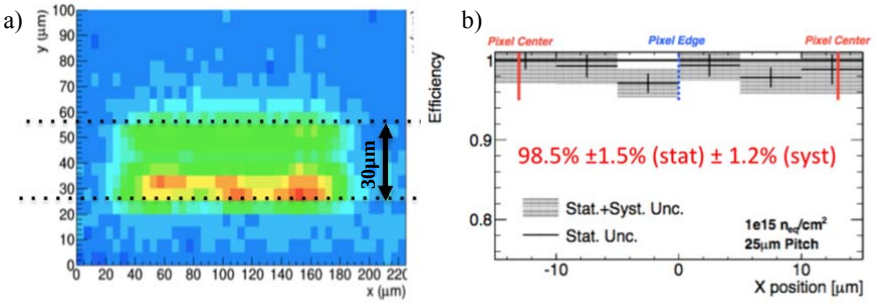

Figure 15 A charge collection map of the Investigator chip in improved TowerJazz technology at 6V bias and 10^{15} n_{eq}/cm^2 fluence measured with the edge-TCT method and b) detection efficiency across pixel borders after fluence of 10^{15} n_{eq}/cm^2 (from [25]).

The advances in TowerJazz technology are a continuation of the development for the ALICE experiment (notably the ALPIDE chip [4]). The ALPIDE has proven its performance up to a fluence of $2x10^{13}$ n_{eq}/cm^2, which is required by the ALICE experiment. To further improve the radiation tolerance, a process modification of extra n-type implantation has been used (see Figure 14b) [26]. The small prototype chip (Investigator [27]) has been produced and characterized showing good charge collection even after a fluence of 10^{15} n_{eq}/cm^2 (see Figure 15). Currently, two large (2x2 and 1x2 cm^2) monolithic devices are being produced which make use of this technology. These devices characterize with small pixel size (36x36 μm^2), low power consumption and bias voltage.

4.3 HV-SOI

Another promising technology is HV-SOI in the XFAB 180nm process. Figure 16 shows a cross-section through a HV-SOI detector. In this process the active logic is fabricated in a thin silicon layer on top of an insulating layer made of silicon dioxide (buried oxide - BOX). The layer underneath the BOX can be used as a sensor layer. Several well structures give the possibility to isolate the transistor from any influence of charge build-up in the BOX (the issue initially seen in FD-SOI technology [28, 29]). The HV-SOI technology allows access to the handling wafer/substrate using vias to create a charge collecting node as well as provide bias to the sensor A standard CMOS circuit can be realized in the logic layer above BOX.

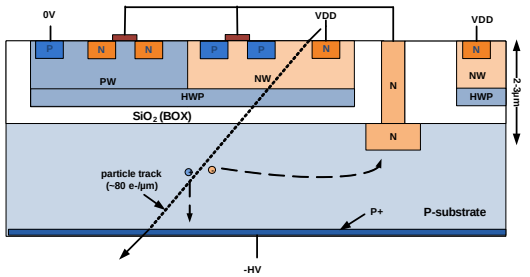

Figure 16 A cross-section through the HV-SOI process. The logic is located above oxide buried layer isolated by deep implants. The handling wafers is used as sensor layer.

The prototyped devices in HV-SOI technology XTB01and XT02 [30, 31] are fully functional. Figure 17a shows that they have good radiation tolerance to surface damage. For the FD-SOI technology those issues are currently being mitigated by introducing double SOI wafer [32]. The sensor has a high breakdown (>300V) and a charge collection after high radiation dose (Figure 17b).

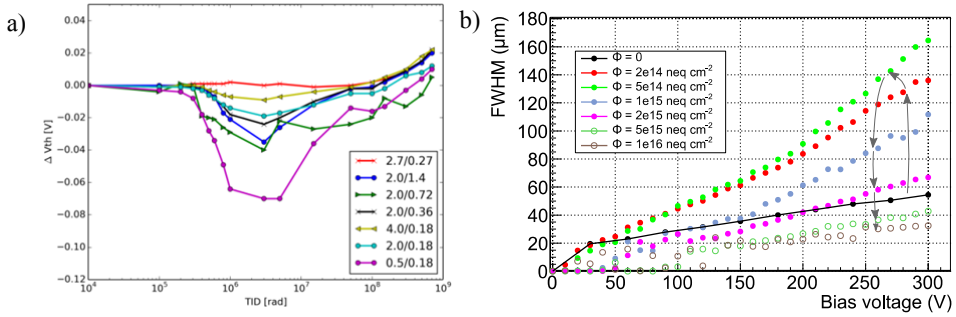

Figure 17 A n-MOS transistor threshold shift for as a function of total ionizing dose (TID) for different transistor dimensions (from [31]) a) and charge collection depth of the sensor for different fluence as a function of bias b) in HV-SOI technology [33].

5. Conclusions

Until present only hybrid pixel devices demonstrated the capability to sustain the high radiation environments at the LHC. However, hybrid devices suffer from many drawbacks, mainly, rather large material and production complexity and cost. Monolithic devices have been successfully used on a large scales for less demanding conditions. Intensive progress has been made in recent years to improve the performance of monolithic devices leading to various pixel sensor prototypes in different technologies. The presented devices show strong indications that monolithic sensors can achieve very high radiation tolerance (fluence of $1x10^{15}$ n_{eq}/cm^2) with parameters similar to the existing hybrid technology. They are being considered in some areas as an alternative to hybrid detectors for the ALTAS Phase 2 upgrade (outer layers) allowing for a reduction of cost, and material. Other application areas like X-ray imaging may also benefit from this development.

Acknowledgments

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