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Silicon pixel R&D for CLIC

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The physics aims at the proposed future CLIC high-energy linear e^+e^- collider pose challenging demands on the performance of the vertex and tracking detector system. The detectors have to be well adapted to the experimental conditions, such as the time structure of the collisions and the presence of beam-induced backgrounds. The requirements include ultra-low mass, facilitated by power pulsing and air cooling in the vertex-detector region, small cell sizes and precision hit timing at the few-ns level. A highly granular all-silicon vertex and tracking detector system is under development, following an integrated approach addressing simultaneously the physics requirements and engineering constraints.

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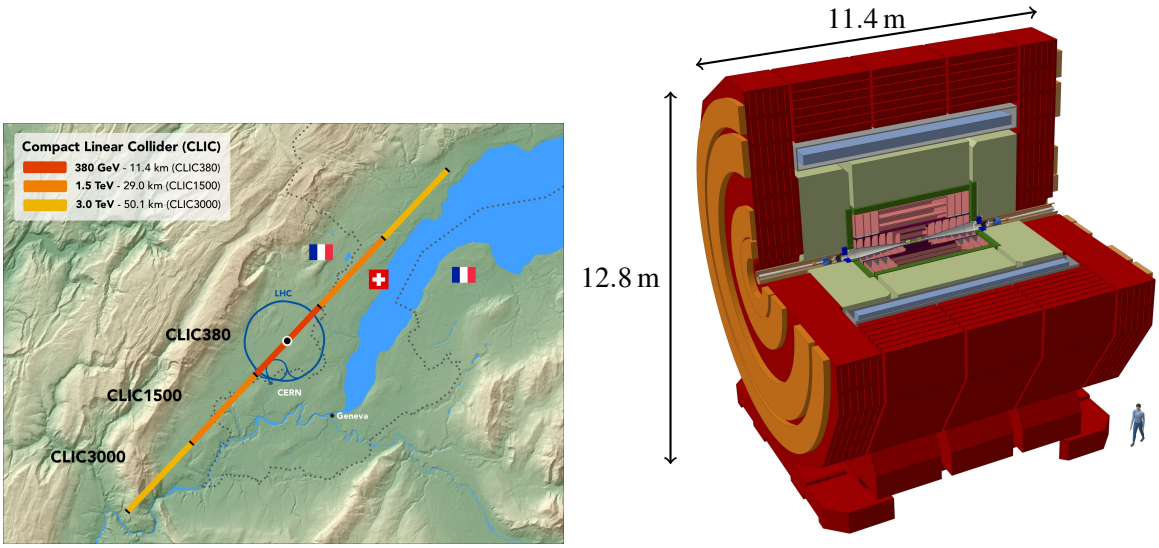
1. Introduction

The Compact Linear Collider CLIC is a proposed high energy linear e^+e^- collider [1, 2], with center of mass energies ranging from 380 GeV in the initial phase up to 3 TeV in the high energy stage [3]. The CLIC accelerator and detector are designed to perform precision measurements of standard model processes, and direct and indirect searches for new physics. A possible layout of the 50 km long accelerator complex in the Geneva region is illustrated in Figure 1a, while Figure 1b illustrates the current detector model [4].

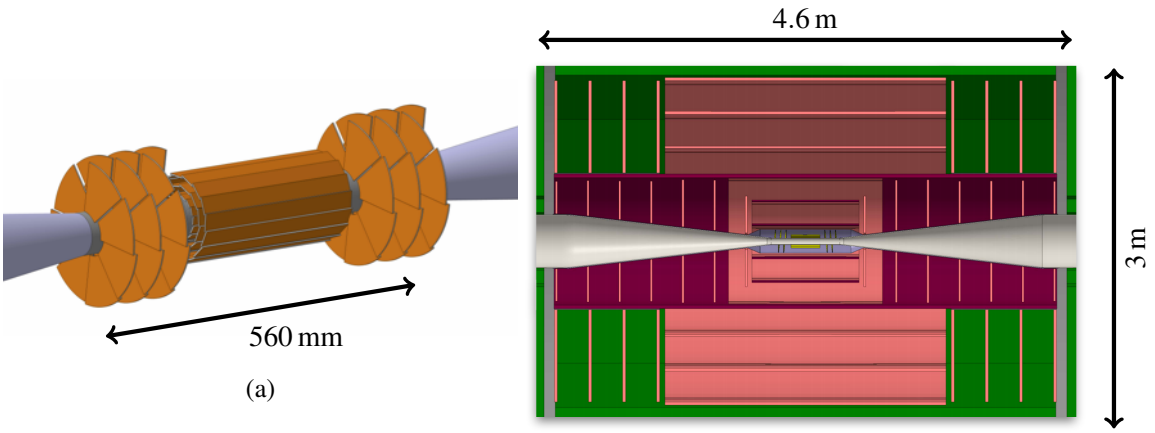


(a) (b)

Figure 1: (a) Possible layout of the Compact Linear Collider CLIC near Geneva. (b) The CLIC detector.

The objective to perform precision measurements imposes challenging requirements on the detector. For the vertex and tracking detector, this manifests in a very low material budget of 0.2 %X_0 per layer in the vertex and 1–2 %X_0 per layer in the tracking detector, a single point resolution of 3 µm in the vertex and 7 µm in the tracker, and a time-tagging capability of 10 ns. In the vertex detector, the material budget leaves no margin for liquid cooling of the detector. The low duty cycle of the CLIC machine (312 bunches in 156 ns long bunch trains every 20 ms) allows for pulsed power operation of the vertex and tracking detectors. This helps in reducing the average power consumption and offers the possibility to apply air-flow cooling of the vertex detector. To cope with the limited cooling power, the power consumption of the vertex detector has to be restricted to 50 mW cm^{-2} [5].

Figure 2 illustrates the vertex and tracking sub-detectors, which are operated in a 4 T solenoid field. The vertex detector consists of three double layers in the barrel part, covering a radius from 31 mm to 60 mm, and a spiral endcap geometry to facilitate efficient air-flow through the detector. The tracker is divided into an inner and outer part by the beam pipe support tube. The detector consists of 3 inner and 3 outer concentric barrel layers ranging up to 1.45 m in radius and 7 inner and 4 outer flat discs on each side. In total, the tracker detector covers an active area of 100 m^2.



(a) (b)

Figure 2: Rendering of the (a) vertex and (b) tracking detector as implemented in the CLICdet detector model [4].

The different detector requirements in the vertex and tracking detector call for different technology options. In the vertex detector, it is particularly difficult to achieve a very good single-point resolution with very thin detection layers. Hybrid pixel detectors allow to optimize sensor and readout chip separately. Either planar sensors bump bonded to dedicated readout chips or capacitively coupled pixel detectors (CCPDs) with active sensors are currently under study. For the tracking detector, the requirements on resolution and material budget are less strict. Throughout the detector, elongated pixels of at most 1 mm to 10 mm length are necessary to limit the occupancy of the detector [6]. Fully monolithic detector technologies, integrating the sensor and readout part on the same silicon die, have the prospect to meet the requirements. This offers the advantage of avoiding costly bump bonding for the large surface detector. In the following, an overview of the ongoing vertex and tracker technology R&D and results from recent tests are presented.

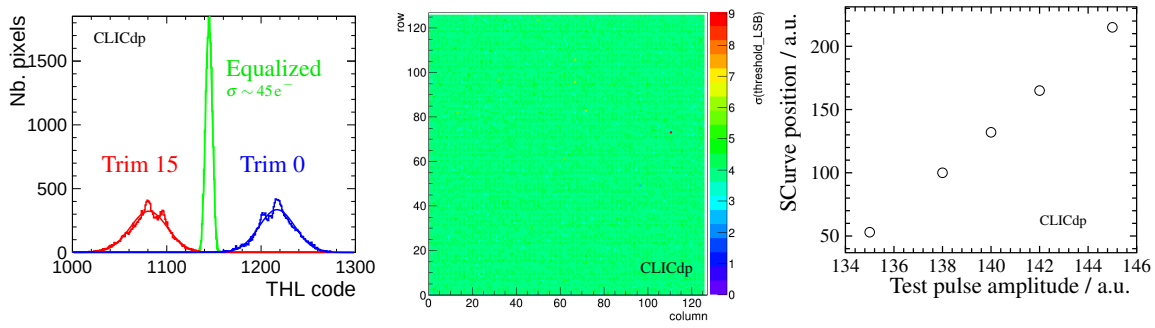
2. Fine pitch hybrid pixel detector R&D

CLICpix is a prototype readout chip featuring a 64×64 pixel matrix with $25\,\mu m \times 25\,\mu m$ pixel size. The architecture is derived from the Timepix/Medipix chip family, and the chip is fabricated in a 65 nm commercial CMOS process [7]. It has been used over the last couple of years to characterize a variety of sensors, both planar and capacitively coupled active sensors. Recently, an updated and improved version CLICpix2 in the same 65 nm process as CLICpix as well as a matching active high-voltage CMOS (HV-CMOS) sensor were designed and fabricated to overcome limitations observed in the first version of the chip. Both chips, CLICpix2 and C3PD, have been characterized in standalone measurements, followed by test beam studies on capacitively coupled assemblies combining both chips.

2.1 Characterization of the Clicpix2 readout ASIC

The list of improvements compared to CLICpix include an increased matrix size to 128×128 pixels, longer counters for charge (now 5-bit) and timing (now 8-bit) measurements, improved

noise isolation and removal of a cross-talk issue observed in first CLICpix, an improved I/O with parallel column readout and 8/10 bit encoding and integrated test pulse DACs and band gap. Standalone characterization of the chip verified the functionality and showed the expected performance. The threshold voltage can be fine-tuned in each pixel to compensate for process fluctuations, as depicted in Figure 3a. The remaining threshold dispersion after optimization of the threshold adjustment bits is $\sim 45\,e^-$. The measured noise of $60\,e^-$ is close to the $67\,e^-$ expected from simulation, and the distribution is uniform over the pixel matrix, as illustrated in Figure 3b. The amplitude response of the front-end amplifier to various test pulse charge injections is linear, demonstrated by Figure 3c.



(a) (b) (c)

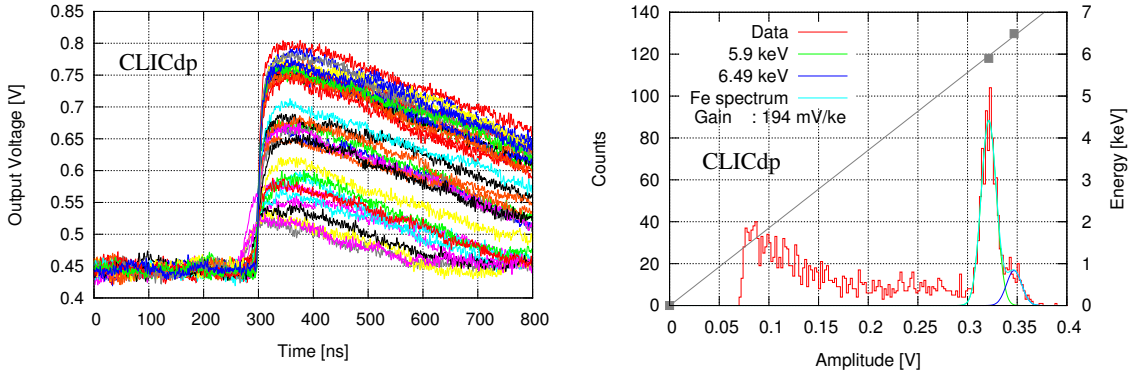
Figure 3: CLICpix2 standalone characterization: (a) threshold equalization, (b) noise homogeneity, (c) front-end linearity.

2.2 Characterization of the C3PD active HV-CMOS sensor

The CLIC Capacitively Coupled Pixel Detector (C3PD) is an active HV-CMOS sensor with an amplification stage in each pixel. A large deep n-well is implanted into a p-type substrate, CMOS transistors are embedded in that n-well. By applying a reverse bias voltage, approximately 10 µm around the n-well are depleted [8], and charge is collected by drift. The matrix footprint of C3PD matches the CLICpix2 pixel layout, i.e 128×128 at $25\,\mu m \times 25\,\mu m$ pixel pitch. Several pixels at the matrix edge can be connected to analog monitoring outputs, which give access to the time resolved amplifier response. These outputs have been used to perform a standalone characterization of bare C3PD chips, before receiving assemblies together with the CLICpix2 readout chip. The sensor has been tested using the internal test pulse injection and an Fe-55 source. The results summarized in Figure 4 have shown an average charge gain of $190\,mV/ke^-$, an RMS noise of $40\,e^-$ and a rise time of 20 ns, for a power consumption of 5 µW per pixel (in continuous power mode). In addition to the standard thickness of 250 µm, several sensors have been thinned down to 50 µm. During the tests, no impact of the thinning on the performance has been observed [9].

2.3 Capacitive coupled CLICpix2 + C3PD hybrid detector assemblies

To achieve a capacitive charge transfer between the C3PD output pads and the CLICpix2 input pads, both chips are glued together in a flip-chip process using a thin layer of epoxy glue,

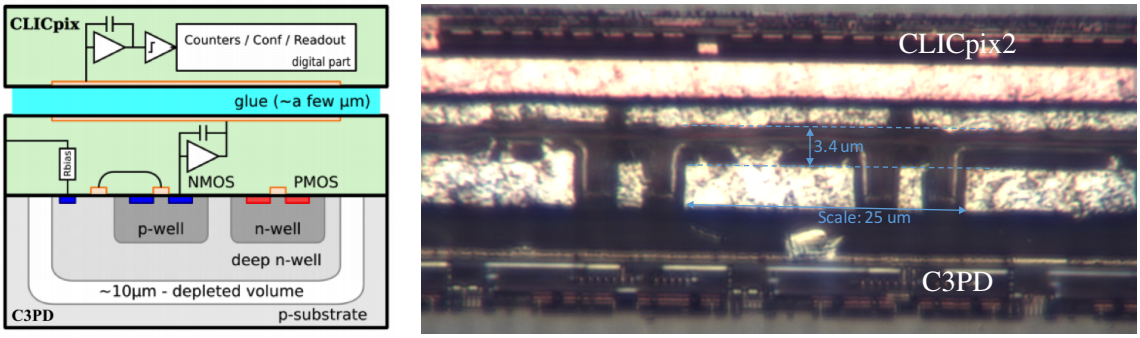


(a) (b)

Figure 4: C3PD standalone characterization: (a) Sample pulses from a Fe55 source. (b) Resulting amplitude spectrum and double Gaussian fit for one of the monitored pixels [9].

as sketched in Figure 5a. To achieve a uniform coupling over the full chip size, parameters like glue thickness or bonding pressure and temperature in the curing phase of the glue are still under optimization.

The assemblies are characterized using test pulses and particle beams. Significant variations in the coupling strength and uniformity between the assemblies have been observed. On some assemblies, destructive cross-section measurement have been performed to better determine the alignment precision and glue thickness. Figure 5b illustrates an example cross-section, showing the C3PD and its output pads in the lower half and CLICpix2 and its input pads in the upper half, separated by the glue and the passivation layers on both chips. These measurements confirmed the alignment of both chips to be better than 2 µm and the pad to pad distance to be 3 µm to 4 µm. From finite-element simulations, the resulting coupling capacitance at that distance has been estimated to be of the order of 3 fF [10].

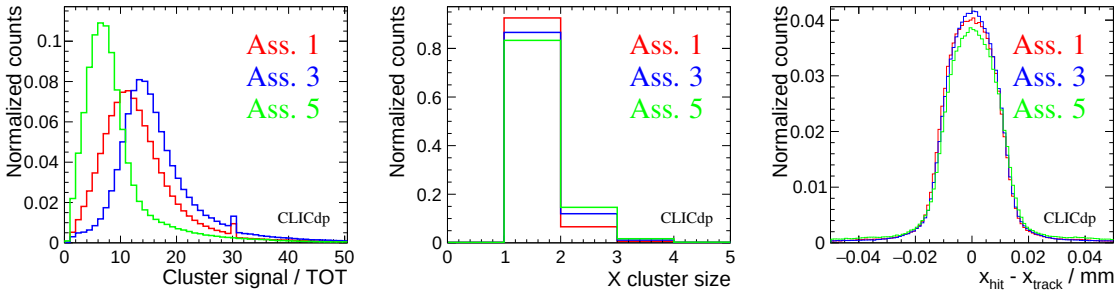


(a) (b)

Figure 5: (a) Illustration and (b) cross section of a capacitively coupled pixel detector. An active HV-CMOS sensor (C3PD) is glued to the CLICpix2 readout ASIC. Charge is capacitively transferred between both chips.

2.4 Testbeam measurements

Several CLICpix2 and C3PD capacitively coupled hybrid detector assemblies have been tested in a 120 GeV pion beam, using a Timepix3 based reference telescope. The preliminary results summarized in Figure 6 show differences in cluster signal and size distributions among the assemblies, as expected from the varying glue assembly quality. The width of the residual distribution of 8.5 µm to 9 µm is similar among the investigated assemblies. As expected from the overall low cluster multiplicities, the resolution is mostly determined by the pixel geometry.



(a) (b) (c)

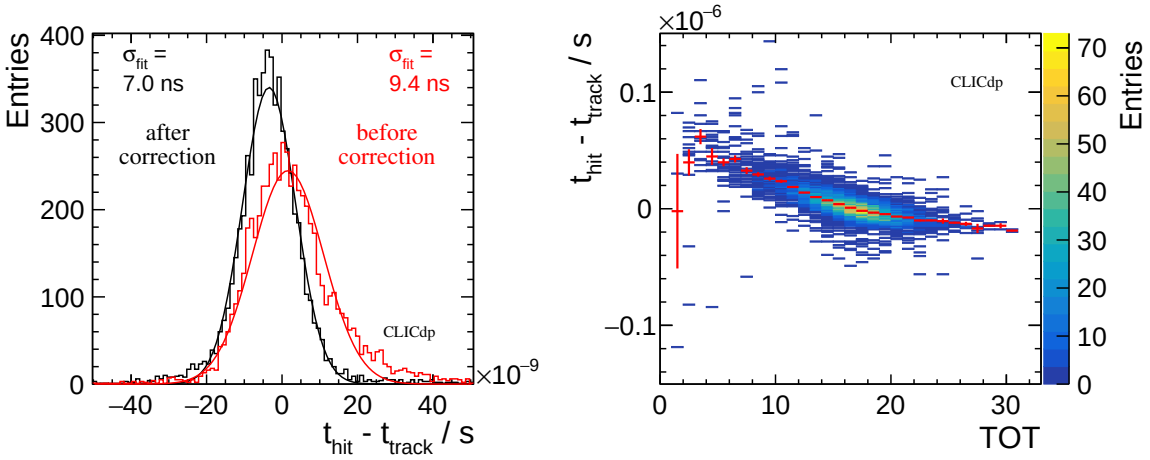
Figure 6: Test beam results on (a) signal, (b) cluster size and (c) resolution obtained with C3PD and CLICpix2 capacitively coupled pixel detector assemblies.

To determine the timing performance of the capacitively coupled assemblies in test beam measurements, the time-of-arrival measurement by CLICpix2 is compared to the reconstructed reference time of the particle track.The track time resolution of the Timepix3 telescope is below 1 ns. CLICpix2 is operated at 100 MHz, the timestamp binning is thus 10 ns. Figure 7a depicts the time residual distribution, before and after applying a time walk correction. A gaussian fit to the non-corrected distribution yields to a resolution of 9 ns.

The non-corrected distribution shows non-gaussian tails towards later hit arrival times, as expected from time walk in the discriminator in the pixel front-end. The time walk effect introduces a correlation between the hit arrival time and the hit energy, which can be exploited to compensate for the effect during the offline hit reconstruction. In Figure 7b, the dependence is illustrated, and the extracted correction function is shown. After correcting, the distribution has a gaussian shape, and a fit results in a time resolution of 7 ns.

3. Monolithic pixel detectors for the CLIC tracker

Monolithic pixel detectors combine the sensitive pixel matrix and the complete analog and digital readout electronics on the same silicon die, making interconnects like bump bonding or capacitive coupling between sensor and readout chip unnecessary. Monolithic detectors are commonly fabricated in larger CMOS feature sizes ($\gtrsim$ 150 nm), which complicates the design of sensors with very small pixel pitch. The design of the CLIC tracker foresees elongated pixels or short strips. Because of the larger pixel area, the tracking sub-detector is thus well suited for monolithic technologies.



(a) (b)

Figure 7: (a) Timing resolution histogram before and after offline time walk correction and (b) time walk measured on C3PD and CLICpix2 capacitively coupled pixel detector assemblies in test beam. The extracted correction is overlaid.

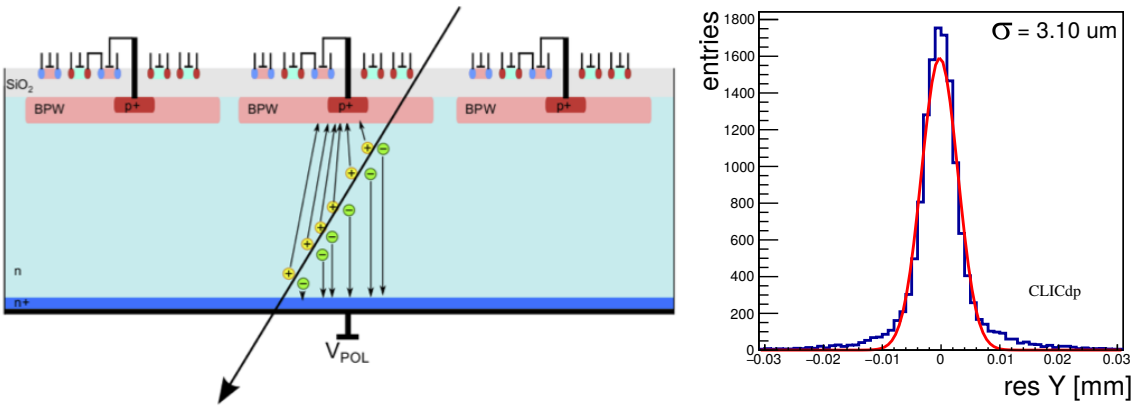
3.1 Silicon-On-Insulator technology

In Silicon-On-Insulator (SOI) wafers, a low resistivity electronics wafer is separated by a buried oxide layer from a fully depleted high-resistivity sensing layer, as illustrated in Figure 8a. P-wells are implanted in a high-resistivity n-doped silicon bulk, acting as charge collection implants. Only a via through the oxide layer connects the pixels to the input transistor, otherwise the electronics layer is fully separated from the sensor wafer. For enhanced tolerance to ionizing radiation, double-SOI structures can mitigate charge-up effects in the oxide layer and consequential shifts of the threshold voltage of the transistors [11].

SOI detectors are under study for the CLIC tracking detector. The investigated test chip is fabricated in a 200 nm process and implements different readout techniques (source follower and charge preamplifier matrix with rolling shutter readout and self triggering matrix). Here, only results obtained with the source follower sub-matrix with 30 µm × 30 µm pixels are presented. The performance of the device has been characterized in test beam measurements. The position resolution is close to 3 µm, as illustrated by the residual distribution shown in Figure 8b. The investigated chip has a 500 µm thick substrate, and thus a significant sharing of charge among several pixels. It is however exceeding the material budget of the CLIC detectors. Nevertheless the results demonstrate the functionality of the concept and give input for further developments. A resolution of the order of 6 µm is expected for devices thinned to 100 µm [12]. The design of the next prototype with larger and more uniform pixel matrices has been finalized recently, offering also a measurement of the hit arrival time with a few ns precision.

3.2 High-resistivity CMOS process

A 180 nm high-resistivity CMOS process, as illustrated in Figure 9, is considered for the CLIC tracker. The process makes use of a high resistive p-doped epitaxial layer grown on a low resistive

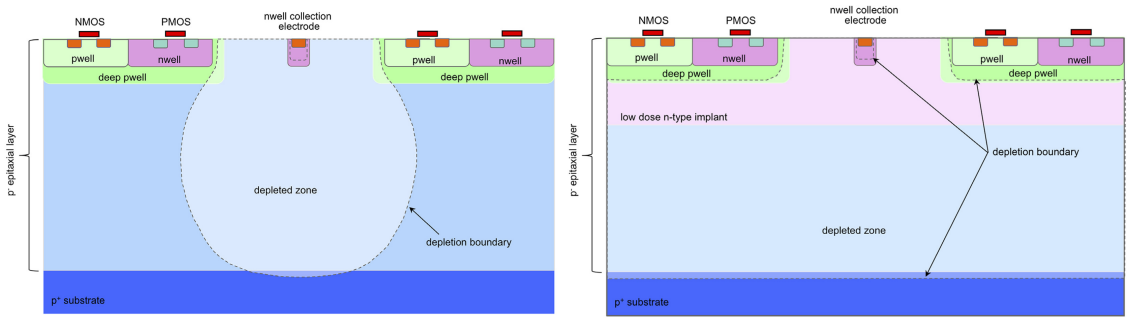


(a) (b)

Figure 8: (a) Silicon-on-Insulator process illustration and (b) spatial resolution obtained in test beam measurements.

silicon substrate. A small n-well serves as collecting diode. The CMOS transistors are embedded in a separate deep p-well outside the collection electrode, as shown in Figure 9a. The capacitance of the diode, and with it the analog power consumption, is reduced. The p-wells serve as bias contact, up to -6 V can be applied. Due to the small fill factor, full depletion of the epitaxial layer under the p-wells is hard to achieve, and the process is possibly prone to slow and inefficient charge collection through diffusion from outside the depletion region. In a recent process modification, this is overcome by introducing a deep planar pn-junction by adding an additional n-implant close to the detector surface [13], as shown in Figure 9b.

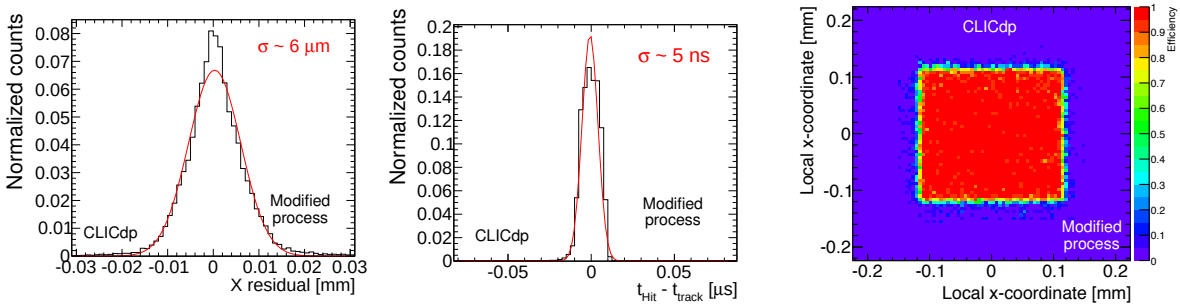
To evaluate the performance of this technology for application in the CLIC tracker, an analog test chip designed by the ALICE collaboration in the framework of their Inner Tracker System upgrade [14] was studied in test beams. The Investigator chip implements 134 different analog mini matrices, varying geometrical and electrical properties of the pixel. Each matrix consists of 8×8 square pixels, with pixel pitches ranging from 20 µm to 50 µm. By selecting one mini matrix, the voltage signal on each of the 64 collection diodes is buffered and routed in parallel to external 65 MHz sampling ADCs. By that, the charge collection characteristics can be studied with high time and energy resolution.



(a) (b)

Figure 9: (a) Standard and (b) modified 180 nm high-resistivity CMOS imaging process [13].

Figure 10 summarizes test beam results for the modified process obtained with a 25 µm epitaxial layer sensor for a matrix with 28 µm pixel size at −6 V bias. A good spatial resolution of less than 6 µm and a timing resolution of 5 ns have been measured [15], extracted from the residual distributions show in Figures 10a and 10b. For the time resolution, this number is to be seen as upper limit to the actual resolution, since the 65 MHz sampling in the readout system is limiting the achievable precision. This number is not directly to be compared to the time resolution obtained with CLICpix2, which has been presented in Figure 7a. Here, only the analog performance of the charge collection process can be studied, whereas for CLICpix2 the full detector front-end is involved, and the resolution is also affected by e.g. the frequency of the TOA clock. The detection efficiency of the matrix is larger than 99 % [15], without apparent substructure over the pixel matrix, as illustrated in Figure 10c.



(a) (b) (c)

Figure 10: Test beam results on (a) resolution, (b) timing and (c) efficiency obtained with the analog Investigator test chip fabricated in the modified HR-CMOS process on a 25 µm epi substrate for a matrix with 28 µm pixel size [15].

The promising results achieved with the high-resistivity CMOS Investigator chip triggered the design of a fully integrated chip specifically targeting the requirements of the CLIC tracker, using the same modified HR-CMOS process. The design implements elongated pixels of size 30 µm × 300 µm with simultaneous energy and time-of-arrival measurement. In order to maintain high detection efficiency, fast timing and low capacitance, the pixels are formed out of ten 30 µm × 30 µm sub-pixels. Each sub-pixel contains an individual analog front-end based on a charge sensitive amplifier. To maintain energy information per pixel, combining the sub pixel contributions in either analog or digital domain is foreseen.

4. Summary & outlook

The CLIC accelerator provides a unique potential for discoveries and precision physics at the TeV scale, but imposes challenging detector requirements on spatial and timing resolution, material budget and power consumption in the vertex and tracking detector. A comprehensive R&D effort for the CLIC vertex and tracking detector on sensors and readout chips is pursued, with focus on hybrid readout for the vertex detector and fully integrated CMOS sensors for the tracker.

The second generation of active HV-CMOS sensors and readout ASICs for the CLIC vertex detector has been produced, and is currently being characterized in laboratory and test beam mea-

surements. First results obtained in standalone measurements and in capacitively coupled detector assemblies show the expected performance of the devices, however the position resolution target of 3 µm has not yet been achieved with thin sensor layers. C3PD chips on higher resistive substrate up to the kΩ range will be produced. The resulting larger signal is expected to make the assemblies more robust against variations in the gluing process. In addition, bump-bonding of planar sensors to CLICpix2 chips is currently ongoing, which simplifies the charge collection studies and allows for a better calibration of the detector front-ends.

The design of a fully integrated prototype chip for the CLIC tracker based on a high-resistivity CMOS process is advancing. Results achieved with an analog test chip in the chosen 180 nm CMOS technology indicate that a pixel size of 30 µm is sufficient to reach the resolution target of 7 µm. In parallel, good performance of a Silicon-on-Insulator test chip lead to the design of a larger prototype matrix, targeting both the CLIC vertex and tracker detector.

Acknowledgments

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References

[1] M. Aicheler et al., *A Multi-TeV Linear Collider Based on CLIC Technology: CLIC Conceptual Design Report*, CERN-2012-007.

[2] L. Linssen et al., *CLIC Conceptual Design Report: Physics and Detectors at CLIC*, CERN-2012-003.

[3] M. J. Boland et al., *Updated baseline for a staged Compact Linear Collider*, CERN-2016-004.

[4] N. Alipour Tehrani et al., *CLICdet: The post-CDR CLIC detector model*, CLICdp-Note-2017-001.

[5] F. Duarte Ramos, W. Klempt and F.-X. Nuiry, *Experimental tests on the air cooling of the CLIC vertex detector*, CLICdp-Note-2016-002.

[6] A. Nurnberg and D. Dannheim, *Requirements for the CLIC tracker readout*, CLICdp-Note-2017-002.

[7] P. Valerio et al., *A prototype hybrid pixel detector ASIC for the CLIC experiment*, *Journal of Instrumentation* **9** (2014) C01012.

[8] M. D. Buckland, *TCAD simulations of High-Voltage-CMOS Pixel structures for the CLIC vertex detector*, CLICdp-Note-2016-004.

[9] I. Kremastiotis et al., *Design and standalone characterisation of a capacitively coupled HV-CMOS sensor chip for the CLIC vertex detector*, *Journal of Instrumentation* **12** (2017) P09012.

[10] M. Vicente Barreto Pinto, *Finite-element simulations of coupling capacitances in capacitively coupled pixel detectors*, CLICdp-Note-2017-003.

[11] S. Bugiel et al., *Development of SOI pixel detector in Cracow*, arXiv:1507.00864.

[12] R. Bugiel et al., *Test-beam results of a SOI pixel detector prototype*, Tech. Rep. CLICdp-Pub-2018-001, CERN, Geneva, Mar, 2018.

[13] W. Snoeys et al., *A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance*, *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* **871** (2017) 90 – 96.

[14] B. Abelev et al., *Technical Design Report for the Upgrade of the ALICE Inner Tracking System*, Tech. Rep. CERN-LHCC-2013-024. ALICE-TDR-017, Nov, 2013.

[15] R. M. Munker et al., *Study of the ALICE Investigator chip in view of the requirements at CLIC*, CLICdp-Note-2017-004.