PROCEEDINGS OF SCIENCE

The LHCb Vertex Locator Upgrade

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The Vertex Locator (VELO) surrounding the interaction region is used to reconstruct the collision points (primary vertices) and decay vertices of long-lived particles (secondary vertices) of the LHCb experiment. The VELO detector will be changed for the upgrade of the LHCb experiment to be able to run at 5 times higher instantaneous luminosity. The modules will be equipped with 4 silicon hybrid pixel tiles, each read out by 3 VeloPix ASICs. The highest occupancy ASICs will sustain rates of 900 Mhit/s and produce an output data rate of over 15 Gbit/s, with a total rate of 2.9 Tbit/s anticipated for the whole detector. The VELO modules are located in vacuum, separated from the beam vacuum by a thin custom made foil. The foil will be manufactured through a novel milling process and possibly thinned further by chemical etching. The front-end hybrid hosts the VeloPix ASICs and a GBTx ASIC for control and communication. The hybrid is linked to the the the Opto-and-Power Board (OPB) by 60 cm electrical data tapes running at 5 Gb/s. The tapes must be vacuum compatible and radiation hard and are required to have enough flexibility to allow the VELO to retract during LHC beam injection. The OPB is placed immediately outside the VELO vacuum tank and performs the opto-electrical conversion of control signals going to the front-end and of serial data going off-detector. The board is designed around the Versatile Link components developed for high-luminosity LHC applications. From the OPB the detector data are sent through 300 m of optical fibre to LHCb's common readout board (PCIe40). The PCIe40 is an Altera Arria10-based PCI-express control and readout card capable of 100 Gb/s data throughput. The PCIe40 firmware is designed as a series of common components with the option for user-specific data processing. The common components deal with accepting the input data from the detector over the GBT protocol, error-checking, dealing with reset signals, and preparing the data for the computing farm. The VELO specific code would, for example, perform clustering of hits and time reordering of the events scrambled during the readout. An additional challenge of the sensor design is the non uniform nature of the radiation damage, which results in requiring a guard ring with excellent high voltage control. The performance of the prototype sensors has been investigated in a test beam, exploring tests of irradiated samples.

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1. Introduction

LHCb experiment is single-arm spectrometer designed to study CP-violation and search for New Physics phenomena in the heavy flavour (beauty and charm) quark sector. The detector consists of a tracking system (VELO and ST), two RICH detectors for particle identification, electromagnetic and hadronic calorimeters and a muon system [1]. The experiment has been running successfully since 2009, producing a variety of results. LHCb will be upgraded to further the physics performance during the Long Shutdown 2 (LS2), currently scheduled for 2019–2020 [2]. The luminosity will increase to 2×10^{33} cm^{-2} s^{-1}, which is a factor five larger than present. Thanks to a more efficient software trigger, this will lead to an increase of the yield by a factor 10 to 20, depending on the process of interest. We will improve considerably the trigger efficiency on hadronic channels and on rare decay and we will expand the scope to the lepton flavour sector, electroweak physics, QCD and exotics searches.

The current limitation of LHCb is the 1 MHz L0 hardware trigger output. So, we will remove this trigger and readout an event at every bunch crossing (40 MHz) using an efficient fully software trigger. This requires new front-end electronics and new DAQ system. In figure 1, we show the general components for the upgrade that would be common for all the LHCb subdetectors.

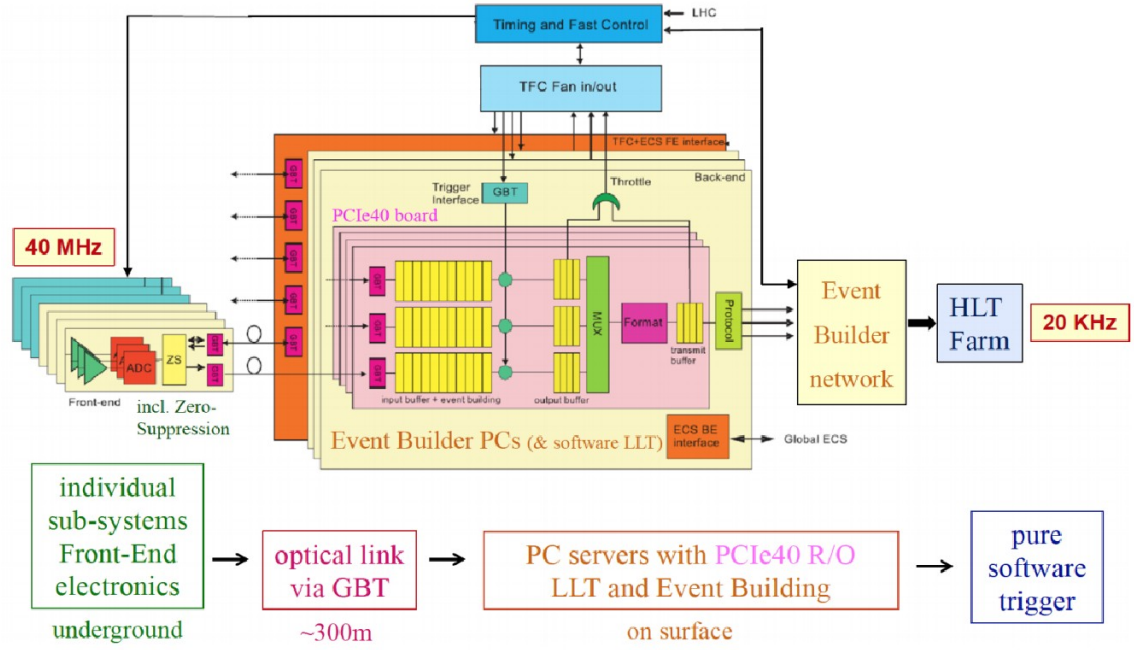

Figure 1: LHCb general components for the upgrade.

2. Current Vertex Locator (VELO)

The main task of the VELO is to enable LHCb to reconstruct and trigger on displaced vertices. The VELO surrounds the interaction region and consists of an array of silicon-strip sensors with a pitch of 40-100 µm with the first sensitive strip at 8.2 mm from the beam. The current VELO detector consists of 42 modules each equipped with two silicon strip sensors:

with one sensor the radial and with the other the azimuthal angle is measured (figure 2). The detector is divided in two moveable halves, which allows to retract each of them by 3 cm during injection and tuning of the LHC beams. Once the beam conditions are stable, the halves are closed and centred around the luminous region. The VELO is contained within a secondary vacuum, separated from the main beam by a 300 μm RF foil and is cooled by CO_2, keeping the silicon strips at an operational temperature of ∼-7 ºC.

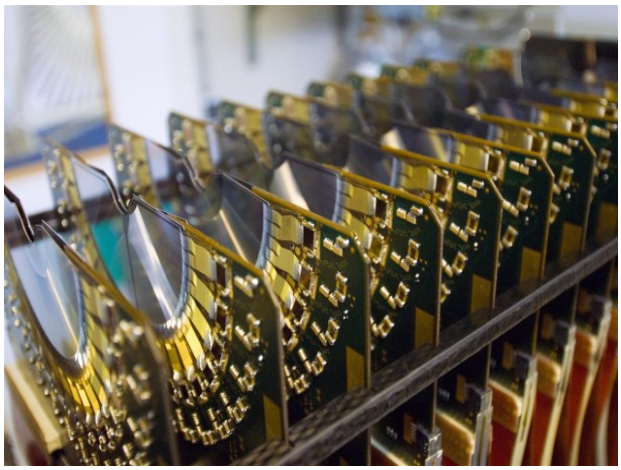

Figure 2: Picture of current VELO modules.

3. VELO upgrade

For the upgrade, the present VELO will be replaced by hybrid pixel detectors with planar silicon sensors [3]. As with the current VELO, the upgraded detector will be composed of two halves, which can be moved apart during beam injection and then returned to their nominal operating positions. Each half (figure 3) consists of a bank of 26 modules with a power disipation ~28 W each, separated from the LHC vacuum using a 250 um RF foil. The closest distance of the active silicon to the LHC beam will be reduced from 8.2 mm of the current VELO to 5.1 mm for the upgrade. A 200 μm n-on-p thinner silicon sensor will be bump bonded to a custom made VeloPix ASIC. The sensors and the ASICs have to carried with a non uniform dose ($\sim r^{-2.1}$) up to 400 Mrads for full lifetime. The readout chain of the VeloPix had to accomplish with the huge data bandwith, up to 20 Gbit/s for the central ASIC.

In the next subsection, the VELO components would be descrived:

- RF foil.
- VELO Module.
  - Sensors.
  - VeloPix ASIC.
  - Electronics.

- MiniDAQ.
- Cooling system.

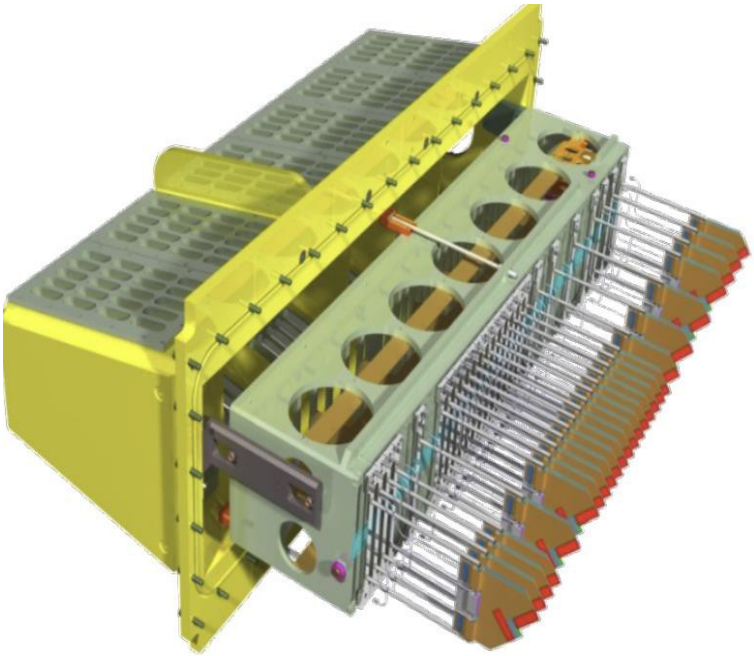

Figure 3: VELO half.

3.1 RF foil

Each VELO-half is surrounded by an RF foil that separates the ultra-high vacuum of the beam volume from the secondary vacuum of the VELO (figure 4). RF foil is milled from a single aluminium block, termally stable, conductive (guide the mirror currents and shield the detectors from possible RF pick-up) and radiation hard. Final model will be 250 µm uniformly thick to reduce the material budget. In figure 4, we show a prototype of the RF foil.

Figure 4: Prototype of the RF Foil.

3.2 VELO Module

In figure 5, we present an illustration of the VELO module. Each module is formed by a 200 µm n-on-p silicon sensors bump bonded to a custom made VeloPix ASICs and the electronics to control and readout the chip. The module layout of the sensors is an L shape geometry with four sensor tiles, two on each side. Each tile consists of three Velopix ASICs connected to a sensor. The VeloPix, based on the Timepix3, consists of a matrix with 256x256 pixels with a pixel size of 55x55 μm^2. The VeloPix is thinned to 200 µm to reduce the material budget and it is made in 130 nm CMOS technology. The ASICs are mounted on a cooling substrate of silicon to reduce the CTLE mismatch, etched with internal CO_2 microchannels, on which are also mounted the hybrid boards which provide the low and high voltage power and the control and readout communication. After the hybrid module we have all the rest of connectivity and electronics: flex cables, vacuum feed-through board and opto-and-power board.

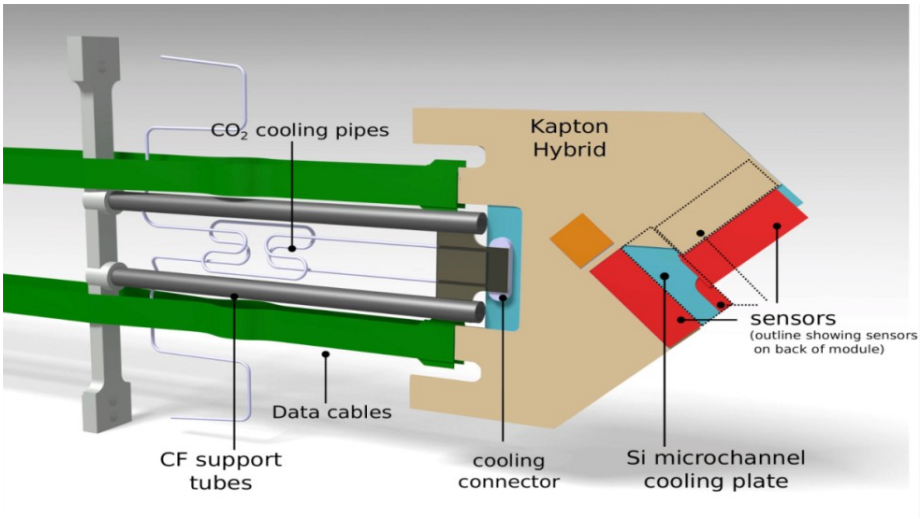

Figure 5: VELO module.

3.2.1 Sensors

The sensors will be 200 µm thick n-on-p silicon pixel (~43x14 mm) bump bonded to three ASICs to mimimize the dead regions. A range of prototype sensor from Hamamatsu (HPK) and Micron had been tested using the Timepix3 telescope before and after irradiation with protons and neutrons in different facilites [4]. Apart from the non-uniform radiation damage, the sensors have to keep with the next benchmarks:

- High enough charge collection efficiency after irradiation (6000 e^-).
- Tolerate high bias voltage (1000 V).
- High cluster finding efficiency after irradiation.

3.2.2 VeloPix Asic

The VeloPix Asic is a 130 nm CMOS technology chip based on Timepix3 [5]. The readout architecture is data driven, zero suppressed, continuous, binary and tigger-less. The power consumption per chip is < 2W. The chip is optimised for electron collection, radiation tolerant up to 400 Mrad and protected from single event effects. The highest occupancy chips will have

hit rates up to 900 Mhits/s/chip and produce rates over 15 Gbit/s. So, a dedicated output serialiser had been implemented using four Gigabit Wireline Transmitter (GWT) at 5.12 Gbit/s. Moreover, to reduce the data rate, a super pixel common logic and layout have been implemented using 2 col x 4 row pixels. The first VeloPix ASIC design was received in September 2016. After a extensive tesing, a new version of the design was send in July 2017.

Measurements of the first prototype were taken using the Speedy PIxel Detector Readout (SPIDR)-readout system and with the first prototypes of the real system. All digital and analogue functionality has been validated and conforms the specifications. Low temperature up to –40ºC have been tested in a climatic chamber. A wafer probe card have been designed and successful tesed.

A Total Ionzing Dose test had been done with a X-ray machine at Glasgow University in December 2016. We irradiated the chip up to 400 Mrad with no change in digital power consumption and no drift in analogue parameters as pixel thresholds, noise and global DACs.

A high speed beam test had been done in Fermilab with 5 planes VeloPix telescope with rates up to 300 Mtracks/s.

Single Event Effects test have been conducted at the Heavy Ion Irradiation Facility (HIF) in Louvain-Le-Nueve using diferent types and angles of heavy ions. The first aim of the test was to determine the cross-section for single event upset (bit-flip) in the chip registers. But we found some issues: Single Event Latch-up (SEL), Large cross-section for the SLVS receiver and small design flaws in the state machines. We have corrected this issues and sent a new design for production.

In terms of high speed test of the GWT transceiver, we found excesive jitter due to the too much cyle-to-cyle period variation of the internal 320 MHz clock that comes form the noise in the VCC and GND bouncing. We lowered the error rate to almost zero by tuning an internal clock phase. For the next version, we have added extra on-chip decoupling, splitting of internal supplies in ePLL, shorter bond wires and add external decoupling; and smaller and slower clock buffers (smaller current peaks, and spread in time and small penalty in clock skew, hence timewalk) to eliminate the jitter.

3.2.3 Electronics

The schematic of the electronics is show in figure 6 [6]. The first electronic part of the VELO module is the front end hybrid (figure 7). Each VELO module has two hybrids. Each hybrid is made of one GBTx chip and two silicon pixel sensors bump bonded to 3 VELO ASICs. One option being considered for the hybrid design is to split it in 3 pieces (Two for sensors and one for GBTx). This 3 pieces option is less rigid than a single module, so less sensitive to deformation, fewer layers, less area and Cu; but, it has more connectors. The hybrid is connected to a flex tape, designed at CERN and USC, firt prototypes were produced at CERN and now in industry. This flex cable have to carry with the movement of the detector, ~5% of the cable length, transmit high-speed signals and have low material budget. A differential strip is been used as a transmission line. In the exit side of the cable, we use a vacuum feed through board to take out of the vacuum the power, control and DAQ signals. A special vacuum flange was designed for this purpose (figure 7). The feedthrough is connected outside of the vacuum with an opto-and-power board. This board supply the low voltage to the hybrid and convert the electrical signals from the hybrid to optical signal and viceversa. The power supply distribution

is done using CERN FEASTMP radiation hard DC-DC converters. For the optical conversion a cern radiation hard VTRx and VTTx componets are used. The opto-and-power board are connected to main low voltage power supplies and to the control and DAQ system prototype (MiniDAQ).

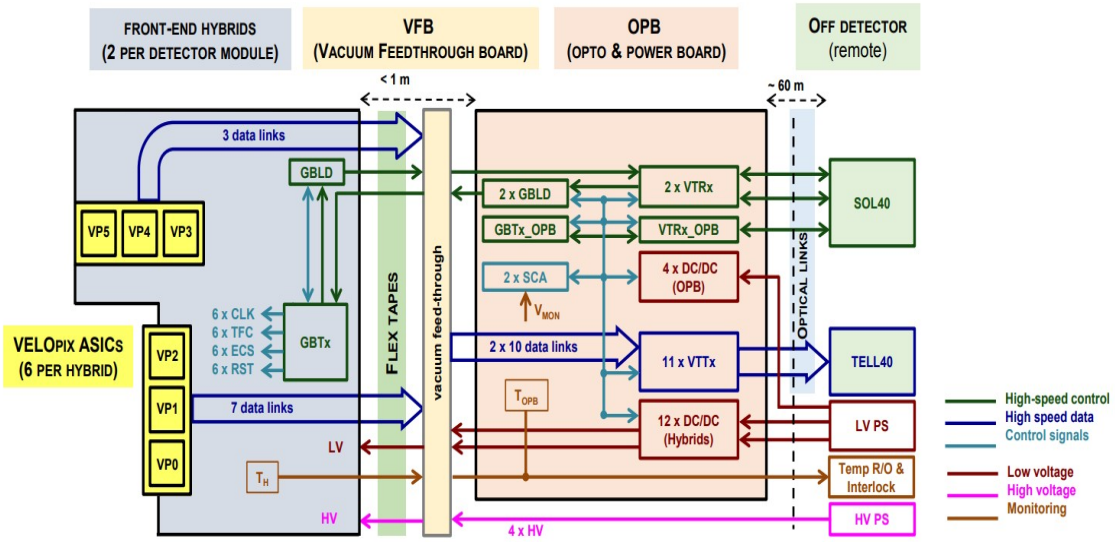

Figure 6: VELO electronics schematic.

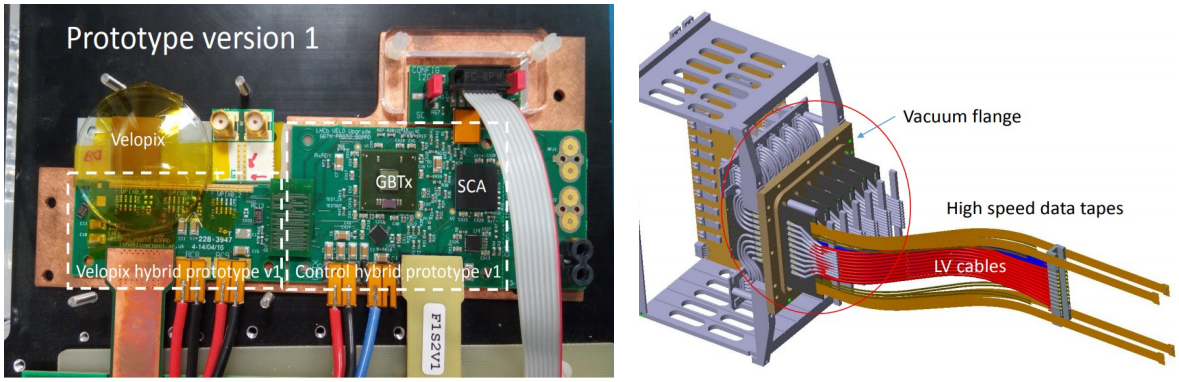

Figure 7: Prototype of the hybrid (left) and design of the vacuum feed through.

3.3 MiniDAQ

The DAQ controls the hybrid (SOL40) and acquires and processes the data (TELL40) using a FPGA [7]. The SOL40 system uses the LHCb standard protocol (GBT) to communicate with the GBTx ASIC while the TELL40 system uses the VELO specific protocol (GWT) to receive data from the VeloPix ASIC. The TELL40 is in charge of collecting, decoding, reordering, processing and packing the incoming data before being sent to the computer network. Due to the specific protocol and the out of order arrival of data, the VELO detector has much more specific code inside the LHCb common framework (figure 8) than other detectors. A prototype version (MiniDAQ) of the final system has been tested while the final one is under development.

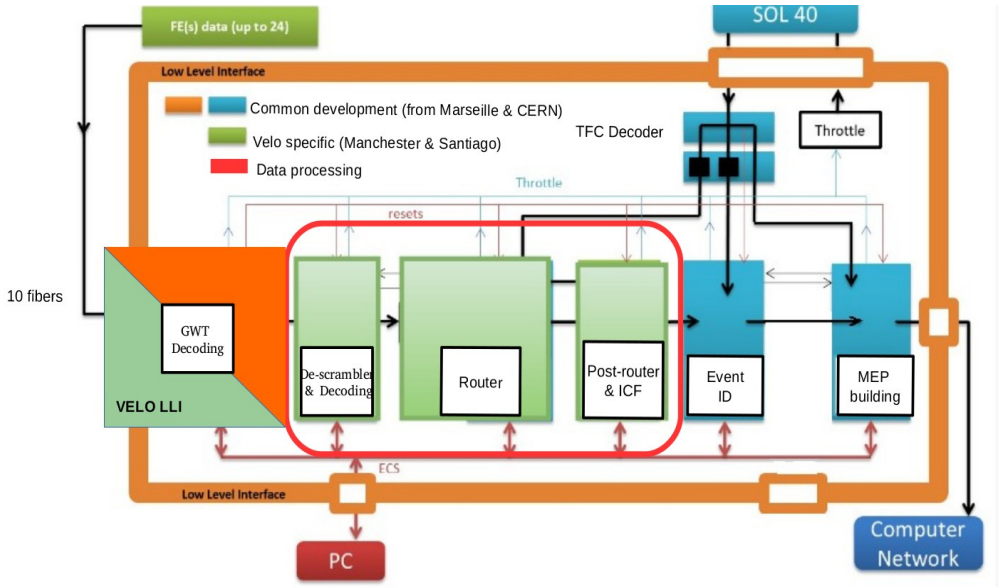

Figure 8: TELL40 scheme of the MiniDAQ.

3.4 Cooling system

Each module of the upgraded VELO detector dissipates 28W and the full detector 1.6 kW. It is needed to keep the sensors bellow -20ºC to minimize the radiation damage. Moreover, the cooling system must operate close to the beam and in vacuum. So, different options of cooling are under investigation to meet this specification [8].

3.5 Conclusion

In the Long Shutdown 2 (LS2), a new VELO detector will upgrade the current one from a silicon strip to a silicon pixel detector. The new VELO will have significant improvements over the present:

- Greater radiation tolerance.
- Increased Readout Rate (1 MHz to 40 MHz).
- Better impact resolution (Closer to Beam).

Prototypes for all components have been produced and are under testing. We are testing the sensors quality in terms of irradiation tolerance, maximum bias voltage and efficiency after irradiation, using test beam telescopes. The VeloPix ASIC has been tested, redesigned and a new version was submitted. The readout electronics and data transmission is under test to verify the specifications of the high speed signals. Different cooling systems have been proposted and we will use the micro-channel cooling one.

The production, reception, qualification and assembly steps are moving in parallel because our schedule is tight.

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