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Readout Electronics of DAMPE BGO Calorimeter and the Status during the First 18 Months in Orbit

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Abstract: The DAMPE (DArk Matter Particle Explorer) is a scientific satellite which was successfully launched in Dec., 2015, with the major scientific objective of indirect searching for the clue of dark matter particles in space. The BGO (Bismuth Germanate Oxide) calorimeter is a critical sub-detector of DAMPE payload, with the functions of measuring the energy of cosmic particles, distinguishing positrons/electrons and gamma rays from hadron background, and providing trigger information. It is composed of 308 BGO crystal bars and each bar is coupled by two Hamamatsu R5610A PMTs (photomultiplier tubes), from both sides respectively. Each PMT sends out three dynode signals, to achieve a large dynamic range, which results in 1848 signal channels. A readout electronics system, which consists of 16 FEE (Front End Electronics) modules, is designed to precisely measure the charges of PMT signals and to provide "hit" signals. The in orbit status of the electronics system is to be introduced in this paper.

Keywords: DAMPE, Calorimeter, Readout Electronics, Dark Matter

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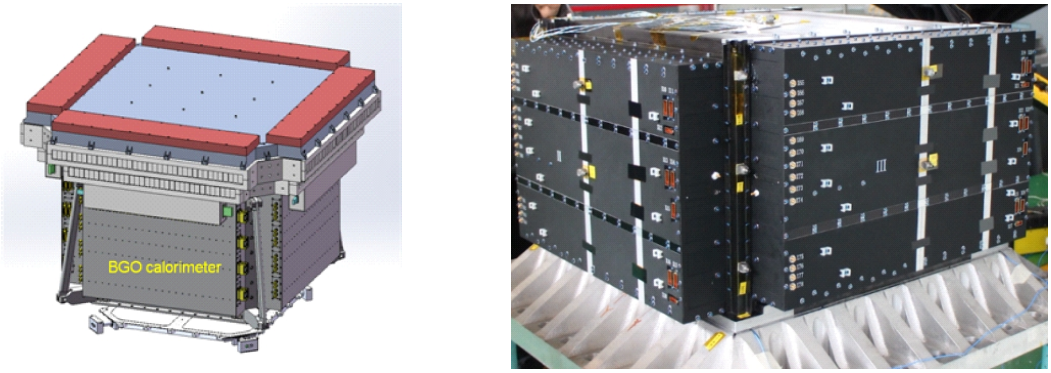
1. Introduction

The DArk Matter Particle Explorer (DAMPE), nicknamed 'Wukong' in Chinese, is a scientific satellite which was successfully launched into a 500 km sun-synchronous orbit, on December 17th, 2015, from the Jiuquan Satellite Launch Center of China. The scientific objectives of DAMPE mission are cosmic ray study, gamma ray astronomy, and searching for the clue of dark matter particles by precisely measure the energy spectra of electrons/positrons and gamma rays with the energy range from 5 GeV to 10 TeV.

The BGO calorimeter, with the weight of 1.05 ton, is composed of 308 BGO crystal bars and each bar is viewed by two Hamamatsu R5610A PMTs (photomultiplier tubes) from both ends respectively. Each PMT sends out three dynode signals, to achieve a large dynamic range up to about 2×10^5 [1], which results in 1848 signal channels.

Fig. 1(a) shows the 3D (three dimension) structure of the DAMPE payload, while Fig. 1(b) is a photograph of the flight model of the BGO calorimeter which is assembled on a vibration facility during ground-based environmental tests.



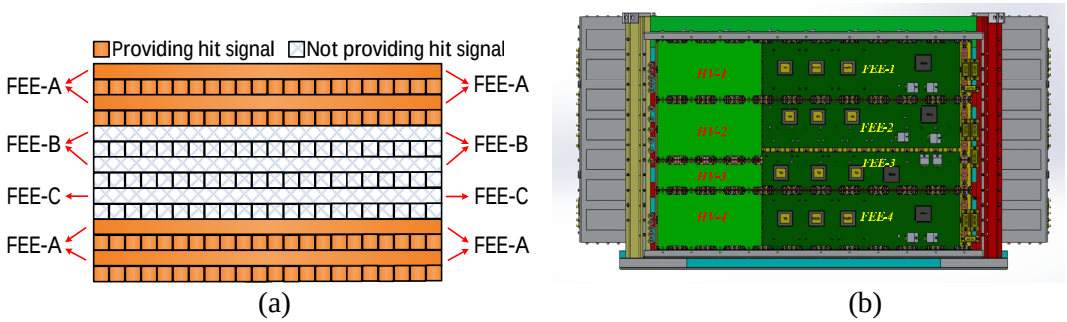
(a) (b)

Fig. 1 (a) 3D structure of the DAMPE payload; (b) photograph of the BGO calorimeter flight model

2. Readout electronics of BGO calorimeter

In order to meet the readout requirements of BGO detector, and considering the strict constrains for satellite-borne experiments, a readout system was designed [2], with three types of FEE (Front-End Electronics) modules named FEE-A, FEE-B and FEE-C respectively.

Fig. 2(a) illustrates the configuration of the BGO detector and its readout electronics. All the 308 BGO bars are stacked in 14 layers, with 22 BGO crystals in each layer, and every two adjacent layers are oriented perpendicularly. There are four FEE modules assembled on each side of the BGO detector, including two FEE-A, one FEE-B and one FEE-C. FEE-A and FEE-B both receive the PMT signals from two adjacent X or Y layers, while FEE-C just reads out the signals from one single layer. In addition to the function of precisely measuring the charge of PMT signals, the FEE-A module needs to provide "hit" signals as well, which indicate that the corresponding layers are hit by particles. Fig. 2(b) shows how the circuit boards are installed, including the four HV (High Voltage) Fan-out boards and four FEE modules assembled from top to bottom on each side.



(a) (b)

Fig. 2 (a) Configuration of the BGO FEEs; (b) Circuit boards installed with BGO detector

A photograph of one FEE-A module for the qualification-model is shown in Fig. 3. Three front-end ASIC chips, one VA160 and two VATA160, are mounted on top side while another three ones are mounted on bottom side. In a single layer, PMT dynode signals from dynode 2, 5 and 8 are sent to the three ASIC (top or bottom side) from left to right respectively. For the FEE-B module, six VA160 chips are employed, while just three VA160 chips are employed for the FEE-C. The control logic of the FEE module is implemented in an Actel Flash-based FPGA (APA600 for FEE-A, and APA300 for FEE-B/C). A calibration circuit for VA160 and VATA160 ASICs is adopted, which is also used to check the functions of ASIC chips on orbit [3].

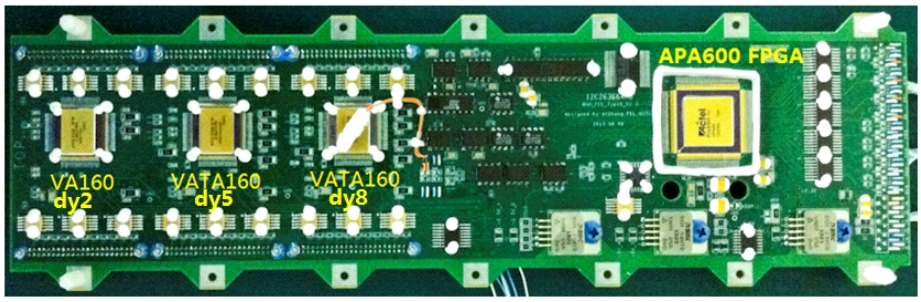


Fig. 3. Photograph of the qualification-model of an FEE module (Type A)

Both the VA160 and VATA160 ASICs were designed by IDEAS Inc. in Norway and fabricated with AMS 0.35um CMOS process, in 2013 [4]. The wafers were thinned, cut into dies and then the bare dies were shipped to China. After the arriving of ASIC dies, a series of quality control measures were taken, such as SEM (scanning electron microscope) check for 8 samples, and visual inspection for all bare dies. Only the dies that passed the visual inspection were encapsulated with ceramic packages (CQFP128). Finally, a series of lot screening for VA160 and VATA160 were carried out [5, 6], obeying the regulations from appendix A of GJB-548B-2005.

A series of radiation tests, including total dose (TID) tests and single event effect (SEE) tests, were conducted both for the ASICs and for the FPGA chips [7, 8]. Based on the test results, several effective protection or mitigation methods were taken for the FEE design, such as current monitoring and latch-up protection circuit for the ASICs, TMR (triple module redundancy) for the logic design, etc. Beside the current monitoring function, other information of the FEE, such as temperature and the values of the status registers are acquired by the FPGA logic and sent to PDPU as well.

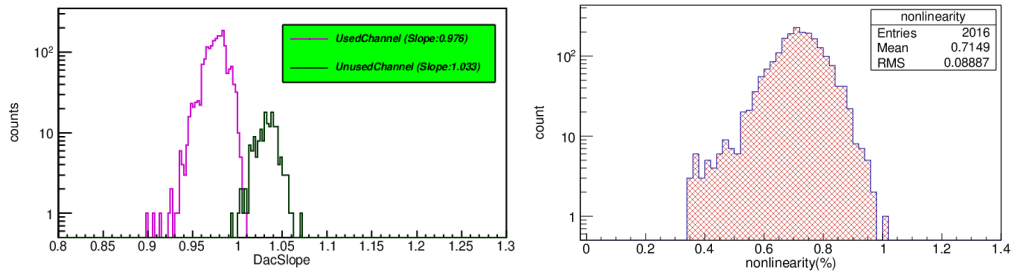
3. Performances of the readout electronics before and after launching

After assembly, integral tests and satellite-level environmental tests were successfully

conducted for the BGO calorimeter together with other sub-systems. Then the flight model of DAMPE satellite was transported to Jiuquan Satellite Launch Center in mid-November, 2015.

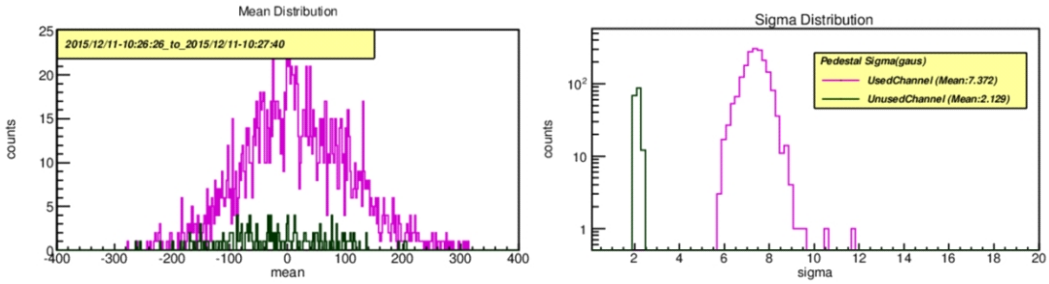
The readout electronics of the BGO calorimeter, operation with the detector, performed well during the ground-based tests which lasted successively for nearly one month before launching.

Fig. 4(a) shows the statistic histogram of FEE calibration slope (ADC bins per fC) of all the 2016 FEE channels (including 1848 used channels and 168 spare channels), while Fig. 4(b) shows the distribution of the INL (integral nonlinearity) values of all the channels. The maximum INL value is about 1%, which is much less than the design specification (2%). Fig. 5(a) illustrates the distribution of the pedestal mean values of all the FEE channels during ground-based tests, while Fig. 5(b) illustrates the distribution of pedestal noises, while the noises are much less than the MIP signal (equvalent to 100 fC or above) and meets the design specifications.



(a) (b)

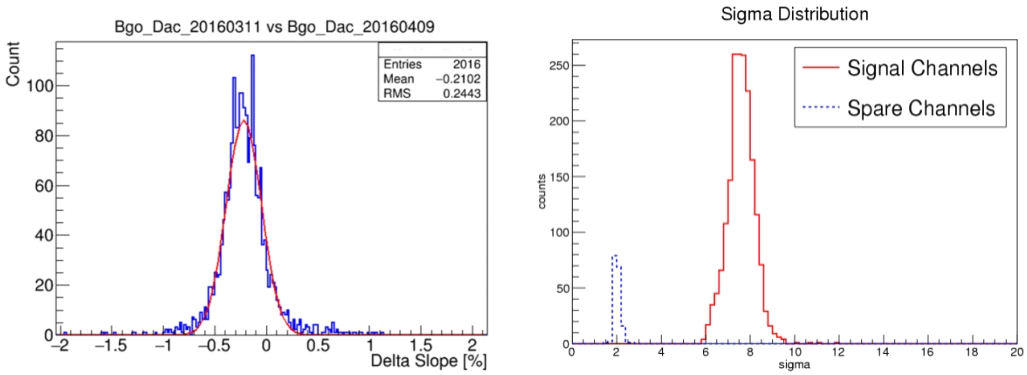
Fig.4 FEE Calibration result before launching: (a) Distribution of slopes; (b) Distribution of INLs



(a) (b)

Fig.5 Pedestal results before launching: (a) Distribution of mean values; (b) Distribution of noises

After sufficient ground-based tests, the DAMPE satellite was successfully launched. According to the operation plan, the readout electronics of BGO calorimeter was powered up three days after launching, and the high voltage supply of the BGO detector was turned on a week after launching. The readout electronics functioned well and the performances of all the FEE channels were consisted with the ground-based test. Fig. 6 (a) shows that the differences of the calibration slopes between in-orbit tests and ground-based tests are all less than 1%. The results of in-orbit pedestal tests are shown in Fig. 6 (b) as well, which are almost the same as Fig. 5.



(a) (b)

Fig.6 (a) Variation of the FEE calibration slopes after launching; (b) Distribution of pedestal noise

4. SEL and SEU events in orbit

Since radiation tests suggested that both VA160 and VATA160 ASICs are sensitive to single event latch-up (SEL), effective SEL protection method was taken for the FEE module. A current sensing circuit was designed for monitoring the supply currents of VA160/VATA160 ASICs. The ASICs will be automatically powered off within 100 us after lach-up, and be powered on after waiting for 100 ms, all by the control of FPGA logic. For each FEE module, a 4-bit counter is used in the FPGA logic to permanently record the number of SEL events unless it is cleared by remote command or the FEE module is powered down.

For the ASIC design by IDE AS, TMR (Triple Modular Redundancy) and auto-correction method is adopted for the 165-bit configuration registers of VATA160 chip. The same methods, as well as CRC (Cyclic Redundancy Check), were taken for the FPGA logic design, such as the high threshold and low threshold configuration parameters which were stored by the block RAM, and the registers for VATA160 configuration which are implemented by programmed DFFs. For each FEE, a 8-bit counter is adopted in the FPGA to record the number of VATA160 SEU events, while another 4-bit counter is used to record the SEU of threshold configuration file.

For the VATA160 ASIC, there is 495 bits per chip, while there are 15840 bits in total for the 32 VATA160 chips (8 FEE-As) assembled for the BGO calorimeter. In the FPGA logic, there are originally one byte high threshold value and one byte low threshold value for each FEE channel and two bytes of CRC codes for each type of threshold for each FEE. In total 98304 bits are stored by the FPGA block RAM for the 2016 FEE channels of the BGO calorimeter, considering the TMR design.

During the one and a half year (18 months, also equals to about 550 days) in-orbit operation, one SEL event for the ASICs and two SEU events for the RAM have been recorded. However, no SEU event has yet been found, either for the VATA160 configuration registers of FPGA, or for the registers in the ASIC chips. The first SEL event was found to occur and quickly recover as expected, on June 5th, and the two SEU events occurred on April 21st and June 28th, all in this year.

Using CRÈME96 we have predicted that SEU probability for the DFFs in APA FPGA chips is about 6.8×10^{-7}/(bit*day) in the DAMPE orbit [9], based on the assumption of the SEU threshold value of about 3 MeV*cm^2/mg, and the SEL probability for VA160 is about 2.7×10^{-5}/(device*day) for VA160 and 8.1×10^{-5}/(device*day) for VATA160. We can roughly calculated out that the SEL probability is about 2×10^{-5}/(day*device) for the 84 ASIC chips in total, and the SEU probability

for the FPGA block RAM is about 2×10^{-8}/(day*bit), which are approximately consistent with predication.

5. Conclusion

The readout system for the BGO Calorimeter of DAMPE satellite was successfully designed and developed, obeying the regulations for aerospace electronics. The readout system passed a series of ground-based tests before launching and right now performs well in orbits. Based on the strict quality control procedure, and with the properly designed SEL and SEU protecting methods, the readout system operates stable in orbit and plays an important role for the scientific observation of DAMPE satellite.

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