PROCEEDINGS OF SCIENCE

Firmware Development for the first level trigger of ATLAS LAr Calorimeter

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The LHC Run3, which is scheduled to be 2021-2023, is expected to have two times higher instantaneous luminosity $\mathscr{L} = 3.0\times10^{34}$ cm^{-2}s^{-1} than Run2. This leads a large drop on the acquisition efficiency of W / Z boson events at the first level trigger of the ATLAS Liquid Argon calorimeter. In order to tolerate an increasing instantaneous luminosity, the trigger readout is upgraded to read 10 times finer granularity than the current trigger readout. This leads to the improvement of a separation power between EM objects (electron, photon) and hadronic jet.

A FPGA firmware which manages huge data (RX : 5.12 Gbps$\times$96, TX : 11.2 Gbps$\times$96) with a fixed latency is in the backend electronics of the upgraded trigger readout. We implemented a multi-stage impulse response filter with high-speed links to convert digitized signals into deposited E_T at a correct bunch crossing of LHC beams. The designed firmware satisfies the requirements of the fixed latency, FPGA resources and the maximum operation frequency. We confirmed the stability of the firmware on a hardware.

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1. Introduction

Large Hadron Collider (LHC) at CERN is an energy frontier hadron collider with the center-of-mass 13 TeV, which is the highest energy in the world. The LHC Run2 has been started since 2015, expected to be until 2018. Then, the 2nd long shutdown (LS2, 2019-2020) for LHC maintenance and detector upgrade will be taken for Run3 (2021-2023) expected to have two times higher instantaneous luminosity, $\mathscr{L} = 3.0\times10^{34}$ cm^{-2}s^{-1} compared to Run2. In the LS2, the upgrade of the trigger readout for the Liquid Argon (LAr) calorimeter at the LHC-ATLAS experiment is planned to improve the first level trigger (L1) performance. Because of limitation on the trigger rate, the transverse energy (E_T) threshold needs to be raised for a higher luminosity, which leads a large drop on the acquisition efficiency of W / Z boson events. Instead of raising the E_T threshold, enhancing separation power between EM objects (electron, photon) and hadronic jets can reduce the trigger rate. In the new upgraded trigger, we digitize the analog signal at frontend electronics, and make real time digital signal processing at the backend electronics. This minimizes noise contributions and also makes higher granularity readout possible. By using the shower shape characteristics on EM objects and jets, we can keep the trigger rate at the same level as Run2 having the same or better W / Z efficiencies at Run3 (Figure 1).

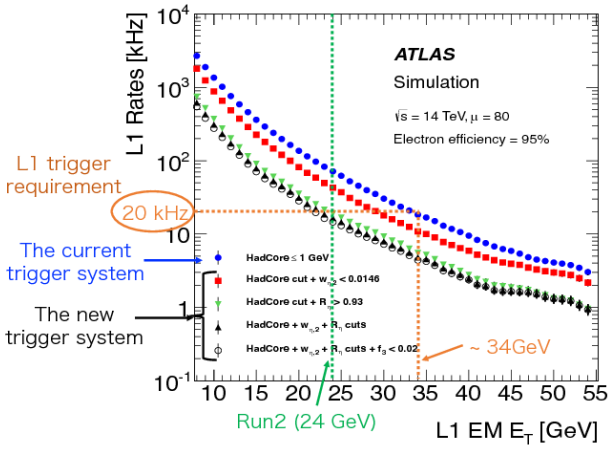

Figure 1: The expected L1 trigger rate as function of E_T in the Run3 condition at ATLAS [1]. At the L1 trigger, the trigger rate of EM objects is required to be 20 kHz or smaller.

2. New trigger readout scheme and readout electronics

The ATLAS LAr calorimeter consists of four layers, and each layer is segmented in pseudo-rapidity (η) and azimuth (ϕ) directions. The current trigger readout, where the unit of the readout segment is called "Trigger Tower", makes analog sum over cells of the 4 layers in a range of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ at the frontend electronics. The summed analog signals are sent via co-axis cables to the backend electronics, then digitized with 40 MHz, which is a beam crossing rate at LHC. In the new trigger readout, the summed analog signals are digitized for each layer separatly

at the frontend electronics and transferred to new backend electronics via optical fibers. In addition, the range of the sum for the first and second layers is changed to be finer, $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$. This new trigger readout unit is called "Super Cells". One trigger tower corresponds to 10 super cells (Figure 2).

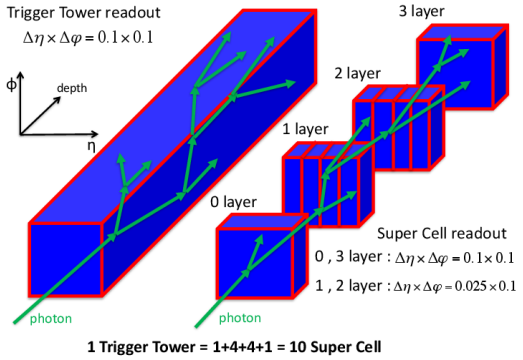

Figure 2: LAr readout scheme

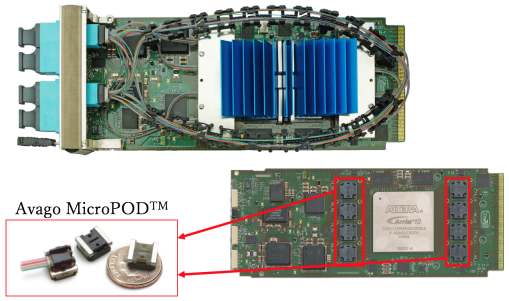

Figure 3: Backend board (LATOME) [1]

The main task of the new backend electronics is to convert the digitized signals into the deposited E_T at a correct bunch crossing (BC) of beams with fixed latency of ~125 ns, and transfer E_T information to L1 trigger at 11.2 Gbps. Figure 3 shows a mezzanine card, LATOME, developed for the new backend electronics. The task is performed with the ALTERA (INTEL) Arria10 Field Programmable Gate Arrays (FPGAs) installed in the LATOME. Tokyo groups works on the firmware development of the FPGA and we report the first version of the firmware in the paper.

3. Real time digital signal processing

The amplitude of the LAr calorimeter pulse and E_T have a linear relation, therefore it is important to measure the height of the LAr pulse. The timing of the peak of the LAr pulse carries information of bunch crossing at which the pulse is injected. An optimal filtering technique (OF) [2] is used to compute E_T (Figure 4). The E_T and relative phase τ are obtained from the following expressions:

$$E_{\mathrm{T}} = \sum_{i=1}^{4} a_i (S_i - P), \tag{3.1}$$

$$E_{\mathrm{T}} \cdot \tau = \sum_{i=1}^{4} b_i (S_i - P), \tag{3.2}$$

where a_i and b_i are the optimal filter coefficients (OFC). S_i is the digitized signal of LAr calorimeter and P is a pedestal. Coefficients and pedestal are computed in advance.

The selection criteria for identifying a correct BC of the injected energy is optimized as follows:

$$\begin{cases} -2E_{\mathrm{T}} < E_{\mathrm{T}} \cdot \tau < 2E_{\mathrm{T}} \text{ for } 10\ \mathrm{GeV} \leq E_{\mathrm{T}} \\ -8E_{\mathrm{T}} < E_{\mathrm{T}} \cdot \tau < 8E_{\mathrm{T}} \text{ for } 0\ \mathrm{GeV} \leq E_{\mathrm{T}} \leq 10\mathrm{GeV} \\ 8E_{\mathrm{T}} < E_{\mathrm{T}} \cdot \tau < -8E_{\mathrm{T}} \text{ for } -1\ \mathrm{GeV} \leq E_{\mathrm{T}} \leq 0\mathrm{GeV}. \end{cases} \tag{3.3}$$

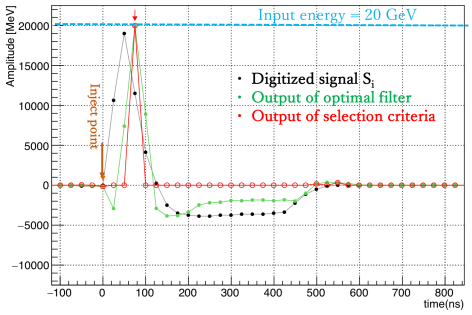

Figure 4: Digital signal processing

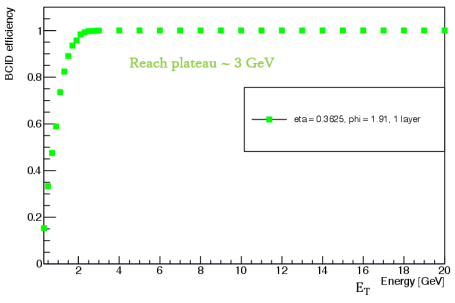

Figure 5: The E_T dependence of BCID efficiency

This selection criteria can be easily implemented on FPGA firmware by the bit shift operation. We evaluated this selection criteria, and found the identification efficiency of signal (BCID efficiency) reachs almost 100 % at E_T = 3 GeV (Figure 5).

4. Firmware development

One FPGA has to handle 320 Super Cells (SCs). It is impossible to process all SCs at the same time. By considering our components, we designed 62 parallel processing with serializing 6 SCs with 240 MHz (40 MHz $\times$ 6). By this design, the number of parallel processing is decreased and it can be implemented on the FPGA. Therefore, a firmware for 6 channel digital filtering was developed.

In order to implement the digital filtering efficiently, we use DSP blocks, which are elements for high-speed multiplication on the FPGA. We design the firmware by cascade connections of DSP blocks. This makes the wiring delay minimized, and all calculations done in DSP blocks (Figure 6). We achieved the latency of 87.5 ns, which satisfies a L1 trigger requirement. The usage of DSP block for 6$\times$ 62 super cells is 16.7 % in total, which allows to be implemented on the FPGA. The maximum operation frequency (F_{max}) is about 257.6 MHz. It means that the firmware works well with 240 MHz clock.

4.1 Test of the firmware with hardwares

We checked the firmware using the LATOME prototype and the Arria10 development kit (Arria10 Dev-Kit [3]) which uses the same FPGA as LATOME (Figure 7). For the hardware tests, we developed generator and checker firmwares. The generator firmware stores ADC data, coefficient and pedestal in Random Access Memory (RAM) and provides these inputs to the target firmware. On the other hand, the checker firmware stores answers obtained beforehand in RAM, and compares the outputs of the target firmware and answers. The checker firmware outputs a flag. In case that the firmware result is correct, the flag is set as 1, otherwise 0. The checker firmware also counts the number of errors (flag = 0). We confirmed that the development of the first version of the firmware was fully done for the super cell readout.

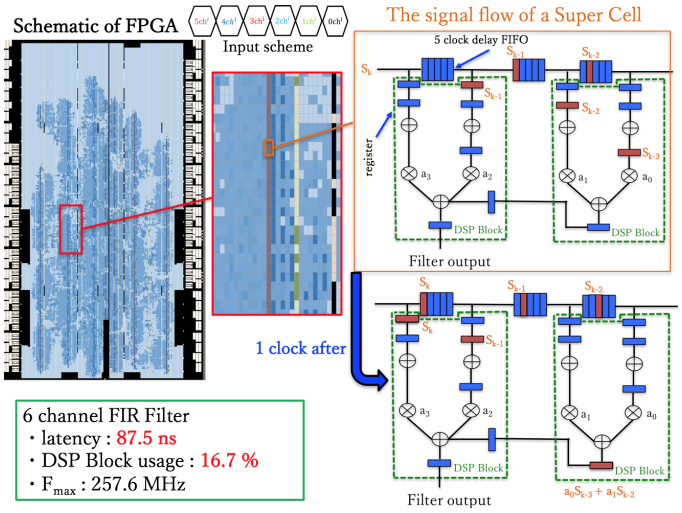

Figure 6: Design of 6 channel digital filtering using DSP blocks

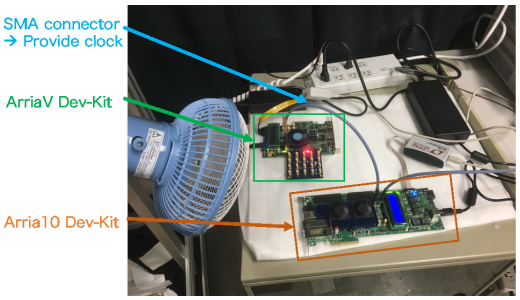

Figure 7: test environment with Arria10 Dev-Kit

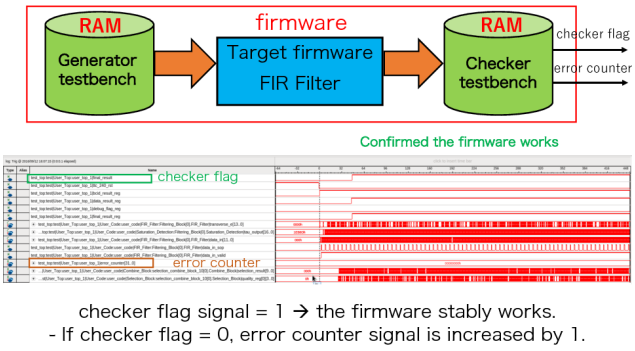

Figure 8: Workflow of test and the output of logic analyzer

5. Summary and prospect

We worked on the firmware development for the backend electronics of ATLAS LAr calorimeter in order to improve the performance of L1 trigger. The firmware calculates the transverse energy and identifies the BC of the injected energy with the fixed latency of 125 ns. We established the first version of firmware fulfilling all requirements, and confirmed stable running in the hardware test. The prototype hardware will be assembled soon and tested before starting mass-production. All hardwares should be verified by the end of 2018 and installed in 2020.

References

[1] ATLAS Collaboration, ATLAS LAr Calorimeter Phase-I upgrade TDR, CERN-LHCC-2013-017

[2] W.E. Cleland, E.G. Stern, Signal Processing considerations for liquid ionization calorimeters in a high rate environment, Nucl. Instrum. Meth.A 338 (1994) 467.

[3] Intel FPGA homepage, http://www.altera.com