

SOI Monolithic Pixel Detector Technology

Yasuo Arai¹, on behalf of the SOIPIX Collaboration

High Energy Accelerator Research Organization (KEK)

& The Okinawa Institute of Science and Technology (OIST)

1-1 Oho, Tsukuba, Ibaraki 305-0801, Japan

E-mail: yasuo.arai@kek.jp

Silicon-On-Insulator (SOI) technology has been regarded as a best match technology for monolithic radiation pixel detector from a very early stage. However, major issues can severely affect the operability of the detector, such as the back-gate effect, the coupling between sensors and readout electronics and Total Ionization effect (TID).

We proved to have solved these issues by developing new technologies such as buried well and double SOI wafer/process. Transistor performance degradation by radiation was studied in detail, and we can successfully increase radiation hardness more than 100 kGy(Si) by changing the dose level of the Lightly Doped Drain (LDD) region.

In addition, the layout size of the pixel circuit is shrunken by introducing PMOS and NMOS active merge technique. This enables much smaller layout size than conventional CMOS process while keeping high enough analog operation voltage.

The process technologies we developed and a few examples of SOI detectors are described.

The 25th International workshop on vertex detectors

September 26-30, 2016

Location

La Biodola, Isola d'Elba, ITALY

¹Speaker

© Copyright owned by the author(s) under the terms of the Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 International License (CC BY-NC-ND 4.0).

1. Introduction

Silicon (Si) pixel detectors are key devices in recent high-energy physics experiments to detect vertex locations of short-lived particles around the beam collision point. At present, they are mainly fabricated as a hybrid detector of Si sensor substrate and readout VLSI connected by bump bonding [1] as shown in Fig. 1-(a). Although the hybrid detector achieved very good performance in many experiments, they also met many limitations. The pixel size is limited by bump bonding technology to around 50 μm . Yield of millions of bump bonding is not so high, and the bump bonding process increases the cost of the detector and adds not negligible contribution to the material budget. Furthermore, it is difficult to test the sensor before bonding.

Many people have been trying to fabricate the radiation pixel detector as a monolithic device. However, it is not easy to build fully-depleted sensor with readout electronics in conventional CMOS process. Although CMOS monolithic detectors using epitaxial layer under transistors are successfully developed and used in a few experiments [2], the depth of the epitaxial layer is not thick enough ($\sim 10\mu\text{m}$) and charge collection is slow due to the thermal diffusion of the charge. Then the signal to noise ratio and timing performance are not so good. Pixel detectors using high-voltage process is also being pursued [3], but it requires multiple-well structures and has large layout area penalty.

Natural solution was to use Silicon-On-Insulator (SOI) technology as shown in Fig. 1-(b). It was already discussed in 1990 to use the SOI technology for vertex detectors [4]. However, there are several issues to address in order to use the SOI technology for particle detector, and the SOI pixel detector is still not so popular.

The first issue is the so called "Back-Gate effect": the high voltage applied to the back-side of the sensor induce back-side channel of the transistors. Then it will cause the threshold voltage shift and drain current leakage of the transistor. The second issue is the coupling between the sensor and the readout electronics, that can cause signal oscillation, cross talk, and noise increase. The sensors and the transistors in the readout sections are in fact separated only by a thin buried oxide (BOX: $\sim 200\text{nm}$ thick).

The third issue concerns the Total Ionization Dose (TID). SOI devices are known to be robust with respect to single event effect (SEE) because the active Si thickness is very thin ($\sim 40\text{nm}$), and TID effect to the gate oxide is limited due to the thin gate oxide ($\sim 4\text{nm}$). However, it has relatively thick oxide (BOX) under the transistors. The oxide will accumulate trapped hole generated by the TID and the potential under the transistor increases. Then the threshold voltage shift and drain current leakage will start in the same way as the Back-Gate effect.

In addition, there was no good SOI wafer, which has high resistivity substrate, in early 90's. So it was difficult to fully deplete the sensor. Thick sensing region is especially important for X-ray applications. We had to wait for good bonded wafer with high-resistivity substrate around year 2000 [5]. With these issues, most of the SOI pixel development could not be successful.

We have started SOI Pixel detector development in 2005 [6] by using smartcutTM SOI wafers. We have been using high-resistivity substrate bonded to a standard thin Si layer (SOI

layer). In section 2, we describe the SOI pixel process which solved the above issues. In section 3, several examples of SOI detectors we have developed so far are presented.

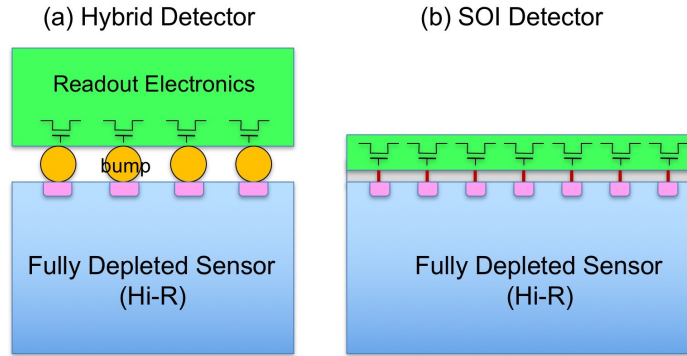


Fig. 1. Schematic drawing of (a) Hybrid pixel detector and (b) SOI pixel detector. The SOI detector looks natural successor of the hybrid detector.

2. SOI Pixel Process

We have developed SOI Pixel (SOIPIX) process based on Lapis Semiconductor Co. Ltd. 0.2 μ m fully-depleted SOI CMOS process [7]. The back-gate issue was avoided by fabricating buried wells under transistors [8]. The specifications of the SOIPIX process are summarized in Table 1, and the main features are listed below;

- There is no mechanical bump bonding and it is fabricated in semiconductor process only. Good yield and lower cost are expected and higher-density smaller pixel size is possible. In addition, the amount of material is reduced to a minimum.
- Thickness of the fully-depleted sensor region can be selected between 50 μ m~700 μ m. So it can be used for many applications.
- Parasitic capacitances of sensing nodes are very small (\sim 10fF), so large signal with low noise is obtained.
- Full CMOS circuitry can be implemented in the pixel.
- Cross section of single-event effects is very small. A latch-up mechanism, which destroys conventional bulk CMOS LSI, is absent.
- The detector can be operated in ultra-low temperature (<1 °K) as well as in a high temperature (\sim 200 °C) environment.

To reduce the submission cost and have a fast design turnaround, we have been operating Multi Project Wafer (MPW) run 1~2 times per year by collecting many designs from many institutes.

Table 1. Specification of the SOI Pixel process.

Top Si Process	0.2 μ m Low-Leakage Fully-Depleted SOI CMOS, 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/ μ m ²), DMOS, Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mm ϕ , 720 μ m thick Top Si : Cz, \sim 18 Ω -cm, p-type, \sim 40 nm thick, Buried Oxide: 200 nm thick Handle wafer: Cz (n) \sim 700 Ω -cm, FZ(n) $>$ 2k Ω -cm, FZ(p) \sim 25 k Ω -cm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Aluminum plating (200 nm thick)

2.1. Double SOI Wafer & Process

Most of the issues in realizing the SOIPIX are coming from the proximity of sensors and transistors. To solve these issues, we have developed Double SOI (DSOI) wafer and process technology. Typical structure of the DSOI pixel detector and photograph of the cross section are shown in Fig. 2 and Fig. 3 respectively.

The DSOI wafer is fabricated by repeating the layer transfer process twice. The top Si layer is used as a standard SOI layer and the middle Si layer is used as a shielding layer between sensors and transistors. In addition, the middle Si layer can work as a fixed potential layer, so that the potential caused by the trapped oxide hole can be compensated.

Thickness and resistivity of the DSOI wafer layers are summarized in Table 2. We have changed substrate type from n-type to p-type to increase charge collection efficiency. We also changed the middle Si layer type from p-type to n-type to lower the resistance by utilizing conduction layer created by lowering the layer potential.

By using the DSOI wafer, we confirmed that the cross talk from circuit to sensor becomes 1/20 of the single SOI case [9]. Furthermore, the gain of charge sensitive amplifier increases because the parasitic capacitance between sensor and amplifier is reduced. Threshold voltage shift of NMOS transistors by irradiation is compensated by changing the middle Si layer voltage (V_{SOI2}) as shown in Fig. 4.

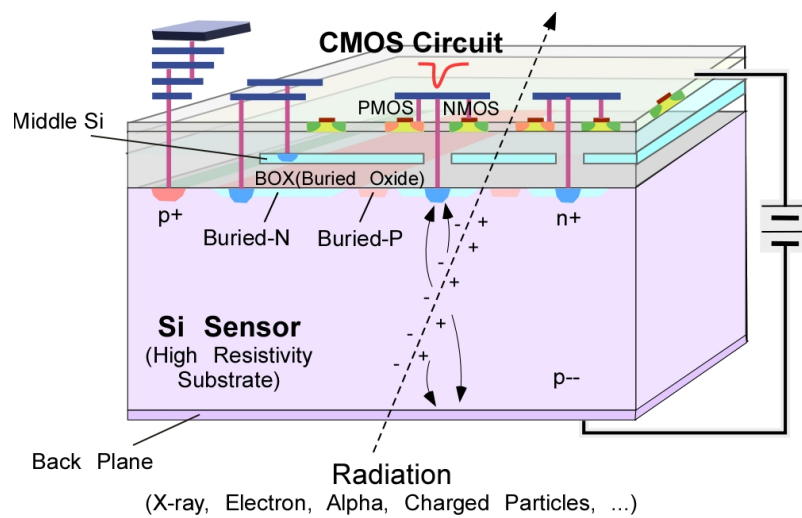


Fig. 2 Schematic structure of the DSOI pixel detector.

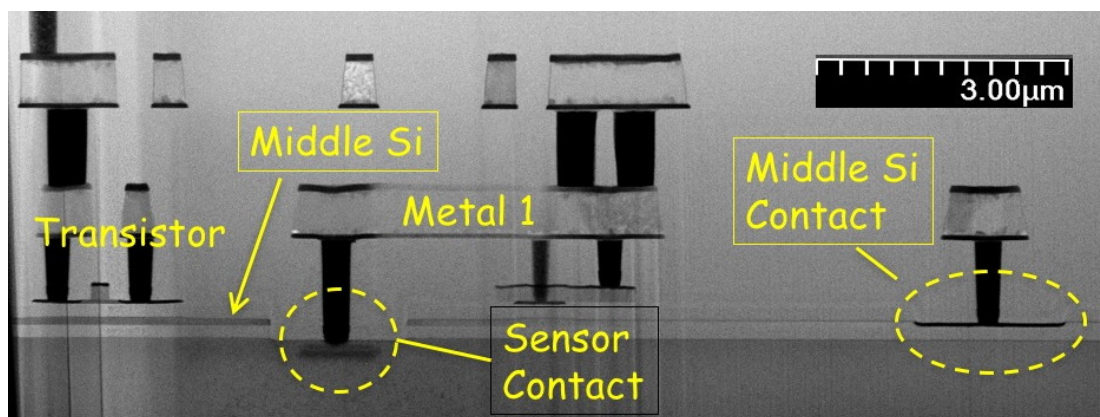


Fig. 3 TEM image of the DSOI pixel detector cross section.

Table 2. Specifications of the DSOI wafers.

Layer	1 st Lot	Present Lot	Next Lot
SOI1	p-type 88 nm, < 10 Ω •cm	p-type 88 nm, < 10 Ω •cm	p-type 88 nm, < 10 Ω •cm
BOX1	145 nm	145 nm	145 nm
SOI2	p-type 88 nm, < 10 Ω •cm	n-type 150 nm, < 10 Ω •cm	n-type 150 nm, 3-5 Ω •cm
BOX2	145 nm	145 nm	145 nm
Substrate	n-type Cz, 725um, > 700 Ω •cm	p-type Low Oxygen Cz, 725um, > 1.0 kΩ •cm	p-type FZ, 725um, > 5.0 kΩ •cm

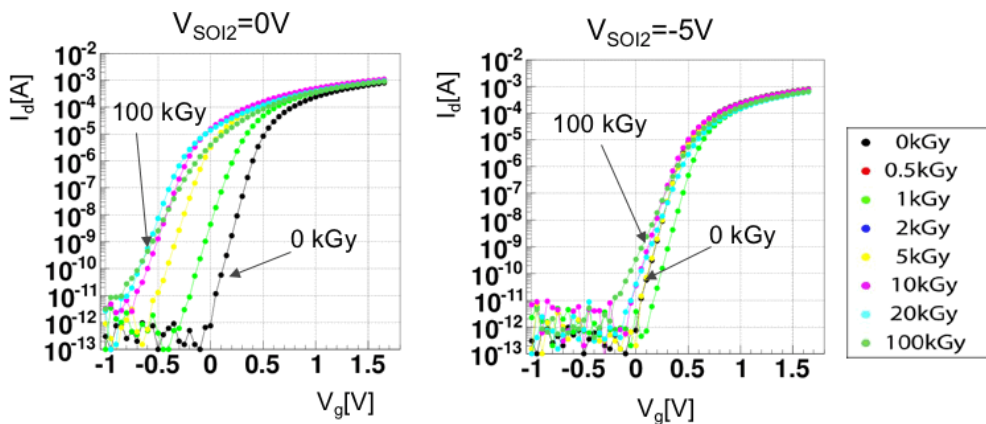


Fig. 4. Threshold voltage shift of a NMOS transistor by gamma-ray irradiation and the effect of middle Si layer voltage (V_{SOI2}).

2.2. Higher Dose LDD

In PMOS case, the magnitude of the threshold voltage shift is not so large compared to the NMOS case. The middle Si layer potential around -5V is also effective to compensate the shift. However, drain current is reduced by 80% at 112 kGy as shown in Fig. 5. By analyzing the PMOS transistor characteristics in detail, we found the effective gate length become longer and channel resistance is increased with the irradiation. We named this effect as Radiation Induced Gate Length Modulation (RIGLEM) [10].

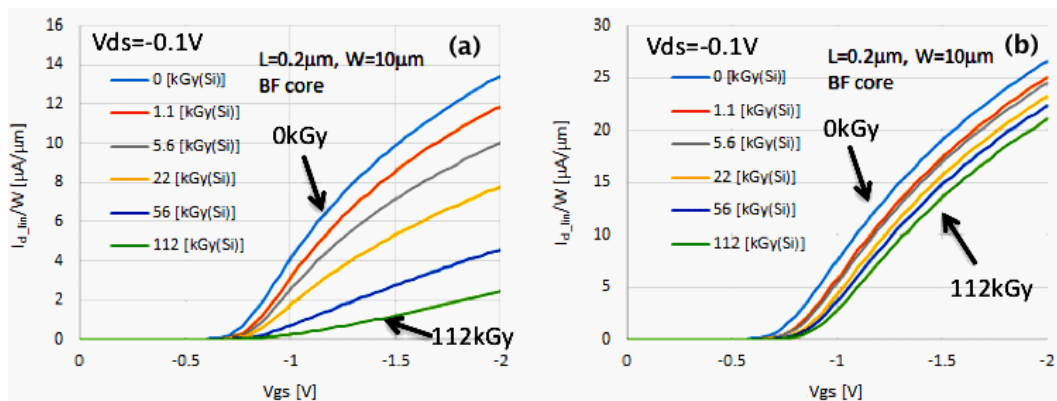


Fig. 5 Drain current reduction by gamma-ray irradiation. (a) previous process, (b) new process with 6 times higher LDD dose.

To fix this effect, we increased the dose level of the Lightly Doped Drain (LDD) region 6 times, then the drain current reduction is suppressed to 20% even at 112 kGy(Si). The original dose level of the LDD was determined to optimize the process for low-power operation. We have checked hot-electron effect and the 6 times increase is still safe for suppressing the effect, and the increase of the leakage current at off state is marginable.

2.3. Layout Shrinking with NMOS-PMOS merge

In bulk CMOS devices, PMOS and NMOS are isolated by creating reverse bias condition with N and P-wells respectively (Fig. 6-(a)). In contrast, in the SOI technology, active region of PMOS and NMOS transistors can be merged and contact to drain/source region can be shared as shown in Fig. 6-(b). The drain and source regions are connected through silicide process. This technique reduces layout size very much which is important to make complex functions in a small pixel area. In our experience, cell size of flip-flops and memories can be reduced more than 50% by using this technique.

We have designed a counting-type pixel by using this technique, and the designed pixel size becomes smaller than those pixels designed with finer feature size technology. This means we can get smaller pixel size while keeping appropriate analog voltage of 1.8V/3.3V which is difficult to get in finer process.

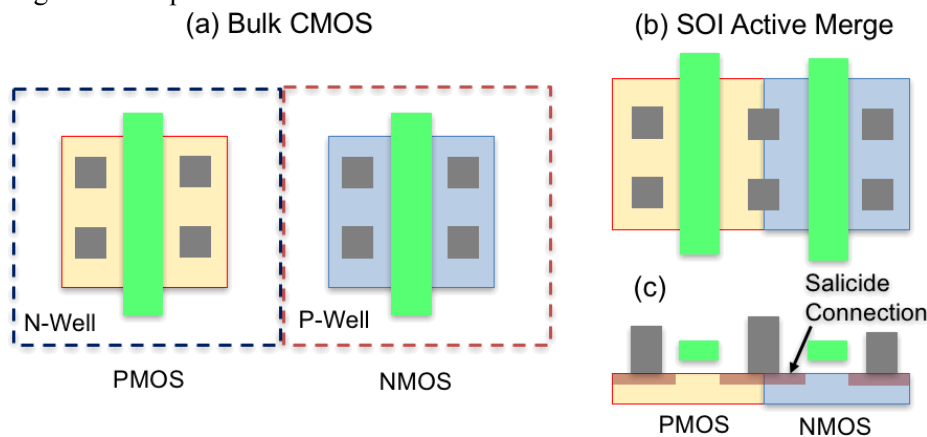


Fig. 6 (a) PMOS and NMOS separation with well structure in bulk CMOS process. (b) layout of merged PMOS-NMOS active layer in SOI technology.

3. Examples of SOI Detectors

There have been many kinds of radiation imaging detector developed by using the SOIPIX technology. A few examples of the detector are presented below.

3.1. Detector for XFEL and Synchrotron Radiation (SOPHIAS)

SOPHIAS is a large dynamic range X-ray imaging detector [11] developed by Riken group for X-ray Free-electron Laser Facility (XFEL), SACLA [12]. The target application is the coherent X-ray diffraction imaging experiments and it is also used in many synchrotron radiation experiments in SPring-8 [13] and KEK PF [14]. Fig. 7 shows photograph of two sensor camera system. The sensor fabricated from SOI wafer enables monolithic sensor with fully depleted p-n junction diode as thick as 500 μm . To fabricate larger sensor (64.77 x 26.73

mm²) than the mask size, stitching technique is developed and used. Each pixel has high- and low-gain channels to achieve large dynamic range. The different gain is achieved by different value of the input capacitor and different number of sensing nodes.

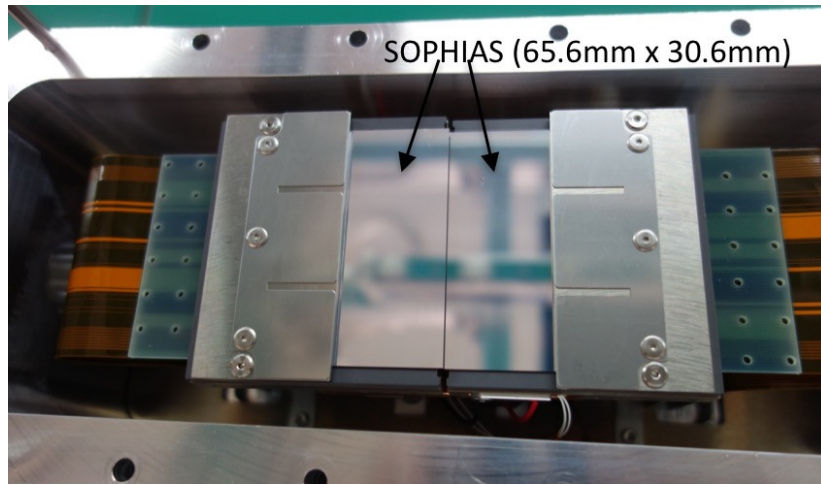


Fig. 7. Photograph of the SOPHIAS detectors mounted in the camera. Pixel size is 30 μ m square and there are about 2 Mega pixels (719 x 3 columns x 891 rows) (Courtesy of T. Kudo [15])

3.2. X-ray Detector for Astrophysics (XRPIX)

SOI detector for astronomical satellite X-ray observation (XRPIX) [16] has been developed to achieve a new X-ray detector system having a much faster readout and lower non-X-ray background (NXB) sensitivity than the X-ray CCDs. It is integration-type detector, and it also has trigger generation and hit position output functions (event-driven readout).

The XRPIX series offers good time resolution ($\sim 1 \mu$ s), fast readout time ($\sim 10 \mu$ s), and a wide energy range (0.5–40 keV) in addition to having imaging and spectroscopic capability. The XRPIX contains a comparator circuit in each pixel for hit trigger (timing) and two-dimensional hit-pattern (position) outputs. Therefore, signals are read out only from selected pixels. X-ray readout by this function is called “event-driven readout”.

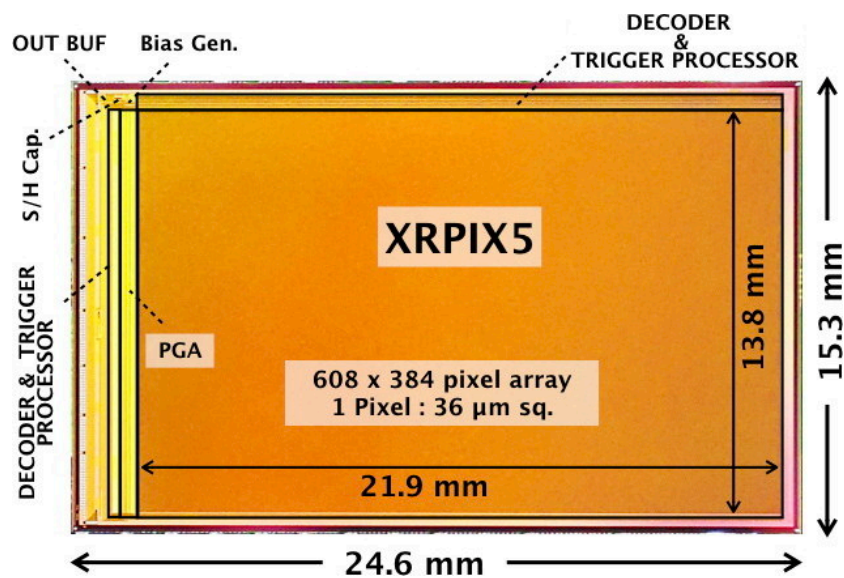


Fig. 8 Photograph of the XRPIX5 and function locations.

The X-ray spectral performance is improved by introducing in-pixel charge-sensitive amplifier circuit [17]. Energy resolution of 320 eV (FWHM) for 5.9 keV X-rays with which Mn-K α and -K β lines are resolved. The latest detector named XRPIX5 is 24.6 mm \times 15.3 mm in size and consists of 608 \times 384 pixels as shown in Fig. 8 [18]. The pixel size and the imaging area are 36 μ m \times 36 μ m and 21.9 mm \times 13.8 mm, respectively.

3.3. ILC Vertex Detector: SOFIST

Vertex detector for the International Linear Collider (ILC) [19] is being developed at KEK and collaborating universities. The detector is named as SOFIST (SOI sensor for Fine measurement of Space & Time) [20]. In the ILC experiments, fine tracking resolution better than 3 μ m and bunch timing identification are required. Our choice of the design is to use both analog signal memories and time stamping memories in a pixel, and implements all circuit within 20~25 μ m pixel area. To achieve this goal, we will use PMOS-NMOS active merge technique described in section 2.3, and we may also introduce vertical integration technology for additional layer of electronics.

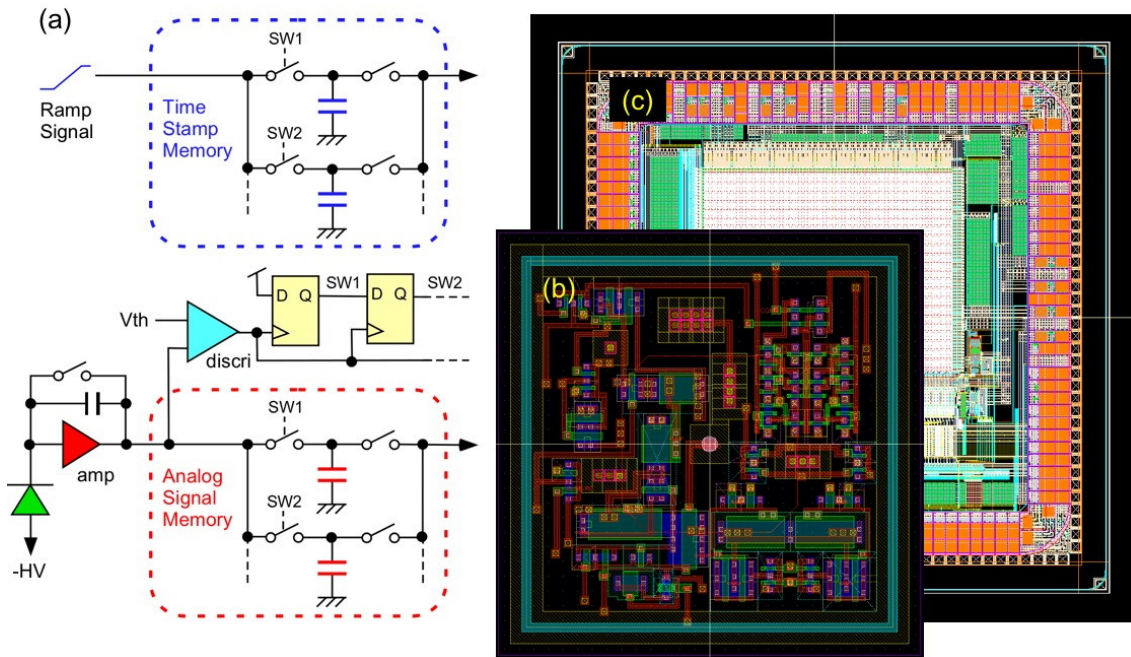


Fig. 9. (a) Architecture of the SOFIST pixel. (b) Layout of a pixel, (c) Layout of the test chip.

4. Summary

Monolithic radiation pixel detectors can be efficiently realized in an improved SOI process. Newly developed DSOI wafer and process solved issues of the back-gate effect, coupling between sensor and electronics, and improved radiation tolerance. With slight increase of the dose level of LDD region, the radiation hardness of the process reached more than 100 kGy(Si). PMOS and NMOS active merge technique reduced circuit layout size very much which is required in implementing complex functions in a small pixel. Many SOIPIX detectors are under development, and some are already used in actual physics experiments.

Acknowledgements

This work is supported by MEXT KAKENHI Grant Number 25109001 and 25109002. This work is also supported by LSI Design and Education Center (VDEC), the University of Tokyo with the collaboration with Cadence Corporation, Synopsys Corporation, and Mentor Graphics Corporation.

References

- [1] A. La Rosa, "ATLAS Pixel Detector: Operational Experience and Run-1 to Run-2 Transition", in proceedings of the 23rd International Workshop on Vertex Detectors, PoS(Vertex2014)001, doi:10.1016/j.phpro.2015.05.067.
- [2] J. Schambach, et al., "A MAPS Based Micro-Vertex Detector for the STAR Experiment", Physics Procedia 66 (2015) 514 – 519
- [3] I. Peric, "Overview of HVCMOS pixel sensors", JINST 10 (2015) C05021, doi:10.1088/1748-0221/10/05/C05021.
- [4] Jean-Pierre Colinge, "An overview of CMOS-SOI technology and its potential use in particle detection systems", NIM A305 (1991) 615-619.
- [5] SOITEC Co., Smart Cut™, <https://www.soitec.com/>.
- [6] Y. Arai, et al., "First Results of 0.15um CMOS SOI Pixel Detector", SNIC Symposium, 2006, SLAC-PUB-12079, <http://www.slac.stanford.edu/econf/C0604032/papers/0016.PDF>
- [7] T. Ichimori and N. Hirashita, "Fully-Depleted SOI CMOS FETs With the Fully-Silicided Source/Drain Structure", IEEE Trans. on Elec. Dev., Vol. 49, No. 12, 2002, pp. 2296-2300.
- [8] Y. Arai, "Progress on Silicon-on-Insulator Monolithic Pixel Process", Proceedings of Science, PoS(Vertex 2013)021, http://pos.sissa.it/archive/conferences/198/021/Vertex2013_021.pdf.
- [9] Yunpeng Lu, et al., "First results of a Double-SOI pixel chip for X-ray imaging", Nucl. Instr. and Meth. A, Vol. 831, 2016, pp. 44-48.
- [10] I. Kurachi, et al., "Analysis of Effective Gate Length Modulation by X-Ray Irradiation for Fully Depleted SOI p-MOSFETs", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 62, NO. 8, AUGUST 2015. Digital Object Identifier 10.1109/TED.2015.2443797.
- [11] T. Hatsui, et al., "A direct-detection X-ray CMOS image sensor with 500 μm thick high resistivity silicon", in Proc. of the International Image Sensor Workshop, Utah, USA, 2013, Art. Num. 3.05. <http://www.imagesensors.org/>
- [12] C. Saji, et al., "Evaluation of data-acquisition front ends for handling high-bandwidth data from X-ray 2D detectors: A feasibility study", Nucl. Instr. Meth. A, Vol. 731, pp. 229–233, Dec. 2013.
- [13] Riken SPring-8, <http://www.spring8.or.jp/en/>
- [14] KEK Photon Factory, <https://www2.kek.jp/imss/pf/eng/>
- [15] T. Kudo of JASRI, private communication.
- [16] T. G. Tsuru, et al., "Development and performance of Kyoto's X-ray astronomical SOI pixel (SOIPIX) sensor", in Proc. SPIE 9144, Space Telescopes and Instrumentation 2014: Ultraviolet to Gamma Ray, Montreal, Quebec, Canada, Aug. 2014, pp. 914412.
- [17] A. Takeda et al., "Improvement of spectroscopic performance using a charge-sensitive amplifier circuit for an X-ray astronomical SOI pixel detector", 2015 JINST 10 C06005, doi:10.1088/1748-0221/10/06/C06005.
- [18] A. Takeda, et al., "Design and Development of an Event-driven SOI Pixel Detector for X-ray Astronomy and Light Dark Matter Search", 8th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (PIXEL2016).
- [19] The International Linear Collider, <http://www.linearcollider.org>
- [20] S. Ono, et al., "A monolithic pixel sensor with fine space-time 0resolution based on silicon-on-insulator technology for the ILC vertex detector". Proceedings of Science, <http://pos.sissa.it/>, In this conference.