

# CMS Forward Pixel Upgrade Electronics and System Testing

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This note discusses results of electronics and system testing of the CMS forward pixel (FPIX) detector upgrade for Phase 1. The FPIX detector is comprised of four stand-alone half cylinders, each of which contains frontend readout electronic boards, power regulators, cables and fibers in addition to the pixel modules. All of the components undergo rigorous testing and quality assurance before assembly into the half cylinders. Afterwards, we perform full system tests on the completely assembled half cylinders, including calibrations at final operating temperatures, characterization of the realistic readout chain, and system grounding and noise studies. The results from all these tests are discussed.

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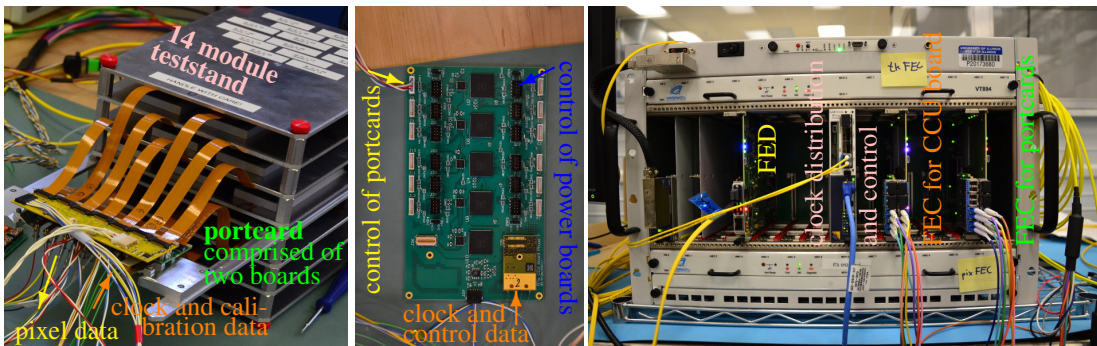
## 1. The CMS phase-1 pixel detector upgrade

The present CMS pixel detector will be replaced with an upgraded pixel system [1] in the LHC year-end shutdown 2016/2017. The upgrade of the pixel detector has been designed to cope with the higher luminosities expected in the coming years, and in particular after the next LHC shutdown. The new upgraded detector will have higher tracking efficiency and lower mass with four barrel layers and three forward/backward disks to provide a hit coverage up to  $|\eta| = 2.5$ . The forward part of the pixel detector (FPIX) contains 672 pixel modules mounted on twelve half disks, each disk made out of two rings. These disks are mounted on four mechanical half-cylinders, two on each side of the interaction point.

## 2. Establishing a full readout chain for the forward pixel detector

The principle of the readout chain of the upgrade is largely unchanged from that of the current detector. The system can be separated into two systems: A front-end part, comprised of pixel modules and readout and control electronics that are located on the half-cylinders inside the detector, as well as a back-end part outside the CMS detector whose front-end electronics control the detector via optical fiber connections. The on-detector readout electronics consist of three major parts: the pixel module itself, readout boards called portcards, as well as a control and communication unit (CCU board). The back-end infrastructure of the current pixel detector, based on the VME standard, will be replaced by a  $\mu$ TCA system. Both the portcards as well as the CCU board receive clock and control data via optical fibers from front-end controller (FEC) boards located in a  $\mu$ TCA crate, while the pixel data are sent to front-end driver (FED) boards located in the same crate. The conversion from electrical to optical signals is performed on small converter boards connected to the portcards.

While the FPIX modules are tested at a dedicated stand, both the portcards and CCU boards are tested within the full readout chain. For this, a group of 14 pixel modules are connected to a portcard at a time. The portcard itself is controlled by the CCU board using the I<sup>2</sup>C protocol. The calibration signals from the FEC board go to the modules through the portcard. The pixel data are sent via the portcard to a FED board. A portcard together with a 14 module stand, a CCU board, and a  $\mu$ TCA crate are shown in Fig. 1.



**Figure 1:** Left: a portcard with 14 connected pixel modules, middle: a CCU board, right: a  $\mu$ TCA crate containing FEC and FED boards.

As the  $\mu$ TCA system for the pixel detector upgrade is still under development, most qualification tests for the portcards have been performed with a front-end electronics readout system based on the VME standard.

### 3. Details on the electronics and full system testing

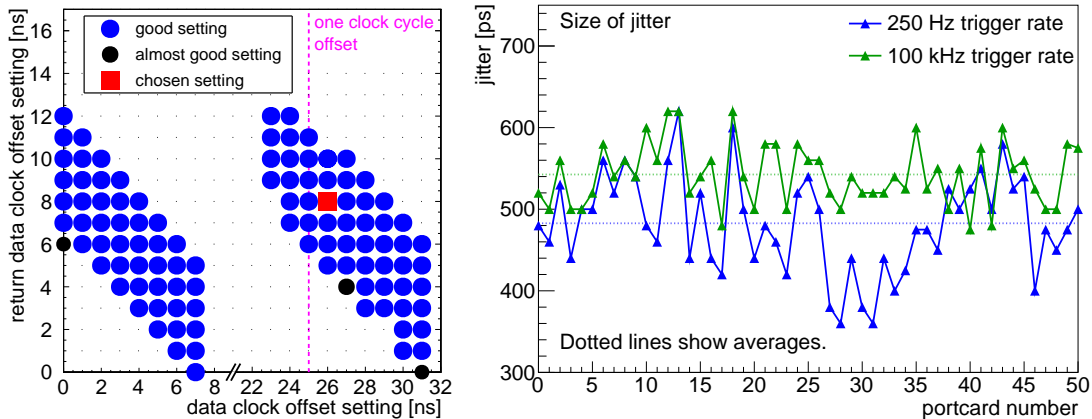
The first stage of testing is the quality assessment of each electronic element prior to its integration into the FPIX detector. Only elements without any faults are installed in the detector. For the portcards and the CCU boards, this assessment is performed in the full readout chain, as described in the previous section, which has been setup at the Fermi National Accelerator Laboratory.

The portcard has various ASIC chips organizing the readout: 14 low current differential signal (LCDS) chips, two detector control unit (DCU) chips for temperature and humidity information, a “delay25” chip aligning clock and data signals with the acknowledgment signals returned from the pixel modules, and a “gatekeeper”, regulating the signals going into the pixel modules, as well as translating the FEC signals into the token bit manager [3] LCDS standard used by the pixel modules. The token bit manager controls the readout of all readout chips of a pixel module. Furthermore, there are two phase-locked loop (PLL) crystals: the Tracker-PLL (TPLL), decoding trigger and clock information, and a quartz crystal oscillator (QPLL) acting as jitter filter.

Each function of those ASICs has to be tested. Some of them need dedicated tests, while others can be tested together, such as the gatekeeper and delay25 functioning. As examples, two tests will be described.

Clock signals and calibration data for the pixel modules are sent from the FEC to the portcard. From there, they are distributed to the connected pixel modules. First, the calibration data has to be aligned with the clock such that the pixel module is able to interpret the commands. Then, the commands are reflected back so that the user knows if the commands had been received by the pixel modules. However, the FEC will be only able to readout this return signal if it is properly aligned with the clock. The delay25 performs the alignment of all those signals. However, the offset between the signals must be small enough so that the delay25 can do the alignment. An additional user-defined delay can be added to each line to compensate for too large offsets. In order to find the proper delay settings, a two-dimensional scan between the calibration data and return data offset settings is performed. One of these scans is shown in Fig. 2, left: Settings for which the FEC sent and received back each signal are indicated in blue. The success of this test does not only indicate the proper functioning of the delay25 chip, but also that of the gatekeeper, as it controls which signals are passed to the pixel modules.

Another test is the jitter filter capability of the QPLL chip. It was observed in early studies [2] that for a readout chain without a QPLL chip, jitter from PLL disturbances of encoded trigger signals cannot be ignored at very high trigger rates. The QPLL chip is tuned to the LHC operation frequency and thus can filter out this jitter. This capability is tested by running the full system at a low trigger rate of order 250 Hz and at a high trigger rate of order 100 kHz, and comparing the jitter in the pixel readout data. The jitter measurements for the first fifty portcards are summarized in Fig. 2, right. As can be seen in the figure, the size of the jitter does not increase dramatically at the higher trigger rate for any of the tested boards.



**Figure 2:** Left: example of the two-dimensional scan of calibration data offset setting and that of its return signal in the delay25 chip, right: summary of the jitter measurements for the first fifty tested portcards.

These and other tests are used for determining the quality of the portcards. The majority of the portcards have been determined good and only those have been installed into the half-cylinders.

In addition to portcards, the CCU boards have also been tested. The CCUs control the settings of the portcards, the on-detector power boards, as well as some of the temperature readouts.

#### 4. Towards integration

Once a full set of electronics is qualified as good, it gets installed into the half-cylinder structure. A secondary quick test is performed prior to the installation of the half-disks containing the pixel modules. These quick tests check if all connections between the various elements are done properly, as well as if any element was damaged during the installation process - such as testing that the laser drivers connected to the small converter boards are still working by measuring their optical light yield.

After the installation of the half-disks containing the pixel modules, the half-cylinder is cooled down to its nominal operation temperature of  $-20^{\circ}\text{C}$  and a full suite of tests is repeated, such as the delay25 scan described above, as well as dedicated pixel module tests.

#### References

- [1] CMS Collaboration, *CMS Technical Design Report for the Pixel Detector Upgrade*, CERN-LHCC-2016, CMS-TDR-11.
- [2] S. Hasegawa, *Prototypes and system test stands for the Phase I upgrade of the CMS pixel detector*, Nucl. Instrum. Meth. A **831** (2016) 385.
- [3] E. Bartz, *The token bit manager chip for the CMS pixel readout*, Proceedings for PIXEL2002, Carmel, USA (2002), <http://www.slac.stanford.edu/econf/C020909/>.