

## Overview of the ATLAS Fast Tracker Project

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The next LHC runs, with a significant increase in instantaneous luminosity, will provide a big challenge for the trigger and data acquisition systems of all the experiments. Intensive use of the tracking information at the trigger level will be important to keep high efficiency for interesting events despite the increase in collisions per bunch crossing. In order to facilitate the use of tracks in the High Level Trigger, the ATLAS experiment planned the installation of a hardware processor dedicated to tracking: the Fast Tracker processor. The Fast Tracker is designed to perform full detector track reconstruction of every event accepted by the ATLAS first level hardware trigger. To achieve this goal the system uses a parallel architecture, with algorithms designed to exploit the computing power of custom Associative Memory chips, and modern field programmable gate arrays. The processor will provide computing power to reconstruct tracks with transverse momentum greater than 1 GeV in the entire tracking volume. The tracks will be available at the begin of the trigger selections, allowing to develop new more pileup resilient triggering strategies as well as allow for entirely new ones. The Fast Tracker system will be massive, with about 8000 Associative Memory chips and 2000 field programmable gate arrays, providing full tracking with a rate up to 100 KHz and an average latency below 100 microseconds. The system began commissioning in 2016, with a full barrel coverage reached by the end of the year. In these proceedings the final version of the electronic boards is presented, as well as reports on the commissioning status and as well as the first data-taking experience.

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## 1. Introduction

The Fast Tracker (FTK) [1] is a new ATLAS [2] trigger component, currently under installation, that will provide full tracking for the High Level Trigger (HLT) for every event selected by the first level hardware based trigger. FTK will be capable to provide the full event tracking for tracks with a transverse momentum,  $p_T$ , above 1 GeV. The ATLAS Trigger system as described in Ref. [3] and split into two levels: a hardware level (L1) and a HLT based on commodity servers. The hardware level trigger is based on custom electronics and the reconstruction of variables is performed at the LHC collision frequency (i.e. up to 40MHz). The average output of the L1 trigger to HLT is about 100 kHz. The HLT uses software algorithms to compute characteristics of the events and decides which events to retain for offline processing.

For every L1 accept a copy of all Inner Detector (ID) <sup>1</sup> [4] output is sent to FTK via dedicated optical fibres. This functionality is implemented in a Dual HOLA mezzanine [1] for the SCT system and the older part of the readout of the Pixel Detectors. For the Insertable B-Layer (IBL) [5] and Layer 2 of the Pixel detector this functionality is implemented in an upgraded readout system. This connections allows for the FTK to "spy" on the output of the Pixel and SCT detectors. This functionality is essential for the commissioning of the system.

## 2. The FTK system

The FTK system has several functional layers that are implemented in custom made electronics boards. Following the data flow the FTK components are: the input mezzanine (IM), the data formatter (DF), the auxiliary board (AUX), the associative memory board (AMB) and its mezzanines called little associative memory boards (LAMBs), the second stage board (SSB) and the FTK to HLT interface board (FLIC). These components are performing, in order, clustering and data reduction of the inner detector incoming data, assignment of the hits to 64 geographical towers in  $\eta$  and  $\phi$ , pattern matching against coarse resolution hits, refined track fitting including the first eight layers of the inner detector and , a second step fitting including all 12 layers of the ID and packing of the tracks into the required format and sending them to the HLT, respectively.

**Input Mezzanine:** The input mezzanine is the interface with the ID readout. It is designed to receive the raw hits from the ID, cluster them, compute the centroid and send this information downstream to the next board. Performing clustering at this stage is important both for data reduction in the FTK system and for achieving a better resolution of the hits considered in the subsequent steps. Due to the differences in the complexity between older generation pixel readout and the newer generation (installed for IBL for example) there are two types of IMs having similar functionality but different processing powers. The less powerful, in terms of processing power, is equipped with two Spartan6 FPGAs while the more powerful one is equipped with two Artix7 FPGAs. Each of the IMs gets four inputs from optical links, two coming from SCT and two from Pixels split equally between the two FPGAs on the IM.

**Data Formatter:** The Data Formatter system is based on ATCA technology. Functionally it is responsible for assigning all hits coming from ID into logical  $\eta \times \phi$  towers. The towers are arranged in a configuration including overlaps of neighbouring towers in order to improve tracking

<sup>1</sup>Throughout this proceeding by the ATLAS ID is the pixel and strip silicon detectors with a covering  $|\eta| < 2.5$ .

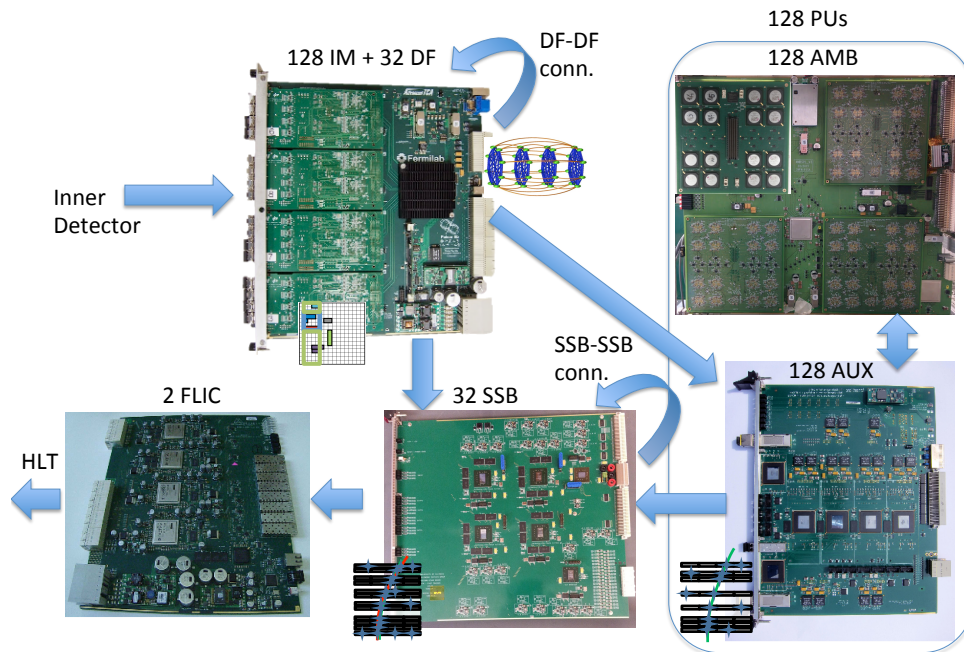


Figure 1: Photographs of FTK boards (labels indicate the number of boards) showing schematically the data flow path between them. The arrows indicate the direction of the data flow between subsystems (straight arrows) and within the components (curved arrows) in the FTK system [1].

efficiency. The DF system consists of a total of 32 boards arranged in four ATCA shelves. The communication between the DFs is performed via the Fabric of the backplane but also via high speed links connecting the DFs in different shelves via rear transition modules. In August 2016 one of the four shelves were fully commissioned in the electronics cavern of ATLAS and by the end of the year all remaining boards will be commissioned. Via the RTMs the DF will send the hits in eight (four Pixel and four SCT) of the 12 ID layers considered to the Processing Units<sup>2</sup> (PUs) and the remaining four layers to the corresponding SSBs.

**Auxiliary Board:** The Auxiliary Board functions as a database and track fitting engine. It maps the incoming ID hits into coarser resolution predefined units (Super Strips) that are used in the AMB for the pattern matching step and roads are returned. The hits corresponding to the returned road are retrieved, using the Super Strip assignment, and fits using linear approximations are used to find the best matching track in a road. Only tracks with a  $\chi^2$  below a predefined value are retained, similar tracks are removed using a procedure to remove duplicates. The surviving tracks are sent further to the SSB.

**Associative Memory Chip 06:** The core of the processing-unit is the associative memory chip (AM06). The chip has eight buses on which the SS identifiers (SSIDs) arrive as they are

<sup>2</sup>A processing unit (PU) consists of one AUX and one AMB located in the same VME slot.

generated in the AUX. The SS are matched against 128,000 pre-stored patterns stored in each chip. A pattern consists of 8 SSIDs and a pattern is considered matched if seven out of the eight SSIDs are matched. This process is improved by the technical feature that up to three of the SSIDs can be defined using ternary bits (using CAM technology) and this allows for extended SSIDs matchings (also it means that less patterns can be used to obtain the same coverage). Physically, 16 AM chips are placed on the LAMBs and each of the AMB boards has four mezzanine LAMBs.

**Second Stage Board:** The roads returned by the AUX use only eight of the 12 layers of the ID for the candidate tracks. The SSB extrapolates the returned track to the four layers, not considered in the first stage track fitting, and performs a second stage fitting. A single SSB performs this function for four AUX boards. Inter SSB connections allow for an effective removal of similar tracks in large geographical regions and reduce the number of outputs to the FLIC on a total of 16 optical links.

**FLIC:** The 12-layer-track data stream from SSB is put into the ROD format of the ATLAS detector by the FLIC and sent to the FTK ROS. After this step the FTK tracks can be used in the HLT.

For a more in depth information on the PUs, Data Formatter, Input Mezzanines and FLIC please consult [7, 8].

**Infrastructure:** The FTK system is installed in seven racks in the ATLAS electronics cavern. Four of these racks are dedicated to the processing units, two are dedicated to the Data Formatter system and one is used for the FLIC and for control computers. Due to the high power consumption of the AM06 chip the processing-unit racks are mostly equipped with customised equipment. Each rack comprises two VME bins, two custom fan units for each bin and one custom power supply that powers both bins and the custom fans. Extended studies were performed, both in simulation and in situ, to understand the airflow and temperature distributions in the rack. The FLIC and DataFormatter systems are built on ATCA technology and mostly use off the shelf equipment. The ATCA shelves for the Data Formatter were modified to allow for vertical cooling and are powered by external power supplies.

### 3. Expected performance of the FTK system, installation status and schedule

FTK will deliver tracks to HLT of a very similar quality as achieved in the offline reconstruction at a much faster processing time. The latency of the FTK system is expected to be within 100 microseconds, leaving ample time for the tracks to be used as input to HLT algorithms. The tracking efficiency with respect to offline tracks as a function of the  $p_T$  can be seen in Fig. 2a. Another example of the expected FTK quality of the tracks can be seen in Fig. 2b where using the re-fitted FTK tracks at HLT the transverse impact parameter  $d_0$  significance is compared with respect to the offline values. As it can be seen the distributions are very similar between offline and using FTK tracks.

At the moment of this conference the focus is on commissioning the FTK system for the central barrel region ( $|\eta| < 1$ ) which corresponds to the installation of 16 PUs in two VME crates. Half of the DF system has been installed. The commissioning concentrates on debugging firmware and gaining operational expertise in the interaction with the ID. The AUX and AMB communication is properly established and work is ongoing for check of functionality using test-vectors obtained

from the FTK Simulation. The SSB is in the process of establishing communication with the AUX, DF and FLIC boards.

The foreseen installation of the FTK system is staggered and follows the expected increase in LHC instantaneous luminosity from today to Run3. For 2017 a system comprised of 64 PUs, hence half of the foreseen system, will be installed. It aims at coping with LHC instantaneous luminosities corresponding to an average pile-up of 50 for full detector coverage. The full installation of the FTK will comprise 128 PUs and will handle LHC instantaneous luminosities up to an pile-up of 80 interactions per bunch crossing.

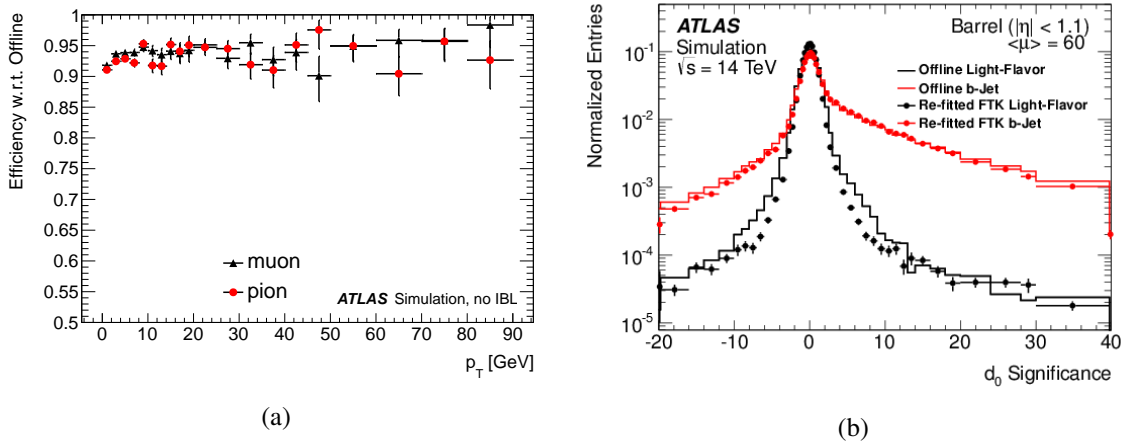


Figure 2: a) FTK efficiency with respect to offline in muon and pion samples as a function of offline  $p_T$  [1]. b) The transverse impact parameter significance for barrel tracks associated to light-flavor (black) and heavy-flavor (red) jets. The transverse impact parameter significance is defined as the transverse impact parameter divided by its associated uncertainty[6].

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