

Upgrade of the ATLAS Calorimeters for Higher LHC Luminosities

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The upgrade of the LHC will bring instantaneous and total luminosities which are a factor 5–7 beyond the original design of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ for the ATLAS Liquid Argon (LAr) and Tile Calorimeters and their readout systems. Due to radiation requirements and a new hardware trigger concept, the readout electronics will be improved in two phases. In Phase-I, dedicated electronics of the LAr Calorimeters trigger readout will provide finer granularity input to the trigger, in order to mitigate pile-up effects and to reduce the background rates. In Phase-II, completely new readout electronics will allow a digital processing of all LAr and Tile Calorimeter channels at the full 40 MHz bunch-crossing frequency and a transfer of calibrated energy inputs to the trigger. Results from system design and performance of the developed readout components, including fully functioning demonstrator systems already operated on the detector, will be reported. A high-granularity replacement of the current Forward Calorimeter (FCal) is proposed, improving on reconstruction of jets and missing energy in the presence of pile-up. The corresponding R&D and expected performance results will be presented. Another upgrade project that is under consideration is a high-granularity timing-device in front of the end-cap/forward calorimeters to help particle identification and pile-up mitigation. The R&D work on this project will be also presented.

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1. Introduction

The ATLAS detector [1] is a general purpose detector at the CERN Large Hadron Collider (LHC), designed to measure proton-proton collisions with a center of mass energy $\sqrt{s} = 14$ TeV at an instantaneous luminosity of 10^{34} cm⁻²s⁻¹. The Liquid Argon (LAr) Calorimeters are sampling calorimeters consisting of 182,468 channels using Liquid Argon as an active medium and combinations of lead, tungsten and copper as passive absorbers. The Tile Calorimeters consist of 256 iron-scintillator wedges that measure the remaining 30% of the hadronic energy after the LAr Calorimeters.

The ATLAS Calorimeters, shown in Figure 1, were designed to survive a total radiation dose corresponding to an integrated luminosity of 1000 fb⁻¹. The LAr readout electronics are designed to provide digitized calorimeter input to the Level-1 (L1) trigger processor at a maximum acceptance rate of 100 kHz. The proposed High Luminosity LHC (HL-LHC) will submit the detectors to instantaneous luminosities 5–7 times the nominal luminosity and record a total integrated luminosity of up to 3000 fb⁻¹. The average simultaneous interactions per bunch crossing, $\langle \mu \rangle$, will climb from its current value $\langle \mu \rangle = 20$ up to a maximum of $\langle \mu \rangle = 140 - 200$. To deal with the aging readout components and an increased instantaneous luminosity, the LAr readout will be upgraded in two phases: a finer granularity trigger upgrade in Phase-I and completely new readout electronics in Phase-II. For similar motivations, the Tile Calorimeter will also implement completely new readout electronics in Phase-II. Additionally, a high granularity sFCal replacement of the Forward Calorimeters (FCal) is proposed for Phase-II to address ion buildup degradation and the high pile-up (PU) environment. Finally, a High Granularity Timing Detector (HGTD) in the forward region is proposed as part of the Phase-II upgrade to provide sub 50 ps single particle timing resolution to mitigate pile-up.

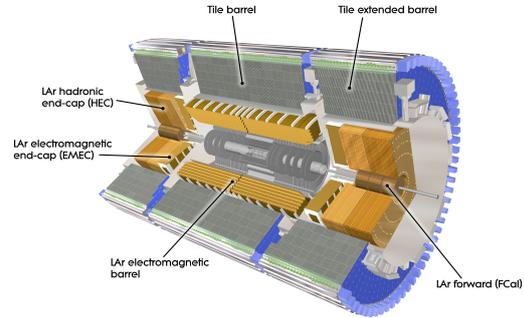


Figure 1: The Liquid Argon Calorimeters cover ranges in pseudo-rapidity, η , of: $|\eta| < 1.475$ (EMB), $1.375 < |\eta| < 3.2$ (EMEC), $1.5 < |\eta| < 3.2$ (HEC) and $3.1 < |\eta| < 4.9$ (FCal). The Tile Calorimeters cover $|\eta| < 1.7$ [1].

2. Phase-I Upgrade

The Phase-I Upgrade to the LAr trigger readout [2] will take place during the so-called Long Shutdown 2 between 2019–2020. During Run 3, the L1 trigger must maintain the current 100 kHz acceptance rate with a latency below 3 μ s. As the instantaneous luminosity increases during Run 3, conditions reaching $\langle \mu \rangle = 60$ will require finer granularity input to maintain low p_T trigger thresholds.

The current Trigger Tower (TT) and new Super Cell (SC) trigger sums are shown in Figure 2. Increasing the granularity by a factor of 10, the new SCs will provide longitudinal shower development information to L1. Jet backgrounds in electromagnetic (EM) triggers can be reduced by

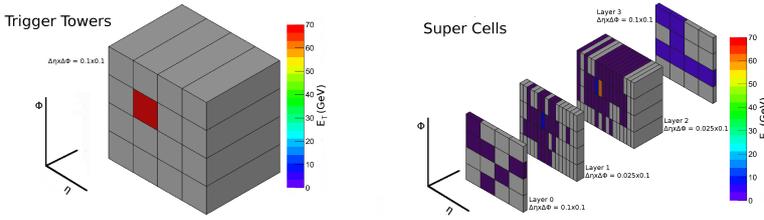


Figure 2: Simulated 70 GeV electron in current trigger tower $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ layout (left) and super cell layout (right) including 4 depth layers, and a finer granularity of $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$ in the front and middle layers [2].

utilizing the shower shape and isolation information provided by the SCs. Using PU subtraction methods, improved jet and E_T^{miss} resolution will reduce rates while maintaining high physics

acceptance. New electronics will need to be developed and installed to supply the finer granularity SC sums to the L1 processors.

An annotated block diagram of the new electronics is shown in Figure 3. On the front end (FE), new Layer Sum Boards (LSB) will be installed on the current Front End Boards (FEB) to create the analogue SC sums from detector pulses. A new baseplane will be installed to route the 34,000 SC signals to new LAr Trigger Digitizer Boards (LTDB) which will reside in spare slots of the current FE Crates. The 124 LTDBs will digitize up to 320 SCs per board at 40 MHz using a radiation hard, 12-bit, 4-stage successive approximation register (SAR) based pipeline ADC. Additionally, legacy analogue TT sums will be sent from the LTDB to the current Tower Builder Boards for backwards compatibility. The digitized SC signals will be multiplexed in 8 channel bitstreams and then serialized in the LOCx2 ASIC.

The bitstream will be amplified and converted to an optical signal with a VCSEL driver ASIC, then sent through 40 optical fibres per LTDB at 5.12 Gbps per fibre to the new back end (BE) LAr Digital Processing System (LDPS) for a total data transfer rate of approximately 25 Tbps from the FE to BE. A 320 channel LTDB prototype with all final base-line components will be produced soon.

On the BE, the LDPS will convert the digitized SC samples into calibrated transverse energies and send them at a total rate of 41 Tbps to new L1 Feature Extractors (FEX). 124 high bandwidth FPGAs with a 5.12 Gbps receiver and 10 Gbps transmitter, on 31 ATCA carrier boards, will each process up to 320 SCs within the proposed latency budget. The LDPS will be housed in three ATCA shelves with 10 GbE switches.

In 2014, a demonstrator with LSB, baseplane and LTDB prototypes was installed on the de-

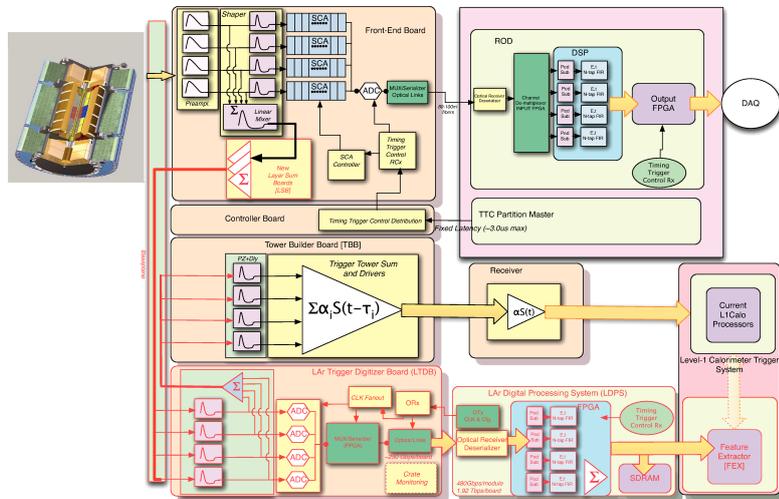


Figure 3: Block diagram of the LAr electronics. New Phase-I trigger upgrade components are shown in red [2].

tor to gain experience and validate expected physics performance improvements. A prototype LDPS with three Stratix IV FPGAs housed in a commercial 10 GbE ATCA crate is used to process the new SC readout. Since October of 2015, there has been parallel demonstrator and ATLAS readout. Analysis of the demonstrator data is currently underway.

3. Phase-II Upgrades

During the HL-LHC, aging detector components will require replacement to endure 3 times the design radiation dosage. A new hardware-based trigger architecture will require L0 and L1 acceptance rates of 1 MHz and 400 kHz and longer latencies of 10 μs and 60 μs respectively [3].

3.1 New Liquid Argon Calorimeter Readout

The Phase-II upgrade of the LAr readout is shown schematically in Figure 4. Taking place during the Long Shutdown 3 starting in 2024, the upgrade will involve the installation of completely new FEBs, called FEB2s, as well as new BE LAr Pre-Processor units (LPPR). The Phase-I trigger upgrade will remain intact and feed the new L0 trigger.

The 1524 new FEB2s will amplify, shape and digitize detector signals with full detector granularity. A radiation hard ADC, with 16-bit dynamic range operating at 40–80 MHz, will send digitized data from all LAr cells off detector through optical links, thus eliminating the need for FEB buffers. VCSEL Array Drivers will convert the digital samples to optical signals and transmit the data through 16 fibres per FEB2 to the LPPR at 9 Gbps per fibre for a total transfer rate of 200–400 Tbps.

The 60–120 new LPPRs will each house four high bandwidth FPGAs, each with 120 input links. The FPGAs will apply digital signal filtering and energy reconstruction to improve PU suppression. Each FPGA will process nearly 1 Tbps with an output rate of approximately 75 Gbps. Buffers will allow full granularity input to the L1 trigger while storing the data during the trigger latency.

Development of radiation hard ADCs, serializers, optical links and high bandwidth FPGAs will benefit from research and development of similar components for the Phase-I trigger upgrade.

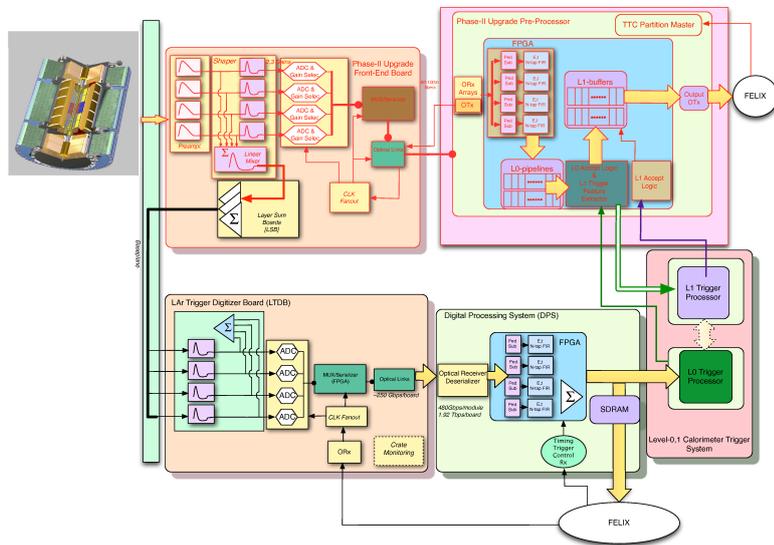


Figure 4: New electronics for the new Phase-II readout are shown in red. The Phase-I trigger upgrade will be reused to feed the L0 trigger [3].

3.2 New Tile Calorimeter Readout

As with LAr, Tile will completely replace the readout components to meet the radiation requirements, comply with the new triggering scheme, and digitize all data at 40 MHz to send off detector.

To optimize dynamic range, electronic noise, radiation tolerance, and pile-up handling, three replacement technologies are under development: a redesigned 3-in-1 amplifier and shaper using newer COTS components, a charge integrator and encoder (QIE) ASIC combined with a 4 gain ADC, and a Front-end for ATLAS TilecAL Integrated Circuit (FATALIC) ASIC with a 3 gain ADC using a current conveyor architecture. The latter two combined amplifier, shaper and digitizer ASICs might benefit from improved radiation hardness and lower noise levels.

New Mother Boards (MB) will perform 12 bit digitization in the case of the 3-in-1 prototype, and route the digitized data from the PMTs to FPGAs on the new Daughter Boards (DB) where they will be sent to the Tile Pre-Processor (TilePPR) on the BE through 4096 optical links at 9.6 Gbps per link for a total rate of 40 Tbps. There, digital trigger sums will be sent to L0 at 40 MHz while pipelines store data for L1 input consistent with the triggering and latency requirements.

Additionally, aging power supplies will need to be replaced. High voltage (HV) prototypes both external and internal to the mini-drawers are being developed. Low voltage (LV) power supply replacement design is completed and pre-production is underway.

A diverse demonstrator testing program in six mini-drawers has been developed involving prototypes of the three FEB alternatives (3-in-1, QIE, FATALIC), new MB and DB designs, both internal and external HV alternatives, and the new TilePPR. The test beam setup providing feedback on the efficacy of the prototypes will be expanded to eight mini-drawers in September.

3.3 Possible High Granularity sFCal

During the HL-LHC, the increased luminosity will particularly affect the forward detectors at larger $|\eta|$, where the particle flux is highest. The current

FCal, shown in Figure 6, has narrow LAr Gaps ranging from 269–500 μm to combat ion-buildup which can distort the electric field in conditions near the nominal luminosity. The gap sizes, however, are insufficient to prevent ion-buildup at HL-LHC luminosities. Additionally, the increased

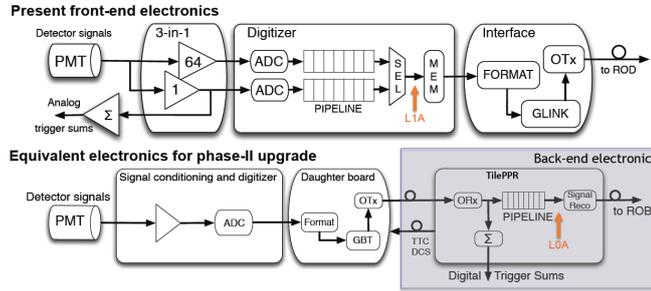


Figure 5: Phase-II Tile readout will digitize with full granularity at 40 MHz, eliminating the need for an analogue trigger [3].

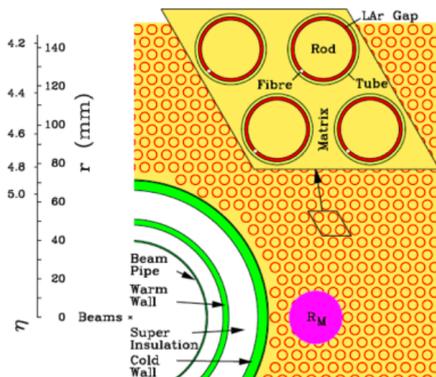


Figure 6: Diagram of FCal module showing LAr gap structure [1].

instantaneous luminosity will draw larger currents across the protective HV resistors, resulting in a HV “sag”, further deteriorating the signal response.

A proposed higher granularity “sFCal” upgrade would implement finer granularity in the first module (sFCal1), narrower LAr gap sizes (100–300 μm), and lower protective HV resistors. The finer granularity of the first module reduces noise from PU and provides improved jet substructure resolution. The smaller gap sizes and lower HV resistors prevent signal distortion from ion-buildup and HV “sagging” at HL-LHC luminosities. The risks to the entire end cap associated with this upgrade, including removing the FCal and cutting cryostat welds, are being factored into the forthcoming decision whether to replace the FCal.

3.4 Possible High Granularity Timing Detector (HGTD)

A high granularity, single particle, sub 50 ps time resolution detector is proposed to sit between the barrel and end cap cryostats with $2.5 < |\eta| < 4.3$ and $\Delta z = 70$ mm. Using silicon based low gain avalanche detectors (LGAD), HGTD will have four Si layers with sensors ranging from 1–9 mm^2 , and three possible tungsten (W) absorbers reaching $|\eta| = 3.2$. HGTD will provide detailed jet substructure timing information for PU mitigation, and improved electromagnetic energy reconstruction in the coarser EMEC inner-wheel from the three W “pre-shower” layers. The specific technology choices, and the decision whether to build, will be made in approximately 1.5 years.

4. Summary

The harsh radiation and PU conditions of the HL-LHC will require a hardware based triggering system and a two phase upgrade to the ATLAS calorimeters’ readouts. Production will start soon for the Phase-I LAr trigger upgrade that will feed L1 with finer granularity, digitized SCs, fully compatible with Phase-II. The LAr and Tile Phase-II readouts will provide full calorimeter digitization at 40 MHz and supply calibrated energies to the trigger inputs. There exists a diverse demonstrator testing program for the Tile upgrade, and LAr design is progressing promisingly. A decision whether to build a finer granularity sFCal to prevent signal deterioration and mitigate PU is forthcoming. Finally, a decision whether to build the HGTD to mitigate PU and improve electromagnetic energy reconstruction will come in approximately 1.5 years.

References

- [1] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, *JINST* **3** S08003.
- [2] ATLAS Collaboration, *ATLAS Liquid Argon Calorimeter Phase-I Upgrade Technical Design Report*, CERN-LHCC-2013-017.
- [3] ATLAS Collaboration, *ATLAS Phase-II Upgrade Scoping Document*, CERN-LHCC-2015-022.