

# Overview of the Compact Muon Solenoid Phase 1 Forward Pixel Upgrade

Irving D. Sandoval on behalf of the CMS collaboration

This is an NSF funded project.

## ABSTRACT

During Run 2 of the Large Hadron Collider a significant luminosity increase is foreseen. At the inner most part of the Compact Muon Solenoid, the silicon pixel detector has to cope with very large particle fluxes and radiation damage. To maintain a high tracking efficiency, the current pixel tracker will be upgraded by incorporating new digital readout chips, front-end electronics for higher data rates and using less passive material.

## CMS Tracker

The CMS tracker active material is silicon: the pixels, at the very core of the detector, and the silicon microstrip detectors that surround it (see Fig.1). This part of the detector is the world's largest silicon detector.

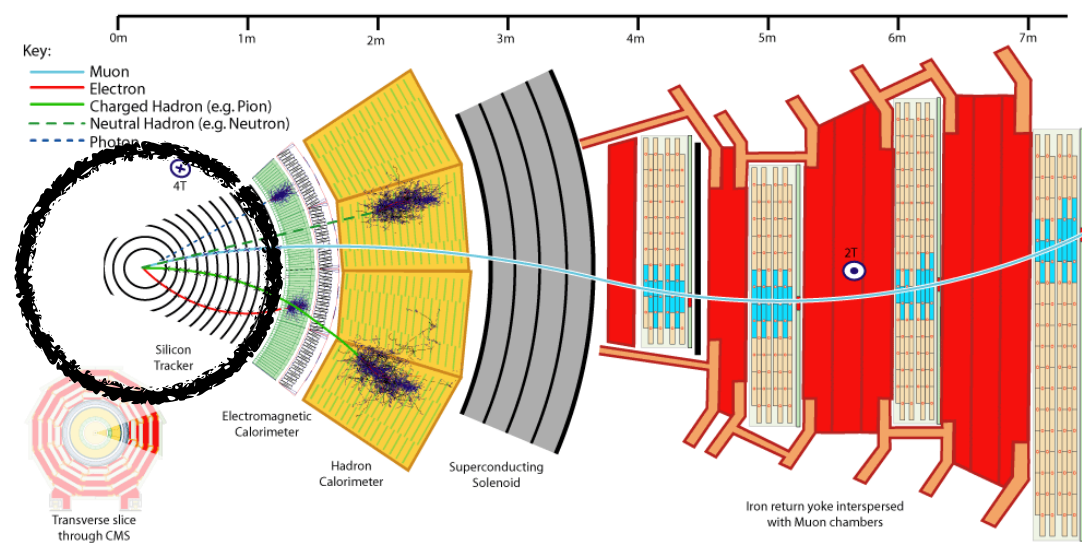


Fig.1 Highlights the silicon tracker of CMS.

## Phase 1 Pixel Upgrade

The current pixel detector was designed for a peak luminosity of  $1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ . Beyond this the pixel readout chip (ROC) suffers from significant dynamic data loss. With more interactions per crossing the tracking efficiency lowers and fake rates increase, Fig. 2.

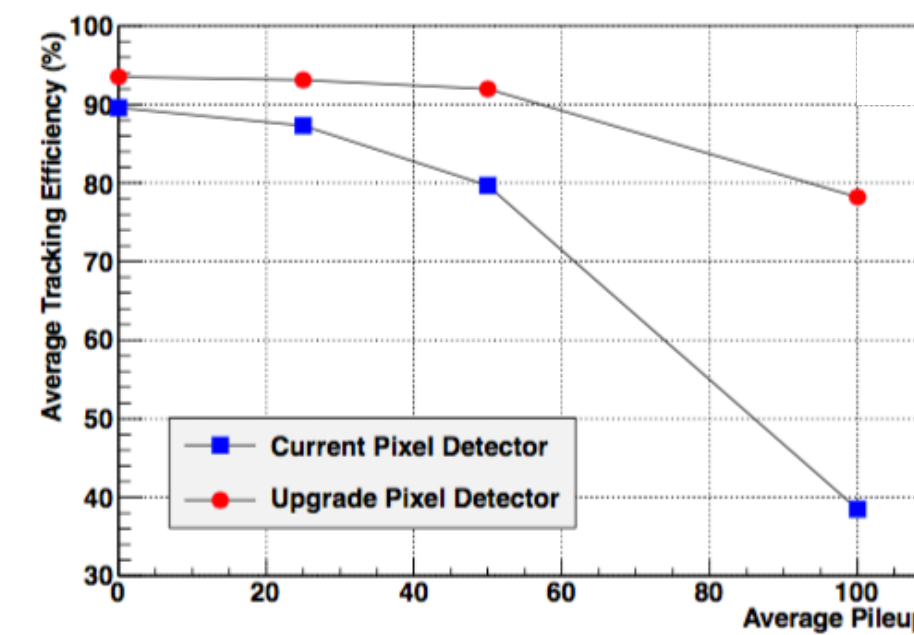


Fig.2 Tracking efficiency comparison.

The Ph.1 Pixel Upgrade will consist of four layers in the barrel (BPIX), adding one more layer compared to the current, also the endcap region of the detector (FPIX) will also have an additional third disk. This is reflected in the number of channels almost doubling from 66 M to 124 M, Fig. 3.

An ultra-light carbon fiber support structure, a two-phase CO<sub>2</sub> cooling system and by shifting the electronic service outside the active volume will allow the material budget to be reduced significantly.

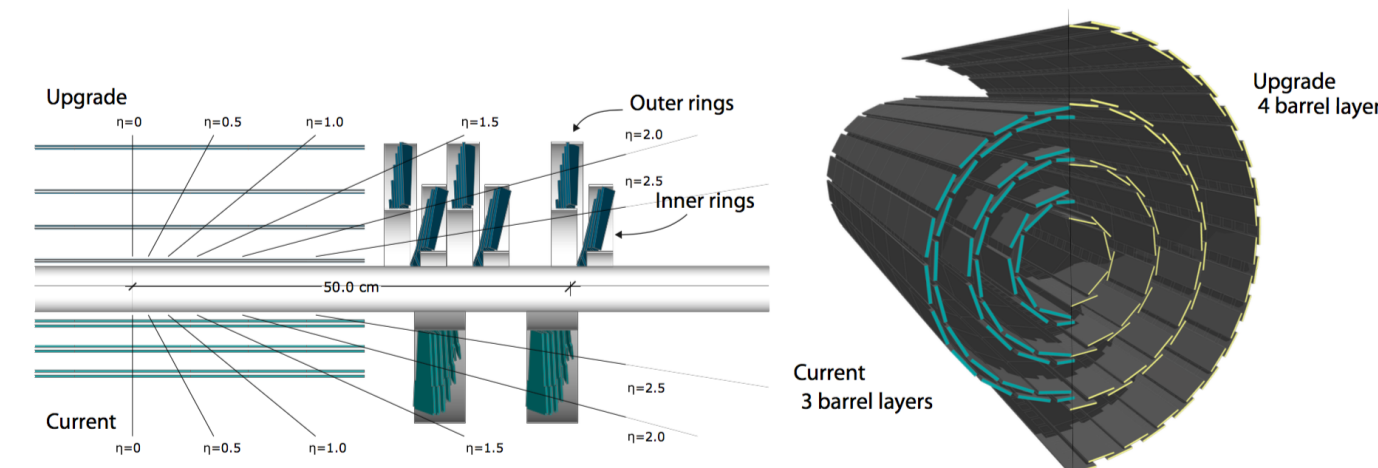


Fig.3 Comparison of the Phase 1 detector (top) versus the current detector layout (bottom)

## FPIX Modules

**FPIX** is a modular component that consists of 4 half-cylinders each with three half disks. Each half disk has an inner and outer part that contains 22 and 34 modules, Fig 4.

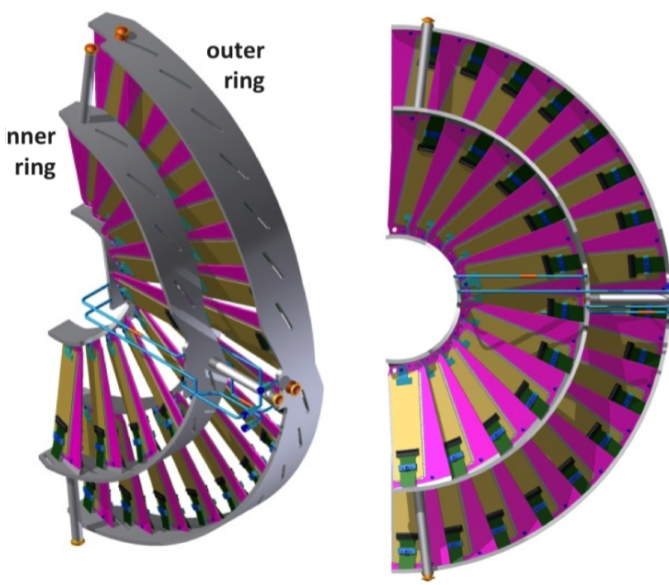


Fig.4. Schematic of the half disks

Each **MODULE** features a n<sup>+</sup>-in-n type silicon sensor with 66,560 pixels each of 100µm × 150µm in size, that is bump bonded to 16 readout chips (ROCs), Fig. 5. This is then glued and wire bonded to a high-density interconnect flex printed circuit (HDI) that distributes signals and voltages (see Fig. 6).

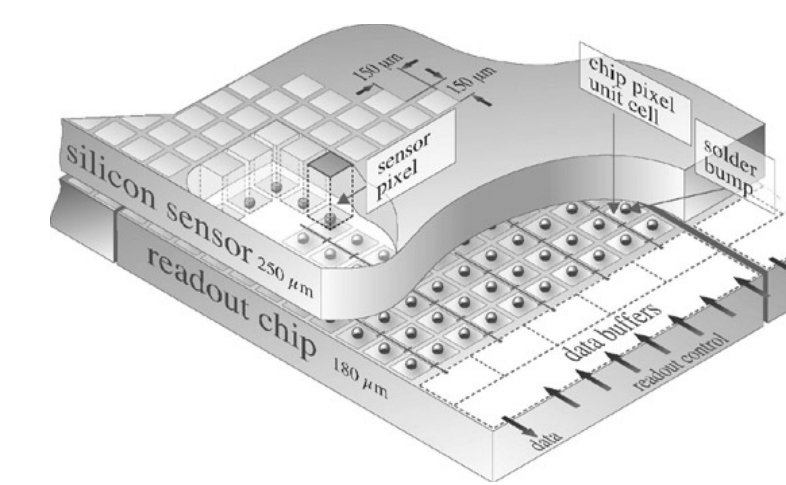


Fig.5 Schematic of the sensor bump bonded to the ROC.

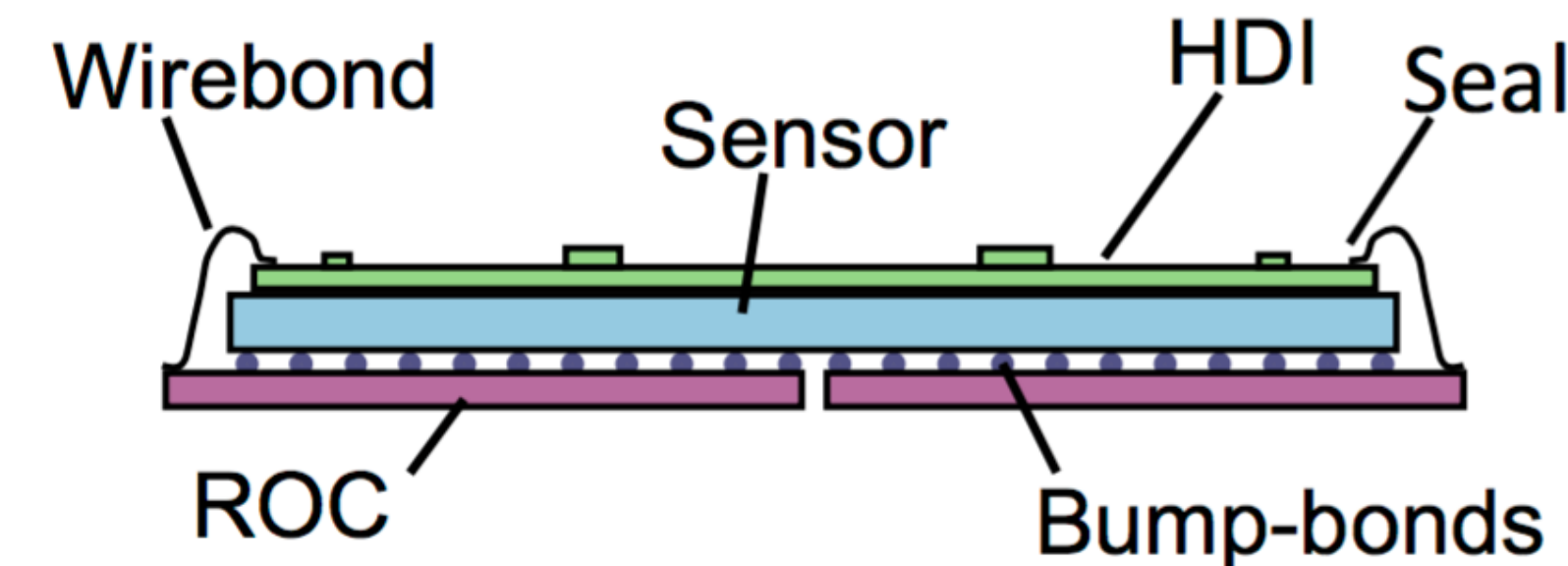


Fig. 6. Shows a cross section of the module components

## Module Testing

There are a total of 672 modules required for the new detector. During each stage of the production the components are tested either electrically, mechanically or by optical inspection. Some of these tests include:

- Measuring the sensor's leakage current (Fig. 8a)
- Testing the ROCs programability and functionality (Fig. 8b)
- Performing a thermal stress test, where the module goes through several cycles between 17°C and -20°C
- Module calibration, where the we unify the signal thresholds for all pixels and optimize the settings of the different digital-to-analog converters (DACs).
- Checking the bump bonding quality (Fig. 8c)
- X-ray testing for energy calibration and for checking readout inefficiencies at high fluxes (Fig 8d)

## Half Disks and the cooling system

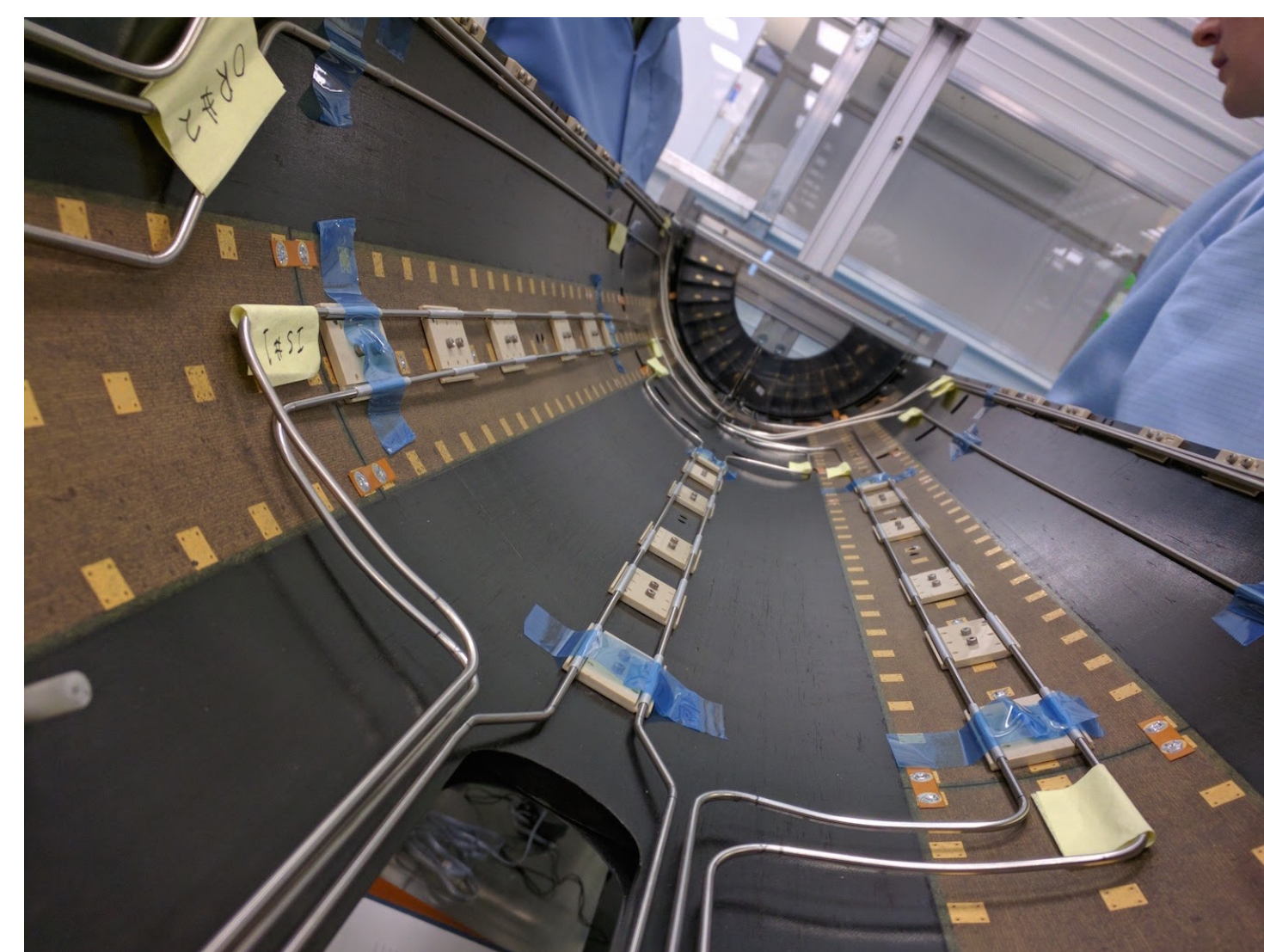


Fig.9. Shows that half cylinder structure and the cooling system

The introduction of CO<sub>2</sub> two-phase cooling is a major innovation of the pixel upgrade, since it greatly contributes to the reduction of passive material in the tracking volume. The choice of CO<sub>2</sub> as refrigerant is advantageous because of its excellent thermodynamical properties that allow the use of very small stainless steel tubes. Fig. 9 shows this cooling system on the half cylinders.

The pixel modules will be mounted on ultra-light-weight carbon fiber support structures integrated with stainless tubes for CO<sub>2</sub> cooling, Fig. 10 .

## Powering the modules

The increase in the number of readout channels by a factor of 1.9 increases the front-end power consumption by the same factor, hence the front-end power consumption plus losses in supply cables, surpasses the current power capacity of the existing system. To overcome this problem we employ DC-DC step-down converters, Fig. 7.

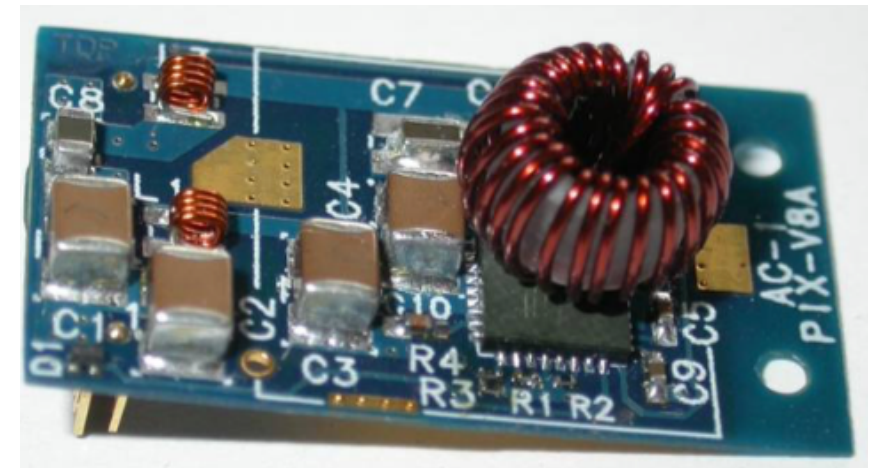


Fig.7. DC-DC converter

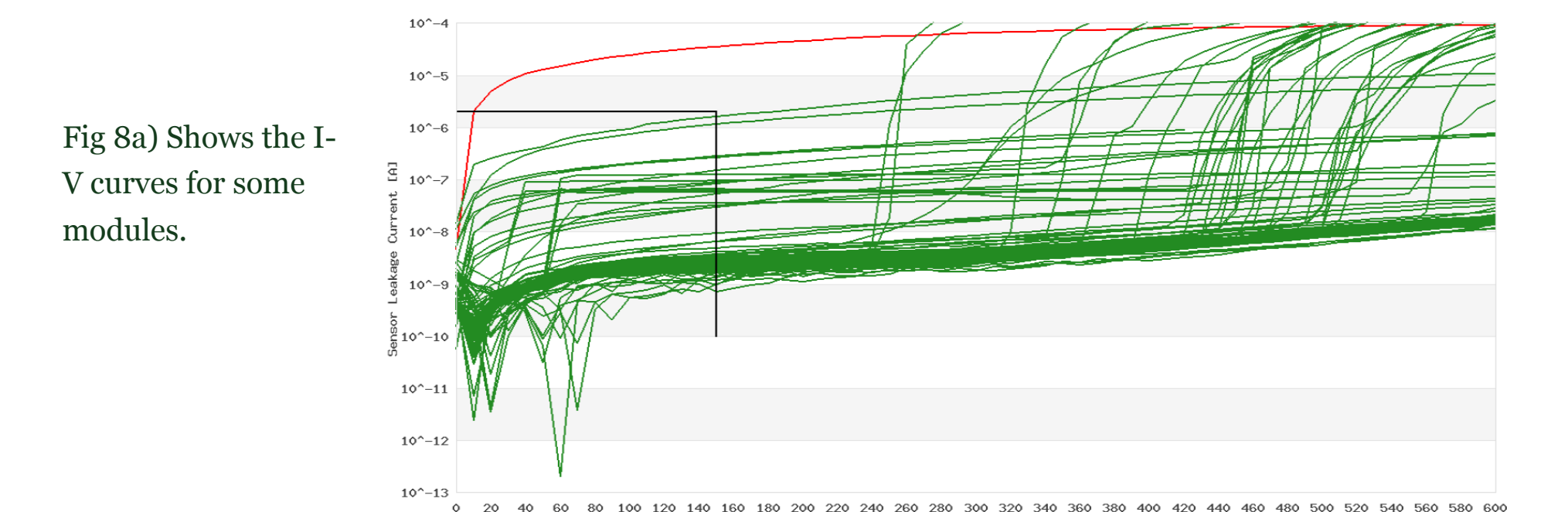


Fig 8a) Shows the I-V curves for some modules.

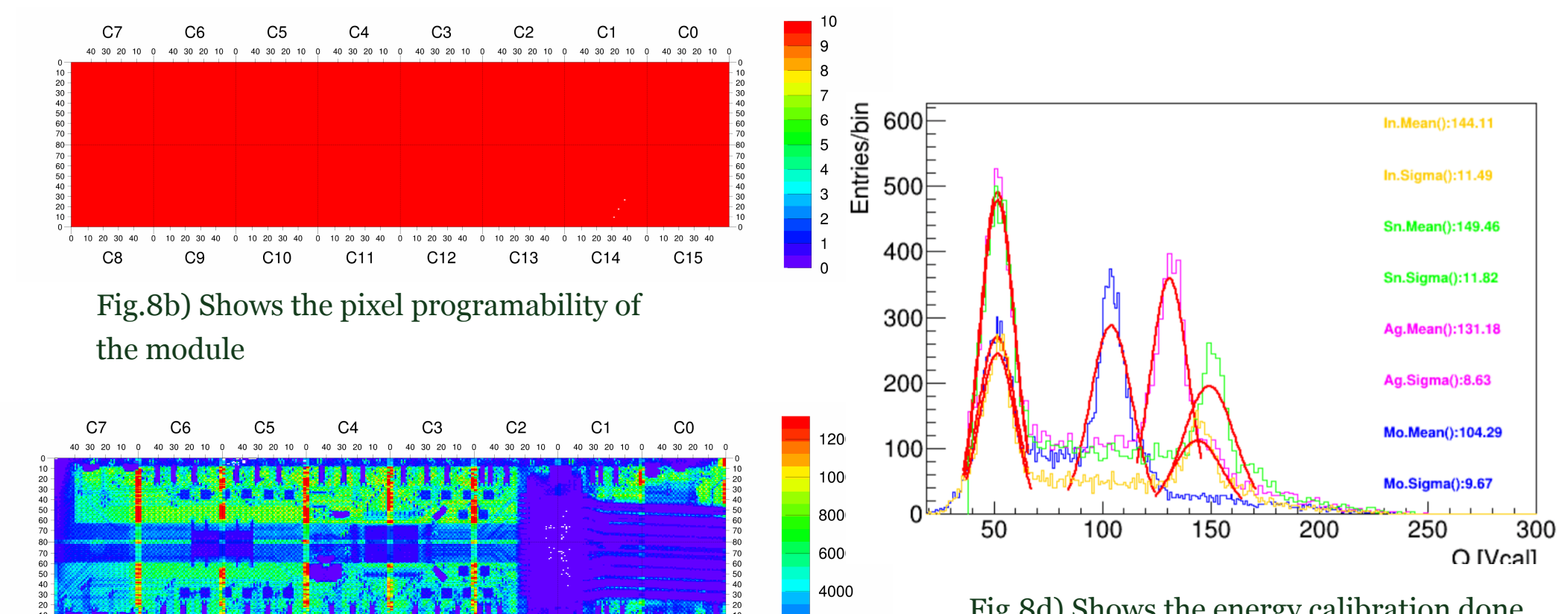


Fig.8b) Shows the pixel programability of the module

Fig.8c) Shows the hit map of the X-ray test

Fig.8d) Shows the energy calibration done with the X-rays.

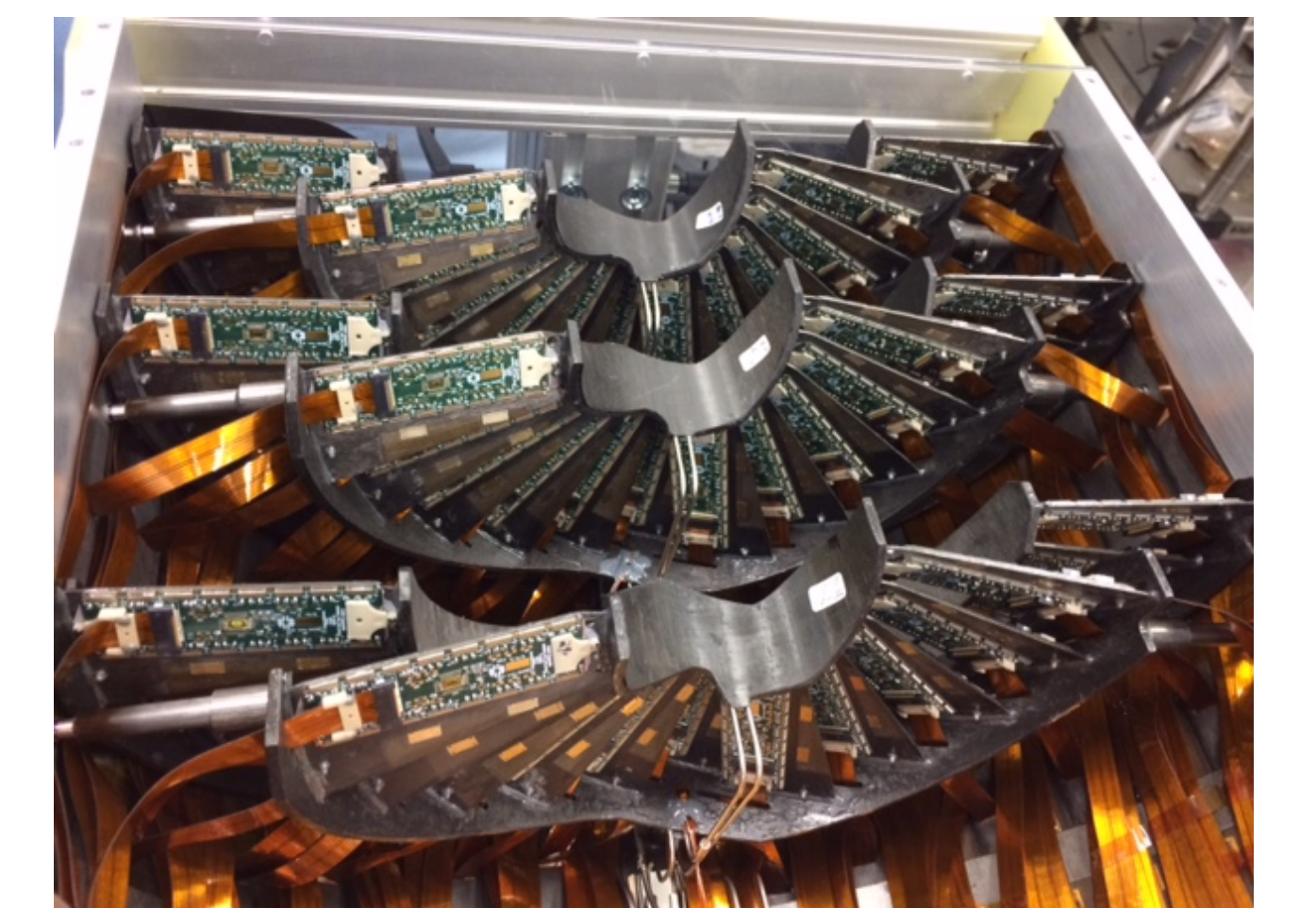


Fig.10. Shows the modules mounted on the half disks

**CONCLUSIONS:** The FPIX will be upgraded during the 2016 winter shut down of the LHC. It will be a more efficient detector that will cope with higher luminosities. The conclusion of the production and testing of the modules is expected to be completed in Fall of 2016.

**REFERENCES:** A.Dominguez et al. [CMS Collaboration] CERN-LHCC-2012-016, CMS-TDR-011. FERMILAB-DESIGN-2012-02.