Upgrade of the ATLAS hadronic Tile calorimeter for the High luminosity LHC

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The Tile Calorimeter (TileCal) is the hadronic calorimeter covering the central region of the AT-LAS detector at the LHC. It is a sampling calorimeter consisting of alternating thin steel plates and scintillating tiles. Wavelength shifting fibers coupled to the tiles collect the produced light and are read out by photomultiplier tubes. An analog sum of the processed signal of several photomultipliers serves as input to the first level of trigger. Photomultiplier signals are then digitized and stored on detector and are only transferred off detector once the first trigger acceptance has been confirmed. The Large Hadron Collider (LHC) has envisaged a series of upgrades towards a High Luminosity LHC (HL-LHC) delivering five times the LHC nominal instantaneous luminosity. The ATLAS Phase II upgrade, in 2024, will accommodate the detector and data acquisition system for the HL-LHC. In particular, TileCal will undergo a major replacement of its on- and off-detector electronics. All signals will be digitized and then transferred directly to the off-detector electronics, where the signals will be reconstructed, stored, and sent to the first level of trigger at a rate of 40 MHz. This will provide better precision of the calorimeter signals used by the trigger system and will allow the development of more complex trigger algorithms. Changes to the electronics will also contribute to the reliability and redundancy of the system. Three different frontend options are presently being investigated for the upgrade and a final solution will be chosen after extensive laboratory and test beam studies that are in progress. A hybrid demonstrator module is being developed using the new electronics while conserving compatibility with the current system. The demonstrator is undergoing extensive testing and is planned for insertion in ATLAS during the next possible opening at the end of 2016.

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1. Introduction

The ATLAS is a general purpose detector designed to study proton and heavy ions collisions at the LHC [1]. The Tile Calorimeter is the hadronic calorimeter of the ATLAS detector [2] covering the central region ($|\eta| < 1.7$). It is divided into the central barrel ($|\eta| < 1.0$, splitted into two parts from read-out point of view) and two extended barrels ($0.8 < |\eta| < 1.7$) along the beam axis presented in Figure 1a. Azimuthally each barrel is segmented into 64 modules, see Figure 1b.

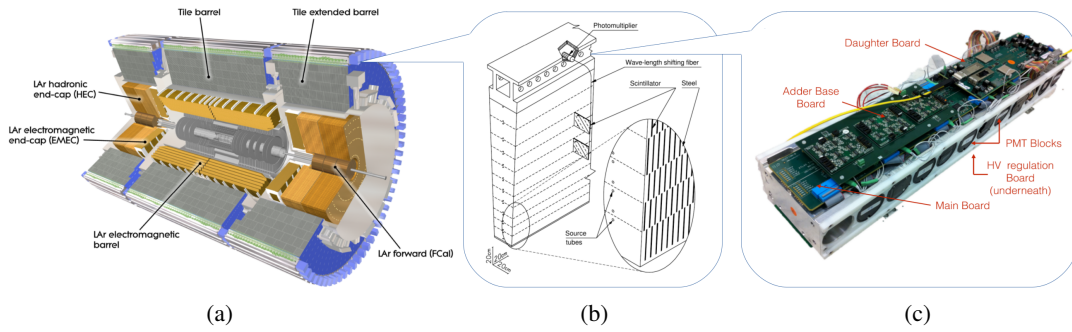|		
(a)	(b)	(c)

Figure 1: A cut-away drawing of the ATLAS inner detector and calorimeters (a), sketch of geometry of one Tile Calorimeter module with the principle of the signal readout (b), Tile Calorimeter hybrid demonstrator minidrawer (c). Taken from Refs. [3, 4].

Scintillating tiles in each module are grouped into individual cells. Each cell is readout by two photomultiplier tubes (PMT) from both sides. Each PMT includes both a photomultiplier and a frontend board (FEB) within the tube. On-detector electronics with PMTs are located at the outermost part of each module (see Figure 1c) in a mechanical structure called super-drawer.

2. Present readout architecture

Figure 2a shows present Tile Calorimeter readout architecture in which a super-drawer is divided into two insertable drawers operating as a whole unit. Figure 2b shows the so called 3-in-1
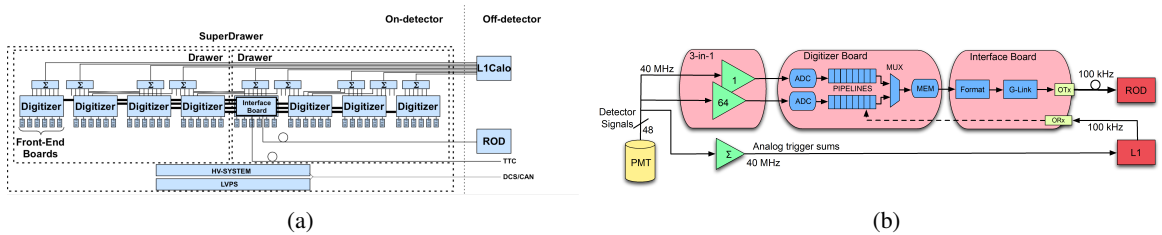

(a)	(b)

Figure 2: Tile Calorimeter super-drawer concept (a) and signal flow in the present system (b) [3].

frontend board which shapes and amplifies an analog signal from the PMT in low and high gains with a ratio of 1:64 [5]. Low gain analog signals from different PMTs are grouped and summed to provide pseudo-projective tower signals to the Level 1 (L1) calorimetric trigger. The 3-in-1 board also includes a charge injection circuit for calibration, and provides slow read-out output via an integrator to Cesium and minimum bias current calibration and monitoring systems. Signals from

both gains are digitized with 10-bit Analog to Digital Converters (ADC) on the Digitizer Board at a sampling frequency of 40 MHz. Samples are stored into pipeline memory waiting the L1 trigger decision. After receiving the L1 trigger acceptance the corresponding seven consecutive samples are selected from the memory for all PMTs of the module, packed into a fragment, and sent to the Read Out Driver (ROD) system by the Interface Board via high speed optical links with frequencies up to 100 kHz. The ROD is the main component of the off-electronics which performs preprocessing and gathering data coming from the FEB and sends data to the High Level Trigger (HLT). Timing Trigger and Control (TTC) system provides each module with clocks, trigger signals, and control and configuration capabilities. The High and Low Voltage Power Supplies (HVPS and LVPS) are controlled and monitored by the Detector Control System (DCS).

3. Upgraded readout architecture

Figure 3a shows the upgraded Tile Calorimeter readout architecture in which a super-drawer is divided into four insertable and independent minidrawers to increase maintainability, serviceability, reliability and minimize single point of failure. Each minidrawer contains 12 PMTs, Main

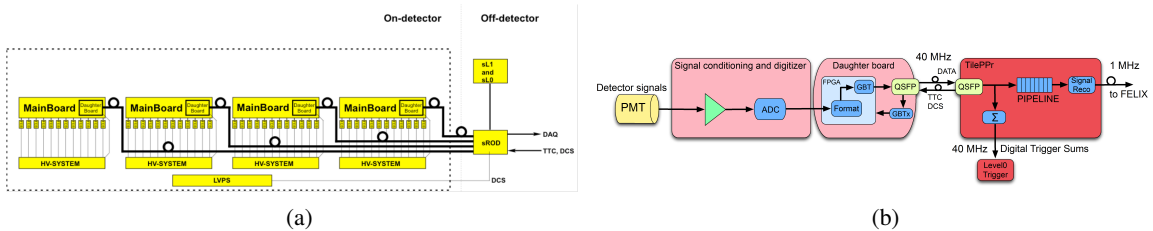(a)   (b)

Figure 3: Tile Calorimeter super-drawer concept (a) and signal flow for HL-HLC upgrade (b) [3].

Board (MB), and Daughter Board (DB) [6]. The FEB and MB together provide conditioning, amplification and digitisation analog signal from PMT. The MB delivers digitized data to the DB. It is also responsible for control and monitoring FEBs, and low voltage distribution in the minidrawer. The analog pulses from the PMTs are conditioned and digitized at a rate of 40 MHz and continuously transferred to the off-detector electronics to TilePreprocessor (TilePPr) via high speed optical links by DB, see Figure 3b. The MB and DB contain two fully independent halves with power, data links, calibration and monitoring services on each side. Such architecture provides read out of each cell by two independent PMTs with separate power, services and data links up to off-detector electronics.

The TilePPr or super ROD [7] can control and read out one complete Tile Calorimeter super-drawer (four minidrawers). It receives and processes digital data from the DB. The TilePPr is also responsible for decoding and distributing Trigger Timing and Control (TTC) signals to the FEB for configuration and synchronization with the LHC clock. It also provides control and monitoring of the high voltage power supplies through a Detector Control System (DCS) interface.

Three FEB options have been developed and are currently undergoing thorough testing. All of them include a charge injection circuit for calibration and an slow integrator for Cesium and mimimum bias current calibration and monitoring.

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The first option is redesigned 3-in-1 FEB [6] presented in Figure 4. It is based on discrete elements and provides better linearity and lower noise with respect to the used one now. An analog PMT signal is shaped by passive LC shaper and amplified in low and high gains with a ratio of 1:32. Both gains are digitized with 12-bit ADC located on MB at a sampling frequency 40 MHz.

A second approach is Charge (Q) Integrator and Encoder (QIE) [8] presented in Figure 5. It is based on an ASIC chip that includes current splitter in four gains followed by gated integrator and an on-board 7-bit ADCs. The QIE does not perform pulse shaping, minimizing pile-up problems and allowing raw PMT pulses to be measured.

A third approach is Frontend for ATLAS TileCal Integrated Circuit (FATALIC) [9] presented in Figure 6. It is also based on an ASIC chip and includes current conveyors with three different gains (1, 8, 64) to cover the PMT signal dynamic range, followed by active shapers for all gains to improve the signal to noise ratio. All gains are digitized with 12-bit pipelined ADCs.
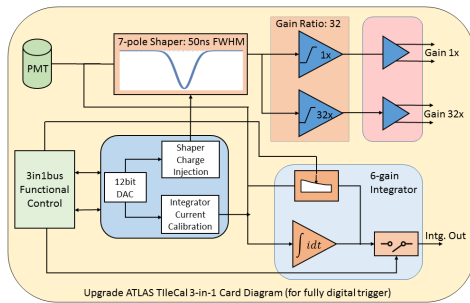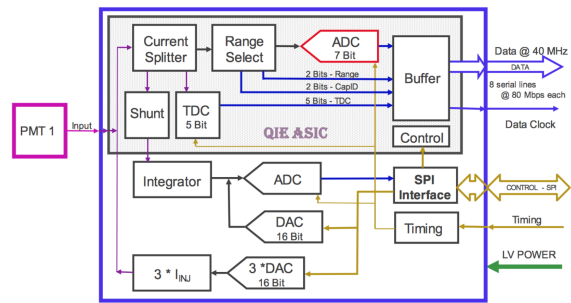

Figure 4: The 3-in-1 frontend board.

Figure 5: QIE frontend board [8].

Eight LVPS bricks located at the outer end of each TileCal module receive bulk 200 V and produce two independent +10 V lines per minidrawer using switching power generation techniques, see Figure 7. In this scheme each LVPS brick provides low voltage for one side of the minidrawer and has the possibility to provide power for the other side to increase redundancy. Two lines of
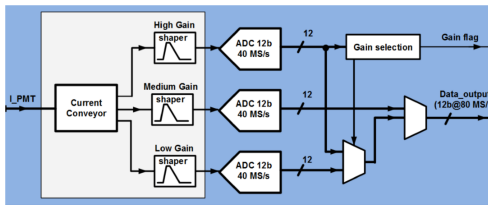

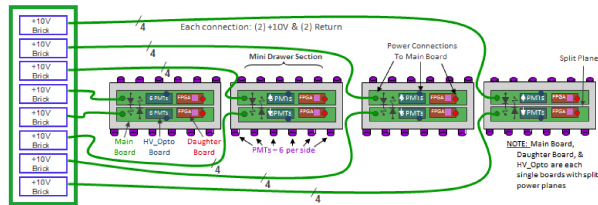Figure 6: FATALIC basic circuit architecture [9].

Figure 7: LVPS distribution in super-drawer and on-detector HV solution [10].

+10 V which are received by each MB are regulated using Point Of Load to produce different voltages, which are distributed within the minidrawer. Two HVPS options with individual PMT control are studied. An on-detector solution uses one radiation hard High Voltage (HV) Board per minidrawer, that provides HV up to 12 channels which is controlled via the DB. An alternative, remote solution distributes the HV for each PMT from the off-detector by routing 12 HV cables to each mini-drawer. To restore linearity in a high luminosity environment active dividers are used in the PMT voltage divider chain.

4. Conclusion

A Tile Calorimeter hybrid demonstrator module is being developed using the new electronics while conserving compatibility with the current system. It has been interfaced with legacy control, monitoring, and calibration infrastructure. Most components passed radiation tests for high luminosity. Figure 8 shows that the control and calibrations tests have proved successful in the Tile Calorimeter hybrid demonstrator module. It is undergoing elaborate testing. The test beam was
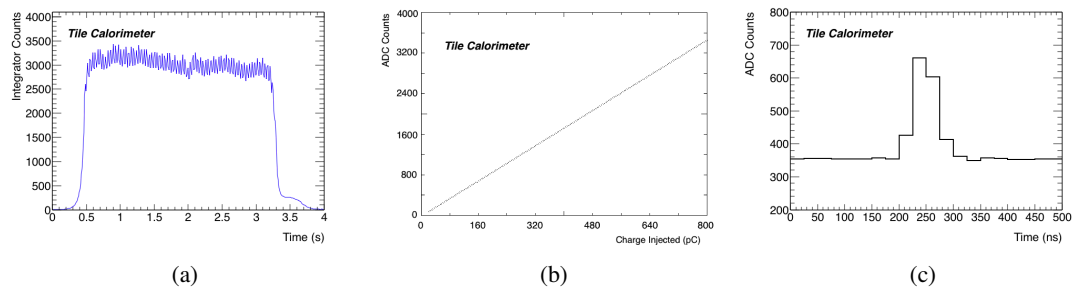
Figure 8: Calibration plots taken with Tile Calorimeter hybrid demonstrator module [3]: Integrator response to Cesium source (a), Charge injection scan (b), Laser pulse of several hundred GeV (c).

in 2015 and there will be more test beam campaigns in 2016. The hybrid demonstrator module is planned for insertion in ATLAS at the end of 2016 to be tested under real conditions.

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