Upgrade of the Inner Tracking System of ALICE

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The upgrade of the Inner Tracking System (ITS) of ALICE is planned for the second long shutdown of the LHC in 2019–2020. The ALICE physics program after the shutdown requires the ITS to have improved tracking capabilities and improved impact parameter resolution at very low transverse momentum, as well as a substantial increase in the readout rate. To fulfill these requirements the current ITS will be replaced by seven layers of Monolithic Active Pixel Sensors. The new detector will be moved as close as 23 mm to the interaction point and will have a significantly reduced material budget. Several prototypes of the sensor have been developed to test different aspects of the sensor design including prototypes with analog and digital readout, as well as small and final-size sensors. These prototypes have been thoroughly characterized both in laboratory tests and at test beam facilities including studies on the radiation hardness of the sensors. This contribution gives an overview of the current status of the research and development with a focus on the pixel sensors and the characterization of the latest prototypes.

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1. Upgrade of ALICE

The ALICE experiment was designed to study the properties of the quark-gluon plasma created in heavy-ion collisions at the LHC. Since the start of the LHC, ALICE has confirmed the existence of the quark-gluon plasma and extended the precision and kinematic reach of many significant probes measured previously at RHIC and at the SPS. After the second long shut down of the LHC in 2019–2020, ALICE will focus on the measurement of heavy-flavor hadrons, quarkonia and low-mass dileptons at low transverse momenta [1]. This requires high-precision measurements at low p_T resulting in the need of recording large samples of minimum-bias events. In order to achieve this, ALICE is planning to read out all Pb-Pb collisions delivered by the LHC which corresponds to a maximum collision rate of 50 kHz. The upgraded detector will record an integrated luminosity of 10 nb^{-1} in Pb-Pb collisions which means a factor 100 compared to the data that will be recorded by 2019.

To cope with the physics requirements of ALICE several upgrades will take place during the second long shut down of the LHC. Two new detectors will be installed: a high resolution, low material Inner Tracking System (ITS) and a Muon Forward Telescope (MFT). They will be accompanied by a new beampipe with a smaller radius which will allow the first layer of the ITS to be moved closer to the interaction point resulting in better impact-parameter determination. The readout chambers of the Time Projection Chamber (TPC) will be replaced by Gas Electron Multiplier (GEM) detectors and its readout electronics will be upgraded together with the readout electronics of the Transition Radiation Detector (TRD), the Time Of Flight (TOF) detector and the Muon Spectrometer. The forward trigger detectors, the online system and the offline reconstruction and analysis framework will also be upgraded [1].

2. Upgrade of the Inner Tracking System

The Inner Tracking System is situated at the center of ALICE closest to the interaction point (Fig. 1). The data taking by the ITS before the first long shut down of the LHC has been successful and data taking has been already resumed since the restart of the accelerator [2].

However, the current detector is not suited for the physics requirements of ALICE after the second long shut down of the LHC, and an upgrade is necessary to improve the physics performance of ALICE in several ways. The impact parameter resolution at $p_T = 500$ MeV/c will be improved by a factor 5 in the direction of the beam and a factor 3 in the transverse direction which will be achieved by different steps. Firstly, the smaller beampipe will allow the first layer of the ITS to be moved as close as 23 mm to the interaction point instead of the current 39 mm. Secondly, the material budget of the detector will be reduce from around 1.14% X_0 to around 0.3% X_0 for the three innermost layers and finally the pixel size will be reduced to about 30 μm × 30 μm from the current 50 μm × 425 μm. The upgraded detector will also have an improved tracking efficiency and p_T resolution at low p_T. To achieve this, the current six layers of hybrid pixel, strip and drift detectors will be replaced by seven layers of monolithic pixel detectors.

Right now ALICE is limited by the current ITS in the readout speed to 1 kHz. After the upgrade, ALICE is planning to read out all Pb-Pb collisions at the maximum rate of the LHC: thanks to the design of the new detector a readout rate of more than 10^5 Hz in Pb-Pb events and
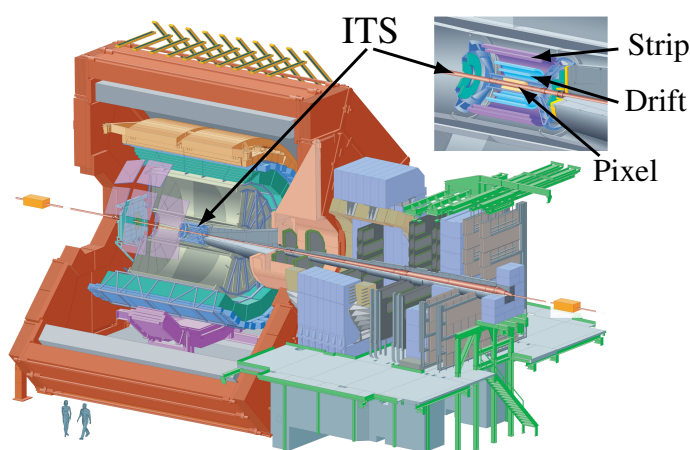
Figure 1: Current setup of the ALICE detector with the ITS highlighted.

several 10^5 Hz in pp events will be possible. The requirement to remove and reinsert the detector during the yearly shut down of the LHC places further strong constraints on the design of the mechanical support of the detector.

The seven layers of the new ITS cover an area of around 10 m^2 and will consists of around 1.25×10^{10} pixels. The layers will be grouped according to the following: the three innermost layers make up the Inner Barrel and the four outermost layers the Outer Barrel. The radial arrangement of the layers can be seen in Fig. 2. All the layers will be segmented into elements called staves which extend the full length of the detector in the direction of the beam. A stave is the smallest operable unit of the detector and has a slightly different design in the case of the Inner and Outer Barrel. The first prototypes of both the Inner and Outer Barrel staves can be seen in Fig. 3.
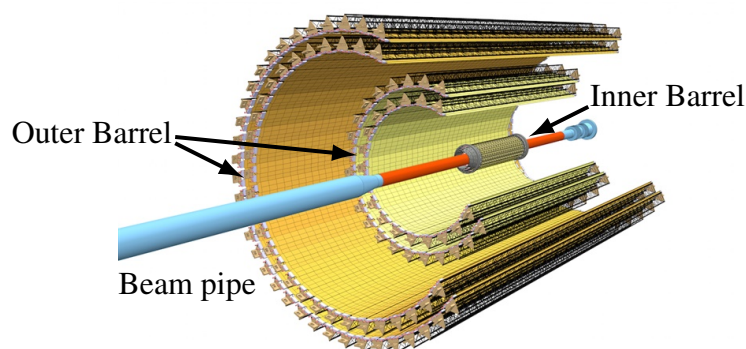

Figure 2: Layout of the layers of the upgraded ITS. Figure is taken from [3].

Since the distance of the layers from the interaction point vary from 23 mm to 400 mm, the working environment and the requirements are very different on the innermost and the outermost layers. The requirements for the different layers are summarized in Tab. 1. The whole detector is planned to be equipped with the same chip, resulting in very stringent requirements on material budget, spatial resolution, detection efficiency, power density and fake hit rate. On the other hand,
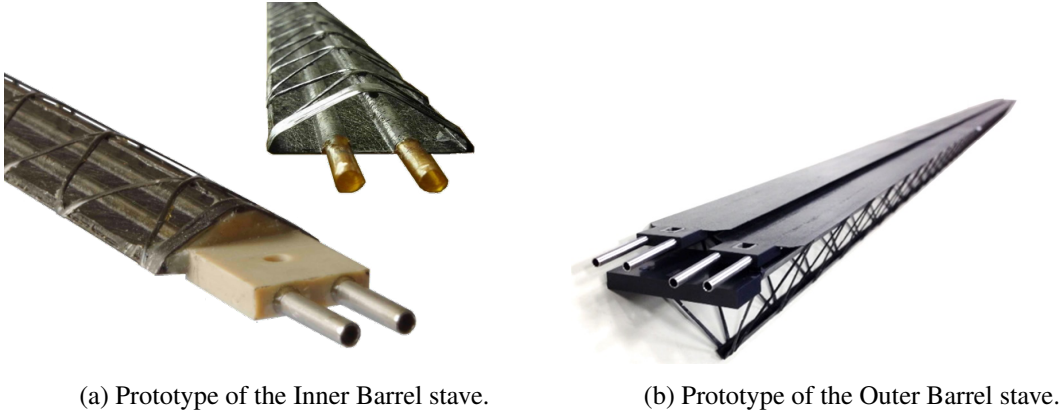
(a) Prototype of the Inner Barrel stave.   (b) Prototype of the Outer Barrel stave.

Figure 3: Stave prototypes.

Parameter	Inner barrel	Outer barrel
Silicon thickness	50 µm	
Spatial resolution	5 µm	10 µm
Power density	$< 300 \, \text{mW/cm}^2$	$< 100 \, \text{mW/cm}^2$
Event resolution	$< 30 \, \mu\text{s}$	
Detection efficiency	$> 99\%$	
Fake hit rate	$< 10^{-5}$ hit per event per pixel	
Average track density	$15\text{–}35 \, \text{cm}^{-2}$	$0.1\text{–}1 \, \text{cm}^{-2}$
TID radiation	2700 krad	100 krad
NIEL radiation	$1.7 \times 10^{13} \, 1 \, \text{MeV} \, \text{n}_{eq}/\text{cm}^2$	$10^{12} \, 1 \, \text{MeV} \, \text{n}_{eq}/\text{cm}^2$

Table 1: Requirements for the Inner and Outer Barrel for the upgraded ITS. Radiation levels include a safety factor of 10. Values are taken from [3], but the radiation levels are updated according to the latest estimates.

the expected radiation environment is relatively modest compared to the radiation levels expected in CMS or ATLAS at the same distance from the collision point. These requirements led to the choice of using Monolithic Active Pixel Sensors for the upgrade of the ITS.

3. Technology choice

In the previous chapter the requirements for the chip for the ITS upgrade was discussed showing that the technology of CMOS Monolithic Active Pixel Sensors (MAPS) suits well these requirements. The first implementation of this technology in a heavy-ion physics experiment was the STAR PXL detector which has been installed in 2014 [4]. The ULTIMATE chip used for the STAR PXL detector however does not meet all the requirements of the ALICE ITS, particularly in terms of readout time. The ULTIMATE chip has a readout time of 190 µs whereas for the ITS upgrade the design goal is to stay below 30 µs. The development of a new chip is therefore needed for the ITS upgrade and the chosen technology is the TowerJazz 0.18 µm CMOS imaging process
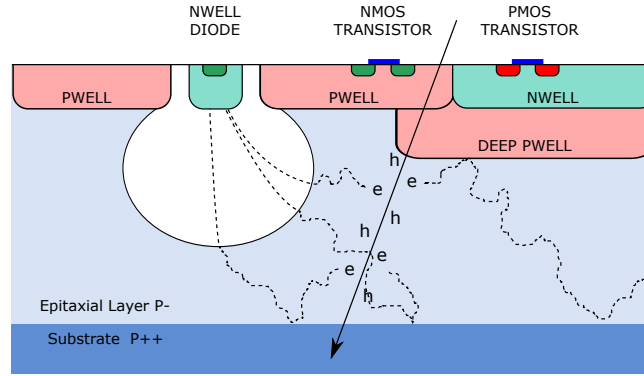
Figure 4: Cross section of one pixel in the TowerJazz 0.18 μm CMOS imaging process. Figure is taken from [3].

for which the schematic cross section of a pixel is shown in Fig. 4. The transistor feature size of 0.18 μm and the available six metal layers in this technology allow for the implementation of high density and low power digital circuitry. The small transistor feature size and the gate oxide thickness of 3 μm also make this technology more radiation tolerant than the 0.35 μm technology used up to now as the baseline in particle-physics applications.

The mechanism of the detection of particles in this technology is the following: the crossing particle generates electron-hole pairs in the high resistivity epitaxial layer; these electrons then diffuse until they reach the depleted volume within which they drift towards the collection n-well electrode where they are collected. Being able to produce the chip on a high resistivity epitaxial layer ($\gtrsim$ 1 kΩ cm) is important, because it results in larger depletion volumes and thus better charge-collection efficiency. It also results in the electrons being less likely to be trapped, making the technology more radiation hard towards non-ionizing radiation. An important feature of the technology is the implementation of the deep p-well which allows the use of CMOS circuitry within the pixel area by shielding the n-well of the PMOS transistors from the epitaxial layer. Without such a shielding, the n-wells of the CMOS transistors would compete in the collection of the electrons with the collection diode and this would result in a lower charge-collection efficiency. For some prototypes a moderate bias voltage can be applied to the substrate ($<$ 10 V) to create a larger depletion volume around the collection diode. This results in a smaller capacitance and consequently in a better charge-collection efficiency. The capacitance can be further reduced by keeping the collection n-well diode small, which in the case of the current prototypes is 2–3 μm.

4. Chip architectures

4.1 ALPIDE and MISTRAL-O

There are two parallel chip developments ongoing for the upgrade of the ITS, the ALPIDE and the MISTRAL-O. The two chips are designed such that their dimensions, physical and electrical interface are identical, so either of them can be used for the upgrade without any modifications in the mechanical and electrical services. The schematic design of the matrix layout can be seen in Fig. 5 for the two architectures.
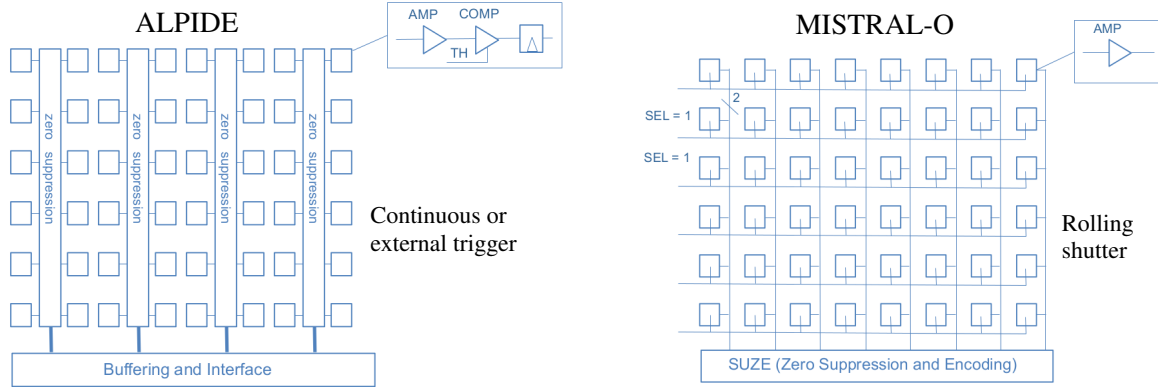
Figure 5: Schematic design for the ALPIDE and MISTRAL-O architectures.

The MISTRAL-O development is a continuation of the ULTIMATE chip development. It has amplification within the pixel, the analog signal is then propagated to the end of column and the digitalization and zero suppression is done at the end of column. In the case of the ALPIDE the amplification, the digitalization and zero suppression is done within the pixel, so that only digital signals are propagated to the end of column. This allows for a data driven readout in the case of the ALPIDE while the MISTRAL-O is read out in the more traditional rolling shutter mode with an event-time resolution of around 20 µs. The event-time resolution of the ALPIDE is $\lesssim 2$ µs and is determined by the rise time of the pulses. The power consumption, the dead area and the pixel pitch is smaller in the case of the ALPIDE (exact values can be seen in Tab. 2) and both chips show good performance in noise occupancy and detection efficiency measurements which resulted in the choice of the ALPIDE as the baseline for the project. The current document focuses on the ALPIDE architecture, while details on the MISTRAL-O family can be found in [5].

	ALPIDE	MISTRAL-O
Pixel pitch	28 µm × 28 µm	36 µm × 65 µm
Event time resolution	$\lesssim 2$ µs	~ 20 µs
Power consumption	39 mW/cm^2	80–90 mW/cm^2
Dead area	1.1 mm × 30 mm	1.5 mm × 30 mm

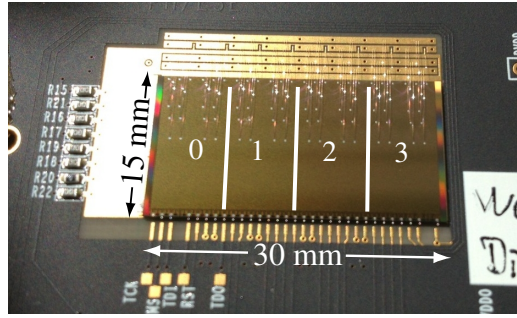Table 2: Performance and specification of the ALPIDE and MISTRAL-O architectures.

Figure 6: Picture of the pALPIDE-1 chip with the four sub-matrices indicated.

4.2 pALPIDE-1

The pALPIDE-1 chip is the first prototype of the ALPIDE family with the final chip size of 15 mm $\times$ 30 mm. It has 512 $\times$ 1024 digital pixels with the size of 28 μm $\times$ 28 μm. It is read out using an asynchronous priority encoder network, thanks to which only hit pixels are read out resulting in very fast acquisition of the data from the full matrix. The chip is organized in four sub-matrices consisting of different types of pixels. A picture of the chip can be seen in Fig. 6 with these sub-matrices indicated. They differ in either the reset mechanism of the pixels or in the spacing between the collection diode and the surrounding p-well. In the following, results will be reported for only one of these pixel variations.

5. Characterization of the pALPIDE-1 prototype

5.1 Methods and tools

In the upgraded ITS the pixel chips will be laser soldered to the flexible printed circuit which will give both the mechanical and the electrical connection, while for testing, the prototypes are wire bonded to a carrier card as can be seen in Fig. 6. The carrier card is then connected to the readout board by a PCI Express connector and the readout board is connected via USB to the computer (Fig. 7a). The first tests of the chips (noise and threshold measurements, noise occupancy determination) are done in this setup while for the detection efficiency and spatial resolution measurements a stack of this setup is used. The stack consists of seven pALPIDE-1 chips where the outer six are the tracking planes and the central one is being tested (Fig. 7b). The seven chips are connected to a computer the same way as the individual chips are and the readout is done by the EUDAQ framework [6]. The analysis of the data collected at beam tests is then done by the EUTelescope software [7].

5.2 Performance

The pALPIDE-1 prototype has been thoroughly characterized both in laboratory measurements and in several test beam campaigns at different test beam facilities (PS, SPS, DESY, BTF and PAL). The beam energy at these facilities range from 60 MeV to 120 GeV and the particles used are electrons, positrons and pions. The following results were obtained at the PS using a 6 GeV negative pion beam.
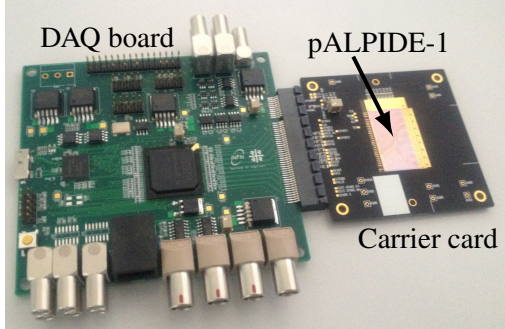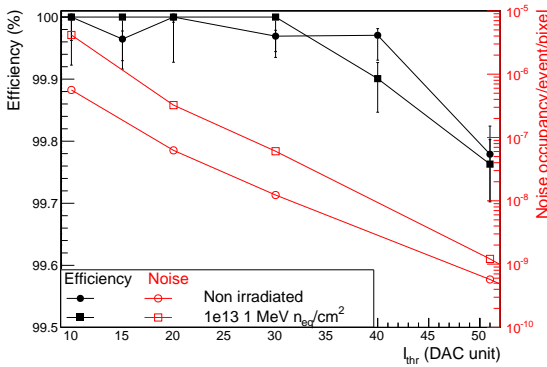
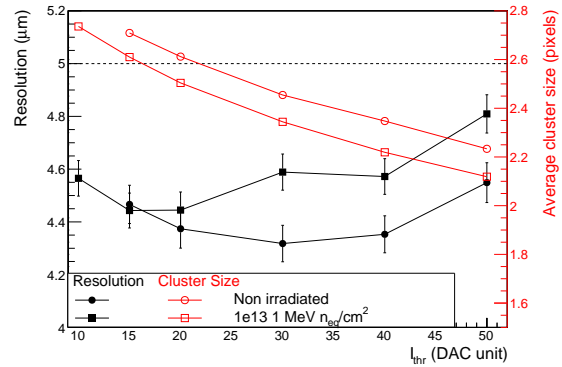(a) Photo of the readout board and the chip wire bonded to the carrier card.
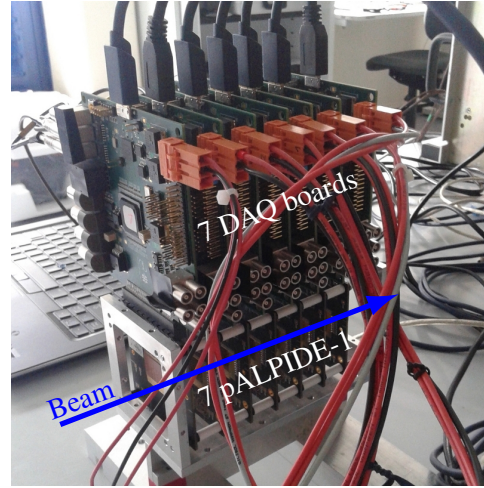
(b) Test beam setup.

Figure 7: Setup used in the measurements for the readout of the pALPIDE-1.

(a) Detection efficiency (left axis) and noise occupancy (right axis) results. The noise occupancy values were calculated after masking the 20 most noisy pixels.


(b) Spatial resolution (left axis) and average cluster size (right axis) results. The spatial resolution is calculated by assuming 2.39 μm pointing resolution for the tracks.

Figure 8: Results for the pALPIDE-1 from measurements at the PS using a 6 GeV negative pion beam. The data for both figures were taken applying -3 V reverse substrate bias and is shown as function of the threshold current.

The results are summarized in Fig. 8 where the left panel shows the detection efficiency and noise occupancy values of the pALPIDE-1 while the right panel shows the spatial resolution and the average cluster size of the chip. Both figures show the results as a function of the threshold current which is a parameter of the chip used for setting the input charge threshold of the pixels. The requirements for the ITS upgrade is to have a detection efficiency better than 99% and noise occupancy lower than 10^{-5} hits/event/pixel. In Fig. 8a it can be seen that both requirements can be fulfilled at a wide operating range of the threshold current. The performance in terms of detection efficiency does not degrade after irradiating the chip by 10^{13} 1 MeV n_{eq}/cm^2, but the

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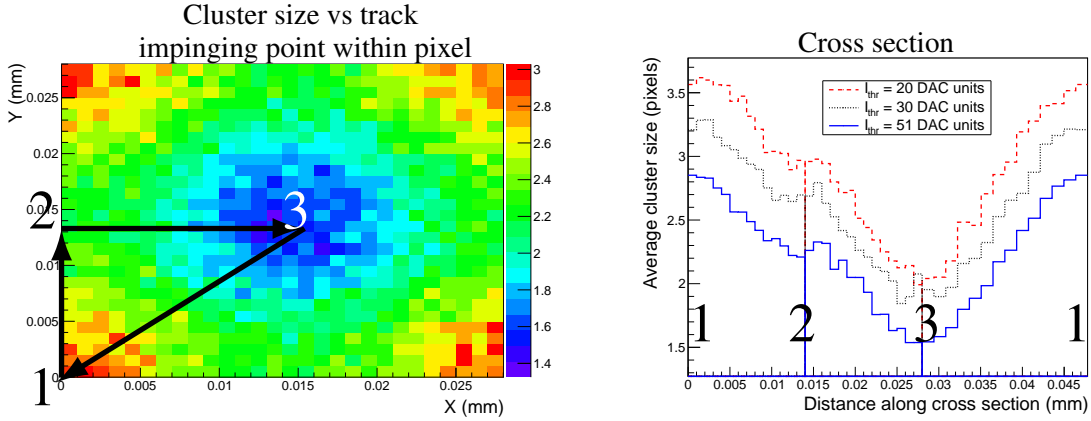
(a) Dependency of the average cluster size on the impinging point of the track within the pixel.

(b) Cross section of figure (a) along the indicated arrows.

Figure 9: Results for the pALPIDE-1 from measurements at the PS using a 6 GeV negative pion beam. The data for both figures were taken with non optimal setting for the chip (applying 0 V reverse substrate bias) to emphasize the effect on the cluster size.

noise occupancy values become slightly higher. In Fig. 8b it can be seen that there is also a large operational margin in terms of spatial resolution where the requirement for the chip is to stay below 5 μm which is fulfilled both before and after irradiation by 10^{13} 1 MeV n_{eq}/cm^2.

In Fig. 9 the average cluster size is shown as a function of the impinging point of the track within a pixel. It is smallest if the track goes through the center of the pixel, close to the collection diode and largest if the track goes through the corner of the pixels where it is more likely to have charge-sharing with the neighboring pixels.

6. Summary

The Inner Tracking System of ALICE will be upgraded during the second long shut down of the LHC in 2019–2020 to fulfill the physics requirements of ALICE after the shut down. The new detector will have seven layers of Monolithic Active Pixel Sensors and will improve significantly the tracking and p_T resolution at low p_T, as well as the impact-parameter resolution. The first large-scale prototypes of both ALPIDE and MISTRAL-O have been thoroughly characterized and show very good performance with a wide operational margin. Tests have also been carried out with irradiated sensors and the chips show good performance after an irradiation level of 10^{13} 1 MeV n_{eq}/cm^2. Overall the development of the new detector is progressing according to schedule with all aspects of the R&D close to completion.

7. Acknowledgement

References

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