PROCEEDINGS OF SCIENCE

Fast data acquisition measurement system for plasma diagnostics using GEM detectors

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This paper refers to measurement system for plasma diagnostics for tokamaks currently being developed. For the most of the GEM detector readout structures, large number of input channels is required to form a working measurement system. This constraint is especially important for two-dimensional GEM readout structures. Presented measurement system layout is a general model for further implementation. The system is based on fast serial gigabit links and PCI-Express interface for communication. The system can support up to 512 measurement channels, per each PCI-Express x16 slot. The system consists of several modules – PCI-Express 8-to-1 switch, Analog Front End, ADC Front End, and FPGA backplane boards. Implemented data processing algorithms enable fast raw data acquisition and real-time processing. The integration algorithms allow measurement system to cooperate with GEM detector working at high rates.

First EPs Conference on Plasma Diagnostics - 1st ECPD
14-17 April 2015,
Villa Mondragone , Frascati (Rome) Italy

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1. Introduction

This paper refers to the measurement system for plasma diagnostics of tokamaks, that is currently being developed. In thermonuclear fusion research reactors, precise determination of the level and spatial distribution of the plasma soft X-ray radiation will be important for plasma parameters optimization. The system is based on the Gas Electron Multiplier (GEM) detector with high speed communication interfaces and effective algorithms for data processing, implemented in the FPGA units and in real time software [1]. The current implementation of the system's hardware allows achieving high signal rates from the detector. The system can work in two modes: First mode performs fast raw data acquisition of the analog signals, giving therefore important information about the plasma or other radiation sources. On the contrary, the second mode performs an online calculation of the charges registered on the GEM channel. Further post processing is done by software running on embedded PC. Due to the modular structure of the measurement system, GEM detector readout boards can have different readout structures (1D, 2D, redundant, etc.). The system can work with connected both one- or two- dimensional readout boards. In order to provide high throughput of the data to the post-processing algorithms, advanced gigabit serial communication interfaces are used.

The main goal of the work was to develop a new generation of SXR measurement system with a large number of measurements channel and high sampling speed. The first generation of the system included 256 readout channels, whereas the sampling frequency was 77 MHz, with 10 ms minimum time resolution [2][3]. The system was based on large number of FPGA units. The new generation of the system can provide even 2048 input channels, with sampling speed of 125 MHz for each channel. The samples resolution as well the strip charge rate will be significantly increased. The number of the FPGA processing units is also reduced to only 4 per 256 channels (Xilinx Artix7 FPGAs). The algorithms will be reworked, in order to work with very intense photon fluxes. The system is highly modular, thus allowing to work with custom number of channels and readout boards.

2. GEM detector readout structures

The main components of a GEM detector, which is filled with special gas mixture, are: window, GEM foils and readout board. The measurement process starts when an photon hits the GEM's window, where it is converted to an electron. Then it passes through GEM foils connected to high voltage. Due to the presence of the electric current, the electron is multiplied each time it passes through a sheet of foil. If three layers of foil are installed in the GEM detector, the amplification ratio is as high as around 1000 times. Finally, the produced cone-shaped cloud of electrons hits the readout board. Channel construction is based on a PCB board with copper stripes. The number of copper stripes determines the spatial resolution of the detector. Since the analog pulses are very narrow, with length of tens of nanoseconds, the system must provide high number of fast readout channels. This results in satisfactory spatial and event resolution.

Most commonly used GEM detector readout structures are one- and two- dimensional. One-dimensional readout boards are simpler for analysis in terms of position of the photons absorbed in the detector conversion layer. They require less channels and provides good spatial

resolution. In case of a two-dimensional readout board, measurement systems require connection of twice or three times more signals from the readout board. The position and charge calculation algorithms are also much more complex [4]. However, this kind of structure (e.g. honeycomb pixels) is useful for the experiments with different intensity of radiation, e.g. plasma generated by the lasers. Complex readout structures of GEM detector require simultaneous, high-speed processing of large amount of channels by the measurement system [5].

3. Measurement system layout

The measurement system hardware model consists of several modules. The description is based on 64 channels configuration of the system. The GEM detector's analog output channels (from readout board) are connected to the Analog-Frontend boards (AFE). The design is radiation-hard, allowing mounting of the units in different places, near high electromagnetic fields and in neutron flux. Boards contain preamplifier and shaper circuits, offset correction and fast comparators. Boards can also work in analog charge integration mode. The analog signals are transmitted to the ADC Frontend boards (ADCFE) using high speed differential cables.

The most important parts of the ADCFE boards are 12-bit ADCs. Each of them can simultaneously acquire signal from 16 channels with 125 MHz sampling speed. ADCFE boards also communicate with integrated circuits on the AFE boards using serial communication links in LVDS standard (Low-Voltage Differential Signaling, especially useful for high speed data transmission with good immunity to the external noise) and moreover provide diagnostics of the hardware, e.g. current and temperature monitoring.

Digital samples of raw or integrated analog signals from the GEM detector, are transmitted to the FPGA backplane boards from the ADCFE boards using serial LVDS interfaces. On each FPGA backplane board up to 4 ADCFE boards can be mounted. The board can handle up to 64 measurement channels. The main processing unit of the board is a Artix7 FPGA. FPGA firmware handles several functions, including:

- Acquisition of the signals from the ADCs (from ADCFE boards) – fast interface drivers for ADCs mounted on ADCFE boards
- Data processing:
    - charge integration algorithms – necessary for high rate, online raw data processing (the raw data comes as pulses that need to be further processed in order to get charge values of the photons),
    - timestamps – markers for charge data in order to properly place in time the charge values (e.g. plasma tomography purposes)
- Data management – DDR3 memory data storage and control algorithms, including specialized DDR3 memory drivers
- System configuration and monitoring – clock distribution and ADCs initialization, signal offset calibration, temperatures and currents readout etc.
- Communication with the measurement system concentrator using PCI-Express links

The final position and energy calculation takes place in the embedded PC unit at the post-processing stage. The backplane boards (FPGA units with pre-processing algorithms) are connected to the PC via data concentrator using PCI-Express communication links. Two configurations are available:

- Direct connection to the PC using mSAS – PCI-E adapter
- Connection through PCI-Express switch (data concentrator) 8-to-1 using mSAS cables

Fully populated system can work with 512 measurement channels (using one x16 GEN3 PCI-Express slot in the embedded PC), working with 125 MHz sampling speed for each channel [6][7]. Figure 1 presents readout section of the GEM measurement system, handling 64 measurement channels. The backplane board is connected to the PCI-Express switch mounted in the embedded PC. Therefore, connecting 8 backplane boards to the PCI-Express switch gives a measurement system with 512 fast, analog input channels.

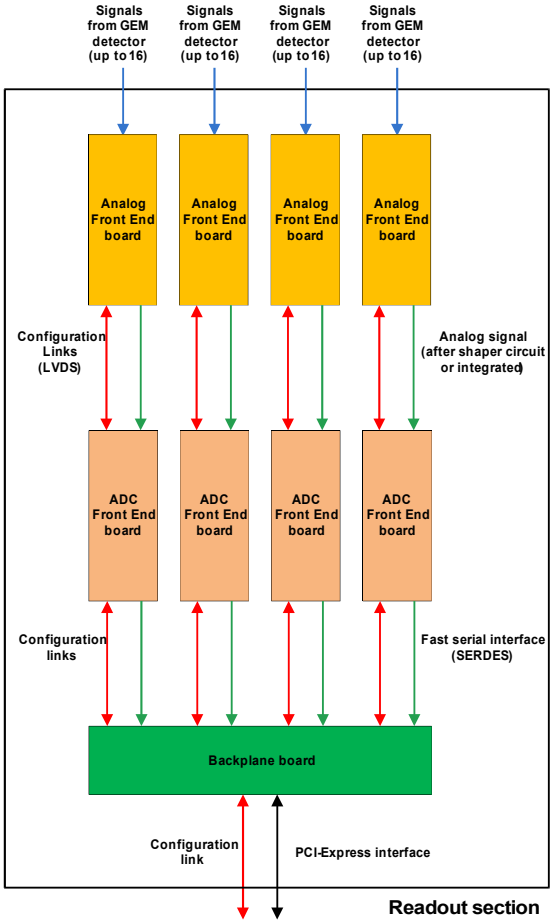

Figure 1 64-channels readout section of the GEM measurement system

4. FPGA firmware and implemented algorithms for fast data acquisition

FPGA firmware is the same for all of the FPGA units available on all the backplane boards. The firmware handles many different communication interfaces for configuration of the measurement system (e.g. ADCs interfaces, offset calibration circuits). Apart from the configuration part, several algorithms for the data processing were implemented [8]. Figure 2 presents main data-flow architecture for fast data acquisition, including:

- Long-time signal analyzers
- Fast signal recorder
- Fast digital charge integrator
- Test modes – digital pulse generator mode and counter mode

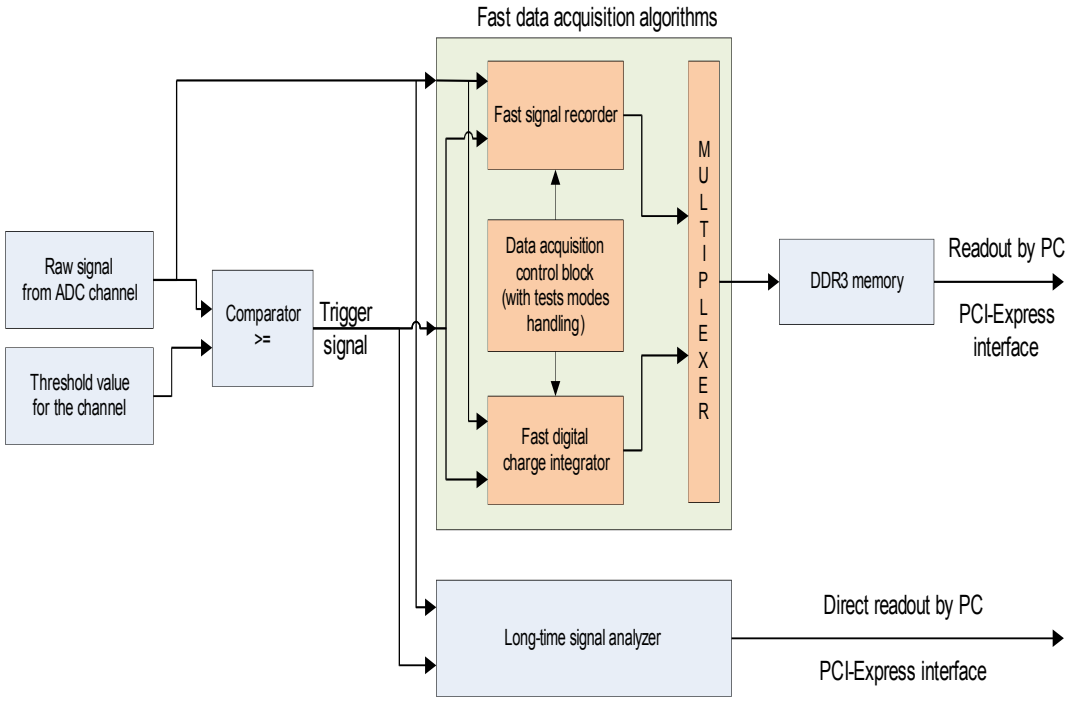

Figure 2 Fast data acquisition algorithms data-flow architecture implemented in the FPGAs

The output of the processing blocks can be connected to the serial streaming module, which automatically creates complex data structures with time markers. The data is then written in the DDR3 memory [9]. Then, the PC unit scans backplane boards for availability of the new data. Once detected, the data is downloaded to the PC unit and further, post-processing algorithms can be applied to the charge data.

4.1 Long-time signal analyzers

The analyzers blocks allow registration of the analog, raw signal from the ADCs. Analyzers work as digital oscilloscopes with configurable trigger position (e.g. post-trigger), trigger edge, threshold level of the trigger, etc.. Each FPGA has 64 analyzers implemented, one for each channel with 1024 sample memory. This mode is used for diagnostic purposes, e.g. can be used while adjusting the shaper circuits on the AFE boards. Analyzers works at 125 MHz sampling speed and stores the data in the FPGA embedded memory blocks.

Trigger section works as analog comparator, with user-defined threshold level for each channel. When trigger event occurs in one of the input channels, all signal analyzers start simultaneous data acquisition (global triggering system). Figure 3 presents a graph of a signals registered with long-time signal analyzers [7][8].

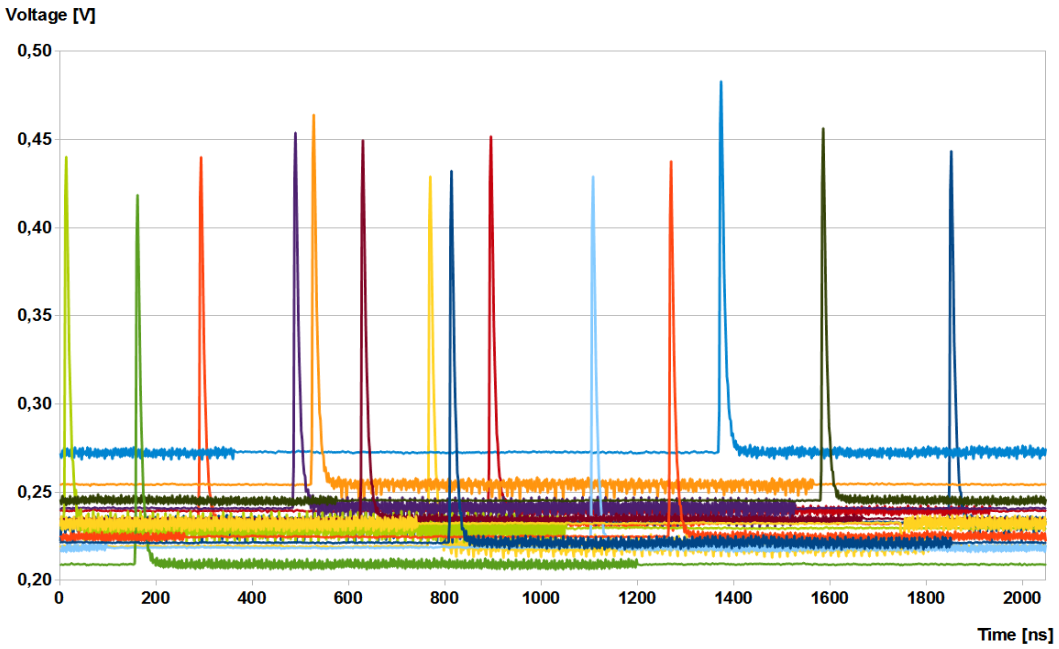

Figure 3 Raw analog signal acquired with the long-time signal analyzers (16 channels) [8]

4.2 Fast signal recorder

Fast signal recorders are available for each of the input channels (64 channels per backplane board). Signal is registered for 40 samples (one trigger event). All of the signal recorders start signal acquisition after receiving a trigger signal, in the same way as long-time signal analyzers. Sampling speed is also of 125 MHz. After raw signal registration, the data is transferred to the DDR3 memory module using a special data flow manager. This mode allows fast acquisition of large number of photons in a short time. After registering required number of samples, the embedded PC reads the saved data from the DDR3 memory and performs offline

processing – i.e. spectrum and photon position calculations. The data gathered contains also timestamp with event number for proper time placement of each signal.

4.3 Fast digital charge integrator

Fast digital charge integrator performs online charge calculation based on the raw ADC data. This significantly improves system throughput thanks to decreased computation time of the charge and reduced data amount transferred to the DDR3 memory module. After receiving the trigger pulse, the algorithm begins integration of the raw signal. Additionally implemented independent algorithm measures average value of the input signal before the pulse (i.e. noise/offset level). This constant value included in the charge value (integral) is subtracted from the measurement result at the end of the algorithm. Therefore no further computation of charge at post-processing stage is required. The charge data with timestamp information is stored in the DDR3 memory module.

An offline algorithm on the embedded PC can reconstruct position and spectrum's for user configurable number of energy bins. The post-processing is based on the data available in the DDR3 memory modules. Fast digital charge integrator, implemented in the system, works at 125 MHz sampling speed. Further details of the system are described in [6][7].

5. Measurement system control software

The system is controlled from the embedded PC using FCS (FPGA Configuration Software) [10]. The FCS software allows flexible configuration of large measurement systems, independently from the communication interface used in the system. In order to meet requirements of the complex measurement systems, FCS allows different parameters of the system to be user-configurable. The system can be automatically easily setup after boot and then configured to fit user needs with command line tools [11]. It also allows integration with graphical user interfaces.

In case of the GEM measurement system, PCI-Express [12][13] and USB interfaces for system configuration are used by FCS. At system boot-up stage, FCS configures all of the integrated circuits available, including: AFE, backplane and PCI data concentrator boards. Then, it does training of fast, serial links of ADCs. After the system setup is complete, user can configure it in different ways, including:

- Threshold levels for ADC channels
- Offset configuration
- Algorithms configuration (record length, test modes, data acquisition mode etc.)
- System status readout
- Download of measurement data from the DDR3 or FPGA memory

FCS is also used for system parameters diagnostics, including temperature and voltage measurements.

6. Summary

The work presented in the paper was based on Authors past experience in development of a measurements system for tokamak facilities [2][3]. In comparison with the previous system design, a significant rework was made. First of all, the whole structure has been divided into AFE, ADCFE, and backplane boards, resulting in a tree-like structure. Moreover, the vital parameters have been significantly improved. This refers especially to the increased sampling speed together with the charge integration time. Charge processing time is around 340ns, enabling work with high rates from the GEM detector. Due to dividing AFE into separate modules with radiation-hard integrated circuits and proper shielding, the system can work in environment characterized by strong electromagnetic fields and ionizing radiation.

The implemented algorithms allow fast and efficient signals processing. The control software FCS handles start-up of the system and provides interface for a user configuration. The measurement system can work with large number of readout channels from GEM detectors at high sampling speed.

ACKNOWLEDGEMENTS

This work has been carried out within the framework of the EUROfusion Consortium and has received funding from the Euratom research and training programme 2014-2018 under grant agreement No 633053. The views and opinions expressed herein do not necessarily reflect those of the European Commission.

This scientific work was partly supported by Polish Ministry of Science and Higher Education within the framework of the scientific financial resources in the year 2014 allocated for the realization of the international co-financed project.

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