PROCEEDINGS OF SCIENCE

An FPGA-Based Bolometer For The MAST-Upgrade Super-X Divertor

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A resistive bolometer system is being implemented for MAST-Upgrade to measure the total radiated power in the new Super-X divertor, with millisecond resolution, along 16 vertical and 16 horizontal lines of sight. The system uses a Xilinx Zynq-7000 series FPGA in the D-TACQ ACQ2106 carrier to perform real time data acquisition and signal processing. The FPGA enables AC-synchronous detection using high performance digital filtering to achieve a high signal-to-noise ratio, and will be able to output processed data with millisecond latency. Data from the multiple intersecting lines of sight will allow tomographic reconstruction of the total radiation emissivity. This information will facilitate studies of exhaust physics and optimisation of the new SXD performance.

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1. Introduction

The MAST-Upgrade (MAST-U) spherical tokamak device under construction at Culham Centre for Fusion Energy (CCFE) will feature a novel “Super-X” divertor (SXD) configuration which aims to reduce the heat load on the divertor target plates [1]. MAST-U will be the first tokamak to feature this new type of divertor, so thorough diagnosis of the SXD is essential.

It is important to measure the power radiated the divertor, as this quantifies the heat lost from the divertor plasma before reaching the divertor target plates. A large fraction of the power is radiated in the 6eV-6keV spectral range, by line emission from impurities and neutrals in the divertor region [2]. A means of measuring the power radiated in this spectral range, which is also capable of withstanding the environment of the MAST-U tokamak, is therefore required. A resistive bolometer is particularly suitable for this application [3].

In section 2, we describe the underlying principle behind the new bolometer diagnostic. Section 3 describes the AC synchronous detection method of improving the signal-to-noise. Section 4 describes the data acquisition hardware, and section 5 the procedure for calibrating the device. Section 6 presents results of some preliminary testing.

2. Bolometer principle

A bolometer measures total incident radiation, integrated over a wide range of wavelengths. A resistive bolometer measures resistance changes due to the temperature rise of a thin absorber foil. The sensors for MAST-U consist of a 4.5μm-thick Pt absorber deposited on a 1.5μm SiN membrane, with 1.2kΩ meander resistors deposited on the rear side of the membrane. The same type of sensor is to be used for the ITER bolometers [4]. A second such arrangement, shielded from the plasma, is connected in parallel to form a Wheatstone bridge. Radiation from the plasma heats the Pt absorber and hence the measurement meander resistors, which unbalances the Wheatstone bridge and produces an output voltage proportional to the temperature rise of the measurement resistors. From this, we can determine the power incident on the foil using the simple relation:

$$P_{bol} = S\left(u_d + \tau\frac{\mathrm{d}u_d}{\mathrm{d}t}\right) \tag{2.1}$$

S is the sensitivity (W/V) of the device, τ is the cooling time constant and u_d is the bridge output voltage. A more complete expression derived using AC circuit theory can be found in Ref. [5].

The measurement is of line-integrated power incident on the bolometer. The MAST-U system will have 16 sensors with horizontal views into the divertor chamber and 16 sensors with vertical views, as shown in Figure 1. It will therefore be possible to tomographically invert the line of sight measurements to recover the emission profile inside the divertor chamber.

3. AC synchronous detection

Care must be taken to reduce pick-up from the noisy electromagnetic environment of the tokamak. To achieve this we employ AC synchronous detection: we drive the bridge with an AC sine wave voltage, and detect only the component of the bridge output signal at the same frequency.

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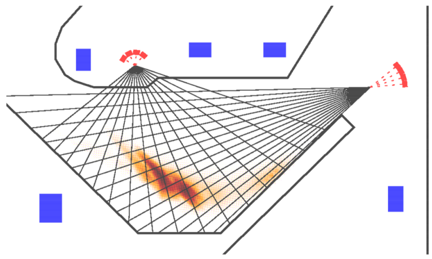

Figure 1: The lines of sight of the divertor bolometer sensors [6]

This offers advantages over DC excitation/detection, such as eliminating 1/f noise and allowing us to make measurements away from large sources of spectral noise. We expect to use a frequency of 20kHz and amplitude 20V.

All the required signal processing is performed digitally, allowing far greater filter performance to be achieved than traditional analogue filtering. The bridge output voltage is digitised at 1MSPS using 16-bit ADCs. Each sample is then multiplied by digital sine and cosine waves at the same frequency as the excitation voltage, to produce “in-phase” and “quadrature-phase” components. These two components are then passed through a digital finite impulse response (FIR) low pass filter which filters out the drive frequency, leaving only the demodulated signals I and Q. These are mathematically the real (I) and imaginary (Q) parts of a complex signal, so a transformation from Cartesian to polar representation is performed using the CORDIC algorithm [7]. This process automatically compensates for any phase delay in the system, so no manual adjustment of the electronics is required. The resulting amplitude u_d is used to calculate P_{bol} in equation 2.1.

The digital filtering approach allows for complex filters to be designed. It is possible to design a filter that will perform the demodulation, differentiate the signal and add the signal to its time derivative. This means that the bridge output voltage can be directly processed into a measure of the incident power using a single digital filter, allowing for low-latency (of order ms) output of power measurements.

4. Electronics

The bolometer sensors described in section 2 are assembled by IPT-Albrecht GmbH[1]. These are connected to the data-acquisition and signal processing electronics, some 20m away from the vacuum vessel, using Cat-7 cables, which consist of four individually screened twisted pairs of cables. Each Cat-7 cable is connected to two bolometer bridges. Two of the twisted pairs carry a differential signal to drive the bridges, and two carry the differential bridge response signals. The screening will minimise cross talk between the signals, as well as reducing external noise.

The signal is digitised and processed using an FPGA-based acquisition unit. The unit comprises a D-TACQ[2] ACQ2106 6-site carrier, populated with 4 BOLO8 ELF/FMC modules. The BOLO8 units, developed by D-TACQ and CCFE, contain one 16-bit, 1MSPS digital-to-analogue

[1] http://www.ipt-albrecht.de/eng/1_2_1_bolometer_system.html

[2] http://www.d-tacq.co.uk

converter (DAC) to produce the voltage to drive eight bridges, and eight 16-bit, 1MSPS analogue-to-digital converters (ADCs) to digitise the bridge response voltages. Eight additional slower (∼1kSPS) DACs allow the bridge to be biased with a low frequency square wave voltage for calibration, and current-measuring ADCs measure the current flowing through the bridge during this process. The calibration process is described in detail in section 5. The main DAC can provide up to $40V_{pp}$ drive at up to 100kHz.

The ACQ2106 is an intelligent, networked module carrier. It features a Xilinx Zynq 7Z030 FPGA, comprising a dual-core ARM A9 processor and 7-series FPGA programmable logic, on the same chip. The chip's IO is connected to 6 ELF/ULPC sites (a D-TACQ extension of the VITA-57 FMC standard), of which four are populated with BOLO8 modules in the 32-channel MAST-U system. Connectivity is provided via Gigabit Ethernet to the ARM processor, which runs a Linux OS, and SFP+ fibre optic connectors directly to the programmable logic of the FPGA for real-time communications. The entire system fits in a 1U, 19" rack.

The FPGA programmable logic controls the DACs and ADCs, by producing the 20kHz AC excitation wave and the calibration bias voltage, and digitising the bridge output voltage and current. The digitised data is processed on the FPGA using built-in DSP resources to implement the FIR filters. These filters feature reloadable coefficients, allowing the frequency response to be changed between shots, with no reboot of the device required. This gives flexibility in deciding upon an acceptable trade-off between noise levels and time response of the system.

The processed data is transferred to DDR3 memory, where it can be read by the CPU. The data is then read from the device post-shot using the FTP protocol. A series of registers on the FPGA to control operation can be accessed by the processor. The processor runs an HTTP server allowing remote configuration and control of the device over the network.

5. Calibration

As with previous bolometer systems, calibration is performed by ohmically heating the two sensor resistors without heating the reference resistors [3, 5]. The MAST-U system uses a DC voltage for ohmic heating and an AC voltage to drive the bridge, employing synchronous detection during calibration. In this scenario, the secondary "offset" DACs apply a DC voltage, and the main DAC applies a sinusoidal voltage, but with a DC offset at the same voltage as the offset DACs. The result of this is that DC current flows through the sensor resistors but not the reference resistors, whilst AC current flows through all 4 resistors. Figure 2 shows this schematically.

The demodulated signal is recorded, and from the heating and cooling curves the sensitivity, cooling time and bridge offset can be measured by performing least-squares fitting to simple theoretical heating and cooling functions:

$$u_{d,h}(t) = C_1\left(1 - e^{-(t-t_0)/\tau}\right) + C_2, \quad u_{d,c}(t) = C_1 e^{-(t-t_1)/\tau} + C_2 \tag{5.1}$$

C_1 is indirectly a measure of the sensitivity, τ is the cooling time (to be used in equation 2.1) and C_2 measures the zero-incident-power bridge amplitude, which can then be corrected for. t_0 and t_1 are the start times of the heating and cooling pulses respectively, and are determined from when the measured bias voltage is (non-)zero.

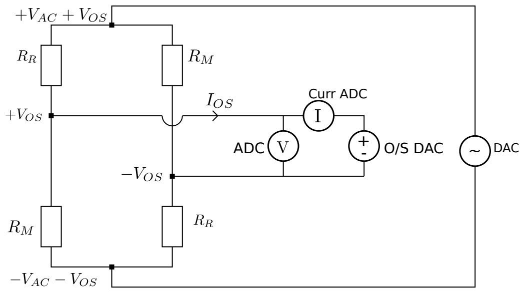

Figure 2: Schematic of the calibration procedure.

During the calibration, both the raw and the modulated bridge response are low-pass filtered. This means that as well as the synchronous detection signal, we have a measure of the bias voltage applied to the bridge, V_{OS}. The applied DC ohmic heating power is then $V_{OS} \times I_{OS}$. Dividing this by C_1 from equation 5.1 provides a measure of the sensitivity S of the sensors.

This calibration process is very flexible. We can set the amount of time the bridge is ohmically heated and left to cool, until the heating and cooling curves reach steady state. We can adjust the amount of ohmic heating by varying the voltage applied by the offset DAC so that the power matches the expected power levels from the plasma, which is important as some non-linearity was observed at higher power loadings during testing. By running the AC drive voltage at a similar amplitude in calibration and in main operation, we can calibrate the sensors in realistic conditions.

The calibration procedure can be performed before each shot. The fitting process is done in software on the ARM CPU immediately after the calibration procedure, and the resulting parameters can be used to design a deconvolution filter for reconstructing incident power. This filter can then be loaded into the FPGA, ready for the shot. This means we can have a recently-calibrated real-time power output for every shot, if desired.

6. Preliminary testing

While the hardware (ACQ2106, BOLO8 and sensors) for the system has been finalised, the software and FPGA firmware is under active development. To test the system operates as expected, we have tested with an older gold-foil sensor, described in [3], as a Pt one was not yet available.

Tests were performed in a vacuum chamber at 5×10^{-5}mBar, with the sensors illuminated using a 3mW, 660nm wavelength laser, with a 5Hz square waveform. The sensor was excited with a 20kHz sine wave, which was digitised and then filtered in software. Using the fit parameters from a calibration run and equation 2.1, the incident power from the laser was reconstructed from the bridge amplitude. The measured cooling time was 150ms, in good agreement with previous measurements of this type of sensor in vacuum. Figure 3 shows the results. The plot uses the cooling time and sensitivity to provide an absolute power measurement. The 5 Hz fluctuation, even at very small signal levels (due to the high reflectivity of gold at 660nm), can be clearly seen.

7. Summary and conclusions

A new bolometer system is being developed for MAST-Upgrade, to measure the power radi-

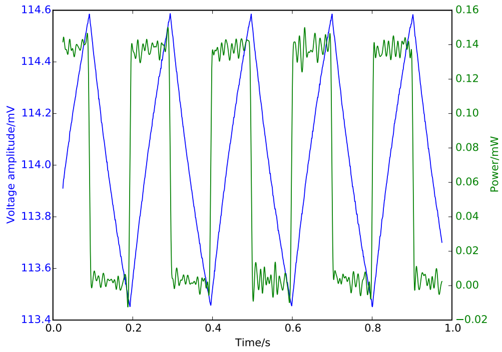

Figure 3: Measured bridge amplitude and reconstructed power, for a 5 Hz pulsed laser

ated in the new Super-X divertor. It will make measurements along 16 horizontal and 16 vertical lines of sight, allowing for tomographic reconstruction of the emission profile inside the divertor chamber. The sensors themselves are of the same design as those proposed for ITER, using a Pt absorber on a SiN substrate. The data acquisition electronics uses FPGA technology to drive the sensors and perform synchronous detection of the resulting signal. This allows the use of high performance digital filtering, and low latency output for real-time control applications.

An automated calibration procedure uses DACs and ADCs driven by the FPGA to perform calibrations in realistic usage scenarios, with no hardware switches required. Whilst still under active development, preliminary tests with an older sensor design in a vacuum chamber in the lab have shown that the system is able to comfortably measure sub-milliwatt levels of power when illuminated by a modulated laser beam.

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