

## Development of a SiPM Camera for a Schwarzschild-Couder Cherenkov Telescope for the Cherenkov Telescope Array

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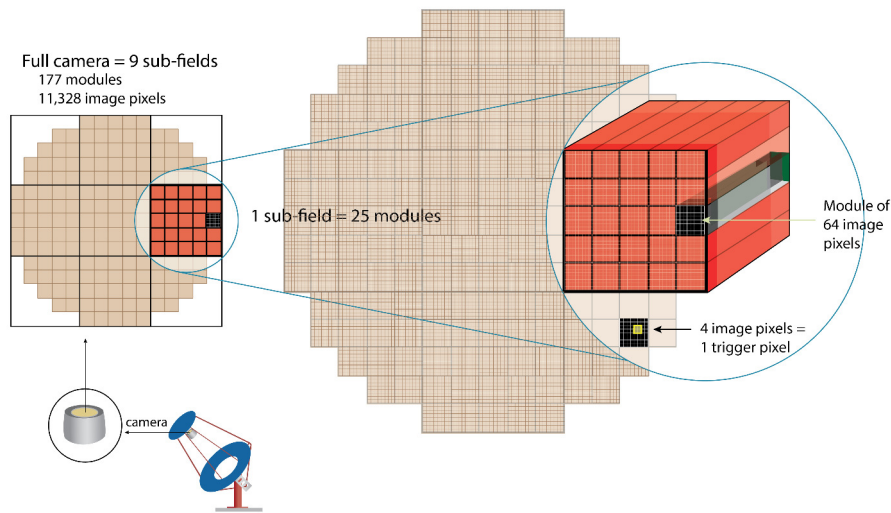
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We present the development of a novel 11328 pixel silicon photomultiplier (SiPM) camera for use with a ground-based Cherenkov telescope with Schwarzschild-Couder optics as a possible medium-sized telescope for the Cherenkov Telescope Array (CTA). The finely pixelated camera samples air-shower images with more than twice the optical resolution of cameras that are used in current Cherenkov telescopes. Advantages of the higher resolution will be a better event reconstruction yielding improved background suppression and angular resolution of the reconstructed gamma-ray events, which is crucial in morphology studies of, for example, Galactic particle accelerators and the search for gamma-ray halos around extragalactic sources. Packing such a large number of pixels into an area of only half a square meter and having a fast readout directly attached to the back of the sensors is a challenging task. For the prototype camera development, SiPMs from Hamamatsu with through silicon via (TSV) technology are used. We give a status report of the camera design and highlight a number of technological advancements that made this development possible.

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**Figure 1:** Conceptual layout of the camera focal plane

## 1. Introduction

Exploring the universe in the very-high energy (VHE) gamma-ray band has resulted in a plethora of stunning discoveries and many paradigm shifts in past years. From observations with the latest generation of Cherenkov telescope arrays it has come clear that our view of the VHE universe is limited by the sensitivity of existing instruments. These limitations spurred the VHE community to pursue the construction of the Cherenkov Telescope Array (CTA) with the goal to deliver a VHE instrument with one-order-of-magnitude improved sensitivity. A detailed description of CTA and its science goals can be found in [1].

The CTA group in the United States has proposed an innovative, two-mirror Schwarzschild-Couder telescope (SCT) [2] array for CTA. The demagnifying SCT optical design provides a dramatic reduction in the plate scale compared to currently used telescopes, enabling a camera based on modern technology including self-triggering custom ASICs with high channel density as well as SiPMs. We have designed a low-cost camera based on SiPM photon detectors, the TARGET custom analog pipeline ASICs, a backplane to merge a large number of channels into a single high-speed FPGA for the pattern trigger, and another FPGA for data acquisition.

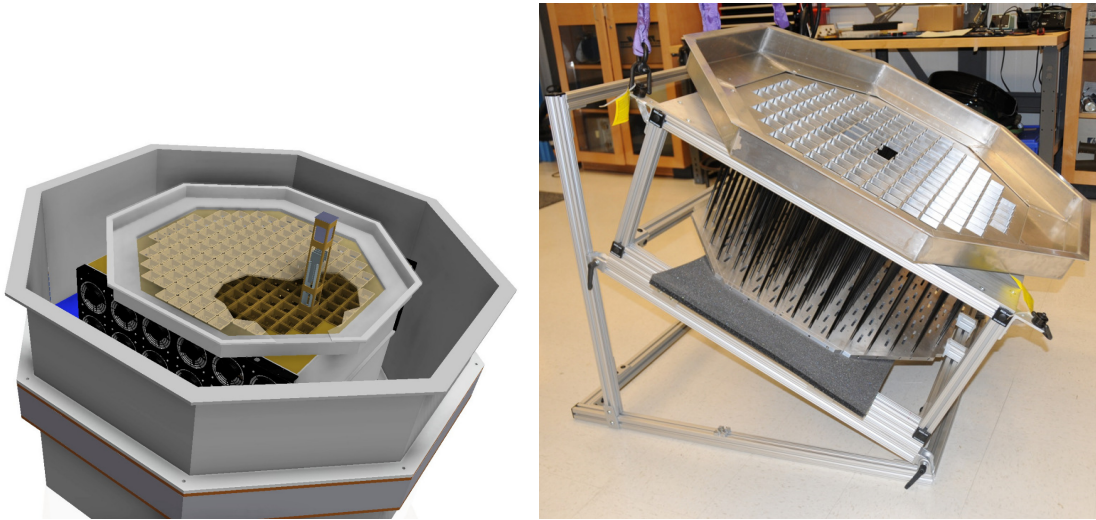
Section 2 gives an overview of the SCT camera. Section 3 describes the photon detectors. How they are being integrated into the camera is being detailed in Section 4. In Section 5, a description of the front-end electronics and data acquisition is given. The paper closes with an outlook of the next steps in camera production in Section 6.

## 2. Layout of the camera

The three main design drivers of the camera are: (1) A hierarchical architecture that is easily serviceable and contains few failure points in the form of cable interconnects, (2) precise mechan-

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**Figure 2:** The left image is a model of the camera and illustrates how one camera module is inserted into the camera. The image on the right shows parts of the fabricated inner camera. Shown are the front lattice and the focal plane enclosure mounted on top of the front lattice. Behind the front lattice can be seen the carbon fibre rods of the drawer structure and the bulk plate.

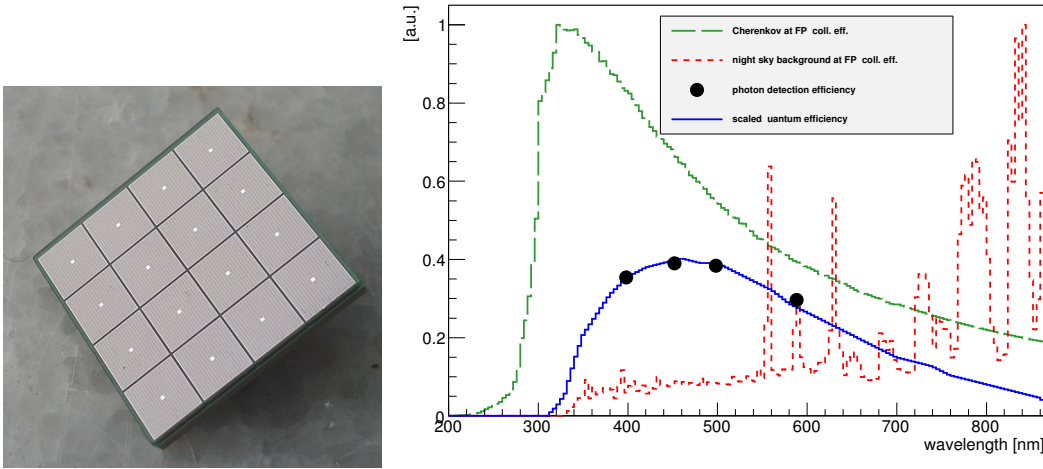
ical registry and adjustment of the SiPMs and (3) thermal/environmental control to remove waste heat from the densely packed camera electronics while providing temperature regulation for the photosensors.

The camera consists of an inner camera and an outer enclosure. The outer enclosure acts as a shield from the elements and serves as interface to the telescope structure. The inner camera hosts the photosensors, front-end electronics, digitization electronics, level-0 (L0) trigger, and back-plane electronics that provide the pattern trigger and data acquisition hardware.

The camera architecture is subdivided into nine subfields or sectors (see Figure 1). A fully loaded sector has 25 modules that are inserted from the front into the drawer-like structure of the inner camera (see left panel in Figure 2). A module consists of 64 imaging pixels in an eight-by-eight configuration. The size of one pixel is  $6.5 \times 6.5 \text{ mm}^2$ , which corresponds to an angular size of  $0.067^\circ$  in the sky. Integrated in each module is the complete readout electronics (see Figure 4). A fully equipped camera has 177 modules with a total of 11,328 pixels.

The SC optics requires positional uncertainties of the focal plane along the optical axis that are less than  $200 \mu\text{m}$ . The primary positional reference for the focal plane is provided by a  $3/4$ " machined aluminum lattice plate (see right panel in Figure 2) that is mounted to a rack of thermally-stable carbon-fiber supports. The modules slide into the front lattice and ultimately register on its front surface through a Delrin collar. Relative to the front lattice, the photon detectors of each module are adjusted to a different height to approximate the ideal curvature of the SC optics. The modules are locked in place by a pulling mechanism that acts on the module from the back of the camera. Deformations between the front lattice and back of the camera due to temperature changes are compensated by dividing the module frame into two separated pieces that can move relative to each other.

Dissipating the about 3 kW of heat produced by the camera electronics is accomplished with



**Figure 3:** Left: One tile of the Hamamatsu S12642-0404PA-50(X) used in the SCT prototype. Right: Photon detection efficiency of the Hamamatsu S12642-0404PA-50(X) when operating at 3 V overvoltage (black) and quantum efficiency (blue) scaled to match the photon detection efficiency (PDE). For the efficiency curves, the absolute efficiency can be read off the labeled y-axis. The green curve gives the Cherenkov spectrum in the focal plane and the red curve the night sky background spectrum in the focal plane. Integrating over both spectra the S12642 detects 21% of the Cherenkov photons that arrive in the focal plane and 14% of the night sky background when operated at 3 V overvoltage.

forced cooled air. Thermally insulated from the camera electronics are the photon detectors that are encapsulated in the so-called focalplane box and isolated from the environment with a UV transparent acrylic window.

### 3. Photon detector used in the prototype SCT

A large number of silicon photomultipliers (SiPMs) have been evaluated from different vendors [3] and the Hamamatsu S12642-0404PA-50(X) was selected as the photon detector for the SCT prototype. The S12642 is a tile of 16 SiPMs, each  $3 \times 3 \text{ mm}^2$  in size (see Figure 3). The microcell pitch of the SiPMs is  $50 \mu\text{m}$ . In the prototype SCT, groups of 4 SiPMs are connected in parallel to form one  $6 \times 6 \text{ mm}^2$  pixel in the readout. One main criterion to choose the S12642 over other devices is its use of the through silicon via (TSV) technology, which minimizes dead-space at the boundary of the pixel.

Extensive tests have been performed on individual tiles, as well as basic functionality tests on 415 tiles that have been purchased for the 25 modules of the prototype SCT. Figure 3 shows the photon detection efficiency of one SiPM measured at 3 V overvoltage. Overlaid over the photon detection efficiency (PDE) measurements is the quantum efficiency (QE) curve measured by Hamamatsu after scaling the QE curve to match the PDE measurements.

Optical crosstalk is fairly high with 50% at an overvoltage of 3 V (5% above breakdown), which raises the trigger threshold of the SCT. The spectral response of the S12642 is such that 21% of the Cherenkov photons are detected and 14% of the unwanted night sky background photons. Newer devices that have become available from several vendors lately have much lower optical

crosstalk and a spectral response that is more favorable for detecting Cherenkov light and will be considered in the future [4].

#### 4. Mechanical integration and temperature stabilization of the SiPMs

The photon detectors for one camera module are divided into four quadrants. Each quadrant has four SiPM tiles with 16 image pixels. Four quadrants are assembled into a focal-plane module, which in turn is attached to the top of a camera module. The sensors are thermally insulated from the back of the camera by a plastic base plate and one inch thick insulation foam (densified Solemide from Evonik). Active cooling of the sensors is accomplished with a thermoelectric element that is thermally coupled to a copper post. Temperature feedback is provided by a thermistor that is mounted on the back side of each quadrant. When the telescope is in operation, the temperature will be stabilized to a temperature a few degrees below the equilibrium temperature of the focal plane box to minimize the required cooling power. See [5] for further details on the photon detector integration.

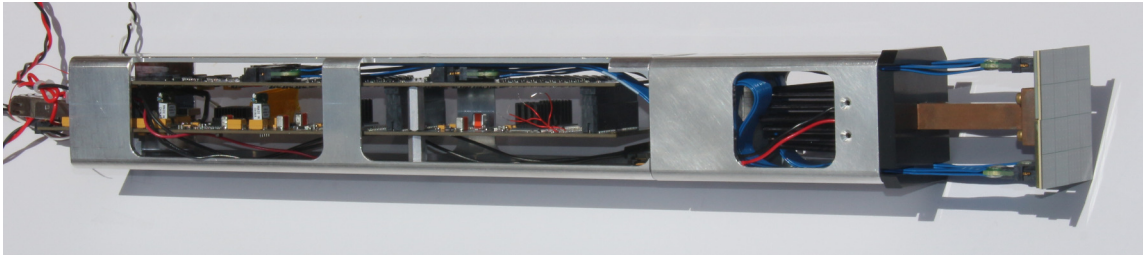
#### 5. Readout electronics

The complete readout electronics is integrated inside the camera. Front-end signal processing, signal digitization, and the first level trigger take place inside the camera modules. The electronics inside the modules also includes ancillary systems such as current monitors for tracking bright stars, high-voltage distribution to the photon detectors, and temperature control for the photon detectors.

Communication between the camera modules and the camera servers, distribution of trigger signals, power distribution, et cetera are managed by camera backplanes, one for each camera sector. The data from the nine camera sector backplanes are merged and delivered to a level-2 event-building system (the SCT Camera Server) using standard high-speed communication protocols (including 10 Gb/s-Ethernet switches). Trigger and time synchronization signals from the backplanes are relayed by the distributed array trigger electronics. The main camera electronic components are described in the following.

##### 5.1 Preamplifier

The raw signals from the S12642 MPPCs exhibit a fast rising edge and a slow decaying tail ( $> 100$  ns) due to the large terminal capacitance ( $> 1$  nF) of the four, connected in parallel SiPMs to form one pixel. For optimum signal separation from fluctuations in the night-sky-background, a full width at half maximum (FWHM) of 10 ns or less is desirable for the SiPM signals. A shorter pulse in the readout is achieved by differentiating the signals with a high-pass filter with pole zero cancellation in between the two stages of the preamplifier (see [5] for further details). The resulting FWHM of 10 ns of the output signal is dominated by the limited bandwidth of the Analog Devices AD8014 chip that is used to amplify the signal. While a higher bandwidth would be advantageous, the two stage amplifier consumes only 10 mW, which amounts to  $\sim 100$  W of waste heat for the 11,328 pixel camera. The dynamic range of the preamplifier is 250 photoelectrons. Further developments of preamplifier concepts that aim at faster signals and less power consumption are ongoing and will be employed in the final SCT array. The amplitude of a single photoelectron signal at the



**Figure 4:** Picture of one fully assembled camera module used for prototype testing. See text for details.

output of the amplifier is 4 mV at a  $50\ \Omega$  impedance for an operating voltage of the SiPM that is 3 V above breakdown.

## 5.2 Signal digitization and first level trigger

After signal amplification and shaping, digitization and the level-1 trigger are integrated in an application-specific integrated circuit (ASIC) TARGET [6]. The prototype SCT uses the 7<sup>th</sup> generation TARGET (TARGET 7). A TARGET chip has 16 input channels, each equipped with a 16,384 cell switched capacitor array (SCA) providing a buffer depth of  $16.384\ \mu\text{s}$  at a sampling rate of 1 GSa/s. When a readout command is issued, an on-chip 10-bit (effective) Wilkinson analog-to-digital converter digitizes the sampled voltage levels stored in the SCA. TARGET 7 has a dynamic range of 1.9 V. Figure 5 shows the charge resolution of the TARGET-7 chip.

In parallel to signal sampling and digitization, TARGET also performs the first stage of the trigger by forming the analog sum of four adjacent image pixels and discriminating the summed signal. A trigger efficiency curve as a function of input pulse amplitude evaluated in a bench test using signals from a function generator is shown in Figure 5. We note that the minimum stable trigger threshold during normal operations for TARGET 7 is 50 mV and the typical trigger noise is 10–15 mV due to coupling between the sampling and triggering circuits of the ASIC. A newer generation of TARGET ASICs, currently undergoing testing, is expected to circumvent the coupling by separating the sampling/digitization and triggering into two separate ASICs, TARGET C and CCTV. Based on the experience with previous TARGET generations we expect to achieve a minimum trigger threshold of 4.5 mV and a trigger noise of  $\sim 0.5$  mV. More information about TARGET and details about the performance of TARGET 7 can be found in [7].

## 5.3 Camera backplane

The (up to) 400 trigger signals in each camera subfield are presented to the level-1 (L1) trigger FPGA on the backplane where the relative timing is adjusted to ns precision and patterns of adjacent hits are located with an essentially dead-time-free pipelined architecture with a coincidence resolving time programmable down to 4 ns. The array trigger and backplane electronics provide phase-locking of the 125 MHz clock through the entire camera electronics to the individual TARGET ASICs, with synchronization good to 1 ns.

The level-2 (L2) trigger collects L1 triggers from the backplane and provides other timing signals required for event synchronization, event tagging, clock synchronization, and synchronous resets. Each backplane takes the 1600 1-GSa/s waveform data streams from 25 camera modules and

combines them in a data acquisition FPGA, where buffering and event building (and, optionally, zero suppression, trace integration, and/or data compression) are performed before outputting the data on a pair of 10 Gb/s Ethernet links. Data are merged with a high-speed switch so that the backplanes can serve data and command telemetry to a number of client computers. One client is the Camera Server computer, which includes the level-2 event builder (combining all data from the multiple backplanes) and an interface to the central DAQ.

The data acquisition electronics are designed to handle a single telescope trigger rate up to 10 kHz. However, a suppression factor of at least 4 is provided by the distributed trigger array system, leading to an effective single-telescope trigger rate of 2.5 kHz. For a full-camera readout size of 1.42 MB (125 bytes/pixel for 11,328 pixels) this trigger rate translates into a raw data rate of 3.54 GB/s (28.3 Gb/s) per telescope. If additional reduction is needed, the backplane FPGAs can perform data compression, zero suppression, and/or waveform integration prior to transmission.

#### 5.4 Distributed Intelligent Array Trigger

The Distributed Intelligent Array Trigger (DIAT) assumes responsibility for the level-2 (L2) trigger event time stamps (camera trigger), and synchronized clock distribution in the camera with nanosecond precision.

DIAT will enable computation of low-order moments of the shower image, which are subsequently sent to the DIAT modules of neighbouring SCTs. In addition to a more traditional telescope multiplicity trigger, application of a hardware-level algorithm that combines image-moment data from nearby SCTs to compute a real-time localized level-3 (L3) trigger decision is also an option [8]. Both allow spurious L2 triggers at a single telescope to be identified and vetoed before camera readout, ameliorating the data-transfer rates for the SCT subarray.

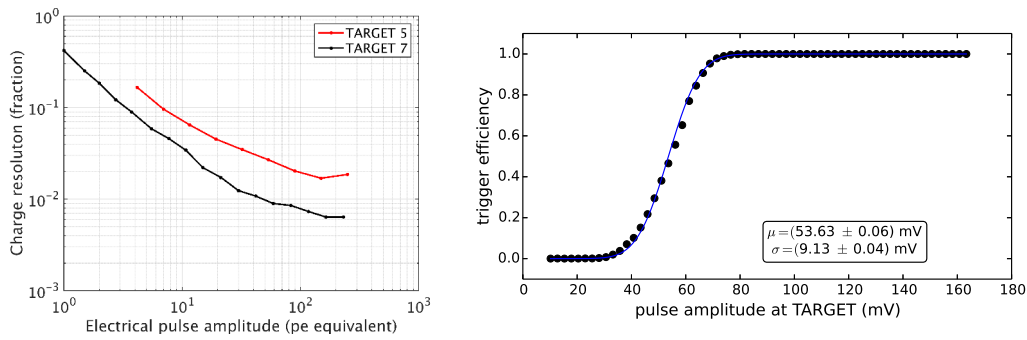
A prototypical trigger demonstrator has been fabricated, which will receive and temporarily store timestamped trigger messages from the local backplane modules. Those messages can be accessed and analyzed asynchronously using slow-control software. It will use a special calibration mode to compute the signal propagation delays that can be used to calibrate the embedded clock signal that it will transmit to each local backplane.

## 6. Outlook

The construction of the camera for the prototype SCT is ongoing. For the prototype SCT one camera sector will be equipped with camera modules. The photon detectors have been tested and are now being assembled into focal plane modules. In parallel, prototypes of the front-end electronic boards have been tested and production of boards for 29 camera modules is ongoing. The fabrication of the camera mechanics, the backplane for one sector and the DIAT are also underway. After integration and final testing of the camera is complete, the camera will be shipped to the VERITAS site for assembly onto the SCT, which is expected to take place in Fall 2015.

## 7. Acknowledgements

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**Figure 5:** Performance of TARGET 7 evaluated using signals from a function generator. Left: charge resolution as a function of input charge (including the contribution from the ASIC only) assuming the 4 mV/p.e. pulse amplitude expected in the prototype SCT camera. Right: demonstration of the minimum stable trigger threshold achievable by TARGET 7 during normal operations. The plot shows the trigger efficiency as a function of input pulse amplitude with best fit Gaussian error function: the inset panel gives the Gaussian mean (threshold) and standard deviation (noise).

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