PROCEEDINGS OF SCIENCE

LHCb Upgrade: Upstream Tracker

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The upgraded LHCb detector will run at an instantaneous luminosity of 2×10^{33} cm^{-2} s^{-1}, five times higher than in the current configuration, and will have a full 40 MHz readout. In order to cope with these higher instantaneous rates, the tracking detector upstream of the LHCb dipole magnet, called Tracker Turicensis (TT), will be replaced by the Upstream Tracker (UT). The conceptual design of the UT and the current status of the R&D are presented here.

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1. Motivations

The Upstream Tracker (UT) [1] will replace the Tracker Turicensis (TT) [2]. It will play an important role in the High-Level Trigger (HLT) tracking, providing a fast estimate of the momentum of charged particles and allowing rejection of low-momentum tracks, thus speeding up the track reconstruction algorithm by a factor of three compared to the current tracking strategy [3, 4]. Compared to the TT, it will guarantee a higher trigger efficiency, mostly due to its improved acceptance coverage at small polar angles. This will be achieved by reducing the beampipe clearance and insulating material and designing the innermost sensors to have a circular opening around the beampipe. The UT will also have a finer granularity, improved radiation hardness, and new front-end electronics that will allow a full 40 MHz readout.

2. Irradiation constraints

The UT is expected to withstand the radiation damage due to an integrated luminosity of 50 fb^{-1}. The resulting fluence and radiation dose profiles, obtained by a FLUKA simulation [5, 6], are shown in Fig. 1 as a function of the y-coordinate (that is, the vertical coordinate), for a slice of the detector that is positioned at $x = 0$. The x-coordinate defines, together with the y-coordinate, the plane transverse to the beam, with $x = 0$ corresponding to the center of the beampipe.

The components close to the beampipe will be irradiated with up to 40 MRad, including a safety factor of 4, while the part of the electronics located further from the beampipe, at a distance of approximately 70 cm, will be irradiated with up to 100 kRad, including a safety factor of 2.

The sensors will be kept at or below a temperature of about -5°C, in order to mitigate the effects of radiation damage and limit the bias voltage to the range between 300 and 500 V after irradiation, as demonstrated by studies on prototypes with similar sensors.

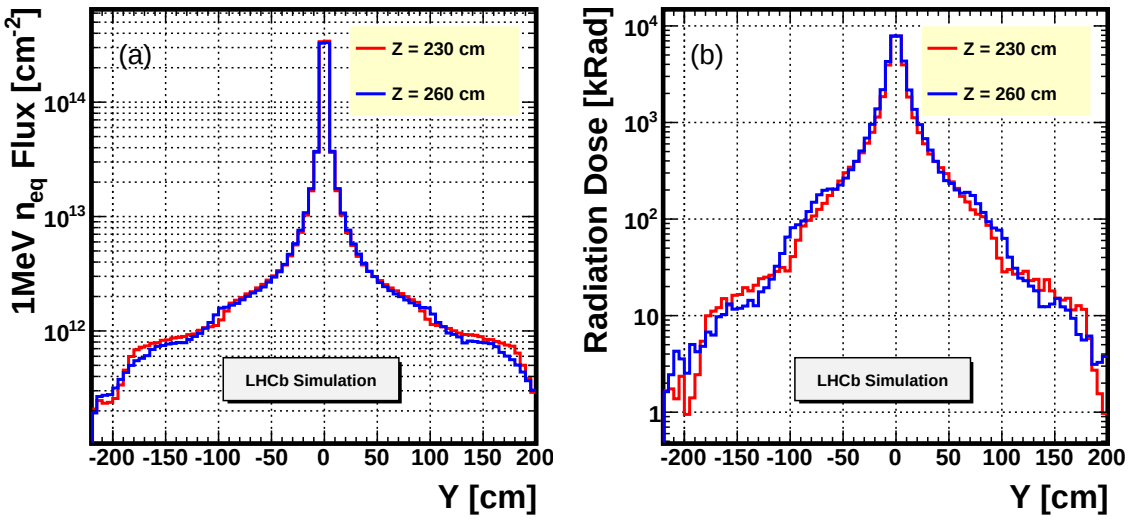

Figure 1: Fluence profile (left) and radiation dose profile (right) as a function of the y-coordinate, for a slice of the detector that is positioned at $x = 0$. The red and blue curves refers to the z-coordinates of the two stations of the UT.

3. Geometry

The UT will consist of four detection planes, divided into two stations of two planes each, as is schematically shown in Fig. 2 (left). The four planes will be put inside a common light tight box that is flushed with nitrogen or dry air in order to avoid condensation on cold surfaces and that also acts as a Faraday cage.

Type	Pitch (μm)	Nominal length (mm)	Strips	ASICs
Outermost	190	97.28	512	4
Intermediate	95	97.28	1024	8
Innermost	95	48.64	1024	8

Table 1: Properties of the different types of sensors.

Each plane will be equipped with single-sided silicon microstrip sensors, having different strip pitches and lengths according to the expected occupancy and read out by 4 or 8 ASICs, depending on the number of strips, as summarised in Tab. 1. Strips will run vertically on the first and last plane and will be tilted of $\pm 5^\circ$ with respect to the vertical direction on the second and third plane.

The functional unit of each plane will be the "stave", shown in Fig. 2 (right) viewed from the front and in Fig. 3 viewed from the side. There will be 68 staves in total. Staves within a plane will be staggered in z in order to provide overlap in x and ensure complete acceptance coverage.

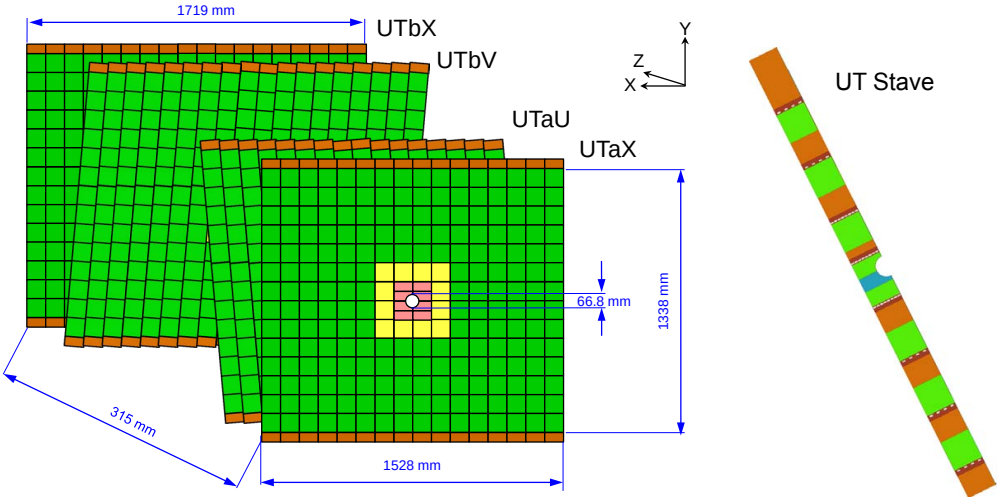

Figure 2: Arrangement of the four planes of the UT. Outermost, intermediate, and innermost sensors are shown in green, yellow, and red, respectively (left). Layout of the stave. Sensors are shown in green, flex cables are shown in orange, and ASICs are shown in yellow (right). Sensors, flex cables, and ASICs are also on the other side of the stave.

Each stave will have a width of 10 cm and a length of 134 cm. It will consist of 14 or 16 sensors (depending on the distance from the beampipe) mounted on both faces and overlapping in y. Data, control signals, and power will be carried by flex cables running on both faces of the stave from the top and bottom to the center. Signals will be processed close to the sensor in a

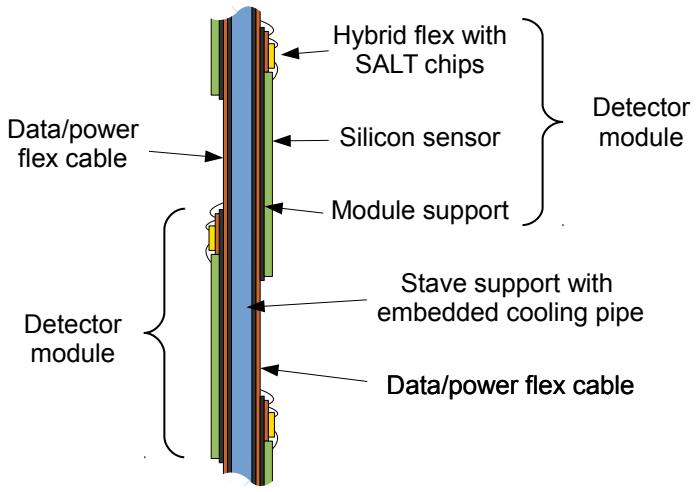

Figure 3: Side view of the stave, showing two detector modules, one on each side of the stave.

newly developed front-end ASIC called SALT [1]. Each ASIC will have 128 channels of front-end amplifiers and will reduce the data volume by performing digitisation, zero suppression, and serialisation output via up to 5 e-ports at a data transmission speed of 320 MBit/s each [7]. Due to the power dissipation in the ASICs, active cooling will be needed inside each stave. A bi-phase CO_2 cooling system with thin cooling pipes embedded in the staves will be used to minimize the impact on the material budget. The UT will have shorter strips than the TT. Good signal over noise ratio will hence be obtained with thinner sensors, 250 μm instead of 500 μm thick (as in the TT). The increase in the material budget due to the active cooling will therefore be neutralized by a corresponding decrease due to the thinner sensors, thus leading to a total material budget comparable to that of the TT.

From the mechanical point of view, the stave will consist of a central support/cooling layer, made of Carbon Fiber Reinforced Polymer (CFRP) facing sheets surrounding a foam core interior in which the cooling pipes are embedded. This central layer of the stave will support the flex cables and detector modules with sensors and ASICs. The detector modules will be fixed on the stave in a way that will allow single modules to be removed in case repairs will be needed.

4. Cooling

The cooling system will keep the temperature of the sensors below -5°C, to suppress reverse annealing, reduce leakage current, and prevent thermal runaway in the presence of radiation damage. The maximum temperature difference across the sensor will be kept below 5°C to limit the mechanical stress. The sensors will be kept cold also during shutdown periods, thus minimising reverse annealing. A bi-phase CO_2 cooling system, using thin-walled titanium cooling tubes embedded in the stave, is being designed. A backup solution using stainless steel instead of titanium is also under investigation. The heat load will be mainly due to the ASICs, which will dissipate nearly 0.77 W/chip. Therefore, their position is taken into account when designing the path of the cooling tubes.

Two designs are currently being investigated. The baseline solution, called "snake pipe", will consist of cooling tubes running directly underneath each row of ASICs, as shown in Fig. 4 (left), thus providing the best thermal performance. The potentially critical aspects of this design (for example, the bending radius of the tubes and the pressure drop) will be validated with full stave prototypes. A backup solution, called "parallel pipe" and consisting of straight cooling tubes running along the stave, combined with heat spreaders and thermal vias to improve the heat transfer from the ASICs, is also under investigation and is shown in Fig. 4 (right).

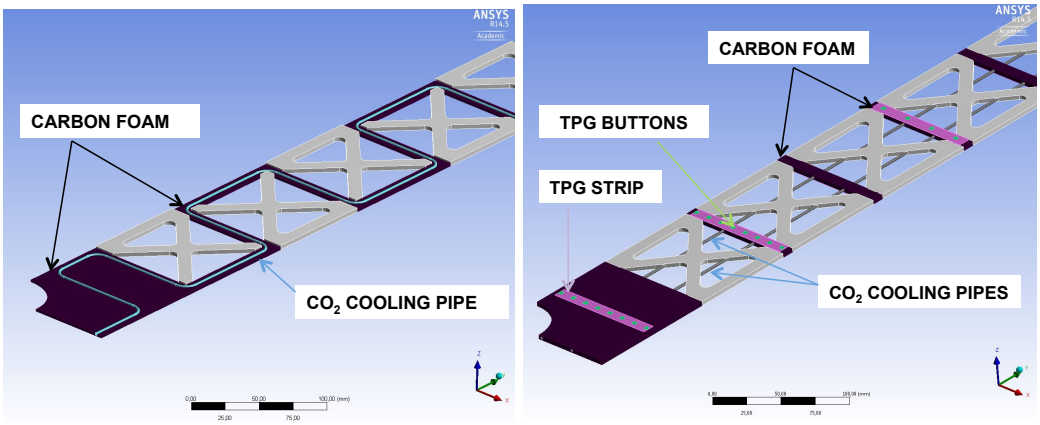

Figure 4: Snake pipe (left) and parallel pipe (right) design, showing the cooling tubes and the mechanical structure of the stave.

5. Sensors

There will be four different types of sensors, whose properties are summarised in Tab. 1. Two different technologies will be adopted depending on the expected radiation damage: n-in-p for sensors in the central region and p-in-n for the remaining sensors.

There will be two technological challenges involved in the sensor design: the circular cut out of the innermost sensors and an embedded pitch adapter, that is, a second metallization layer, that will allow transitions from the strip pitch of 190 μm on the outermost sensors to the input pad pitch of the ASICs of approximately 80 μm. The embedded pitch adapter presents two main advantages with respect to the conventional solution using an external pitch adapter: reducing the number of wirebonds, thus decreasing the probability of wirebond failures, and reducing the material budget. A solution based on an external pitch adapter is also being considered.

6. Modules

The design of the modules is rapidly evolving and the current iteration is shown in Fig. 5. A kapton hybrid flex will host the ASICs and will provide electrical connection to the data/power flex cable, to which it will be wirebonded. The ASICs will be glued to the hybrid flex using an electrically conductive epoxy. The hybrid flex will have copper thermal vias to optimize the thermal path from the ASICs to the cooling system. The hybrid flex and the sensor will be glued to a thin support structure, referred to as the "stiffener", using two different types of glue, differing

in their thermal conductivity. This design feature is important to limit the heat transfer from the ASICs to the sensor. The stiffener will extend under the sensor along two of its edges and will consist of a material, still under investigation, that will give mechanical rigidity to the module and will allow handling during production and testing. Several options are being considered for the material, although the preferred choice at the moment is Pyrolytic Boron Nitride (PBN), since it has a coefficient of thermal expansion that is very similar to that of the silicon and it is both thermally conductive and electrically insulating. The module will be fixed to the stave using a thin layer of removable epoxy.

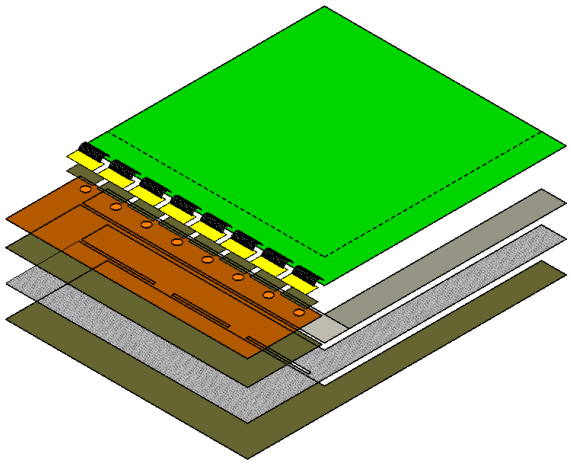

Figure 5: Layout of the module. The sensor, in green, and the ASICs, in yellow, are connected through wirebonds, in black. The hybrid flex is shown in orange, the stiffener is shown in shaded gray, and the different types of glue are shown in dark green and gray.

7. Thermal and mechanical studies

The results of a thermal simulation of the stave with the snake pipe design are shown in Fig. 6. In the simulation, each ASIC is connected to the sensor through 128 wirebonds of 25 μm diameter. The values in the profile correspond to the difference in temperature between sensor/ASICs and coolant, where the temperature of the coolant is set to 0°C. The maximum difference in temperature between coolant and sensor is found to be 5°C, while the one between coolant and ASICs is found to be 24°C. The higher temperature in the upper part of the sensor is due to the heat transfer from the ASICs through the wirebonds. The lower temperature on the right side of the sensor is due to the cooling tubes that are passing underneath. According to the simulation, all the requirements of the cooling system are met by this design when using an evaporation temperature of -30°C.

Besides the thermal simulation, a first mechanical/thermal prototype is now available: the support/cooling layer is made of realistic stave materials and is based on the snake pipe design with bent titanium cooling tubes glued into the stave using epoxy. The sensor is mimicked by thin plates of silicon in the center of the stave and brass in the rest. The heat load of the ASICs is mimicked by heaters. The prototype has been successfully cooled down, well below the nominal

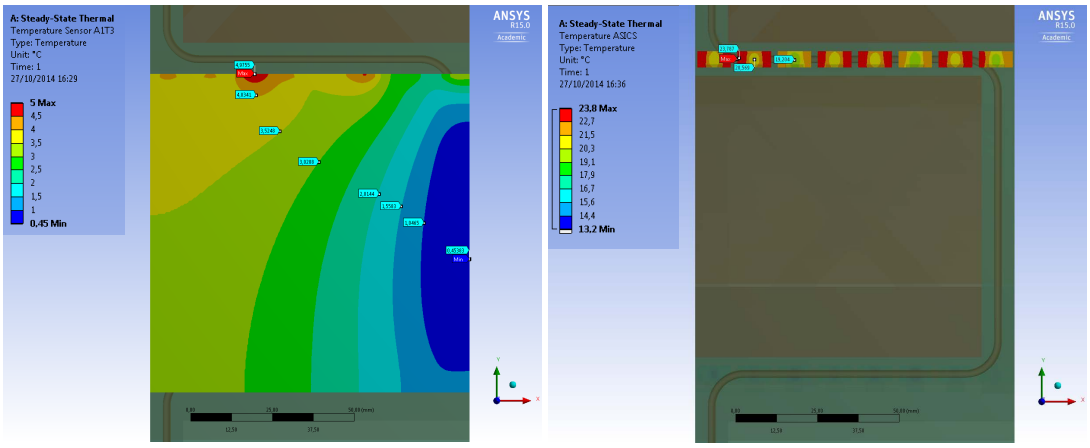

Figure 6: Temperature profile on the sensor (left) and on the ASICs (right) for a module with 8 ASICs obtained from a simulation of the current stave design with the snake pipe. Strips run vertically, cooling tubes pass underneath the ASICs and then go down on the right side.

temperature of the sensors, and several measurements are currently ongoing, including deflection and thermal stresses.

8. SALT ASIC

The SALT chip, whose block diagram is shown in Fig. 7, will read out 128 channels at 40 MHz, will be manufactured in TSMC CMOS 130 nm technology, and will have an input pad pitch of approximately 80 μm. It will have an analogue block, consisting of a preamplifier and a shaper, to guarantee a fast signal, with a peaking time of less than 25 ns and a remainder 25 ns after the peaking time of no more than 5% of the peak value. This design will reduce spill over between consecutive LHC bunch crossings. It will be optimised for load capacitances of up to 15 pF and will have a power consumption of $1-2$ mW/channel. There will be both n-in-p and p-in-n sensors, and the SALT chip will be able to read out both polarities. The shaper will be followed by a SAR ADC with 6 bit resolution operating at 40 Ms/s. Once digitized, the data will be fed to the digital signal processing block, that will allow the experiment to mask bad or noisy channels and perform pedestal subtraction, mean common mode subtraction, zero suppression, and data compression. The last block will create and transmit the data frames to the peripheral electronics located on the outer frame of the detector box. Data frames will be transmitted through e-links using the SLVS standard at 320 MBit/s data rate. Each ASIC will be equipped with 5 e-links, but only some of them will be active, depending on the expected hit occupancy on the sensor. The total power consumption of the ASIC is expected to be below 1 W at room temperature.

9. Flex cable

The flex cable will connect the hybrids and the peripheral electronics, transmitting data, control signals, and power. It will run along the stave, from the top and bottom to the center, and will have a length of up to 0.8 m.

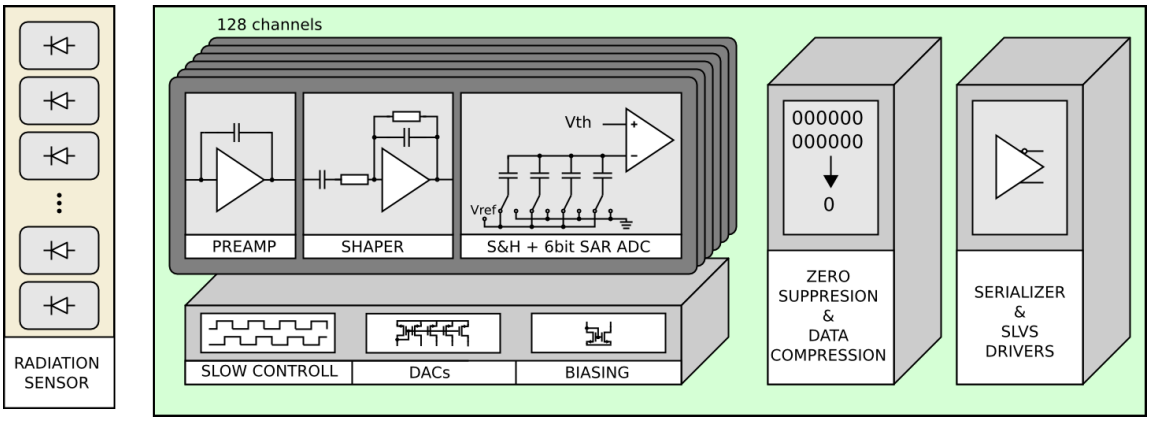

Figure 7: Block diagram of the SALT ASIC readout chip.

The main requirements on the flex cable design are low material budget, low voltage drop, with a maximum round trip drop of 0.5 V, and good signal integrity. The first prototype design is shown in Fig. 8. It consists of two layers of kapton and copper traces, with signal traces in the top layer and power traces in the bottom layer. All traces are terminated with bond pads that will be connected to the hybrids. On the outer end, the flex cable will be connected to the peripheral electronics through an appropriate connector. First prototypes will be ready to be tested in autumn 2014.

Figure 8: Flex cable design. Signal traces are shown in red and power traces are shown in blue.

10. Peripheral electronics

The peripheral electronics will perform further digital signal processing that cannot be included in the front-end electronics, since it would imply a significant heat load and amount of material budget in the sensitive area of the detector. It will consist of several boards, shown in Fig. 9, each with a specific function: electrical to optical transition (DCB), distribution of fast timing and slow control signals (TFC/ECS), and low/high voltage power conditioning and distribution. The peripheral electronics will be located on the outer frames of the detector box, close to the detector planes, although the exact location is not decided yet. After the electrical to optical transition, the data will be sent to the TELL40 readout boards located in the counting room, at a distance of 300 m from the detector, and thereafter will be available to the trigger.

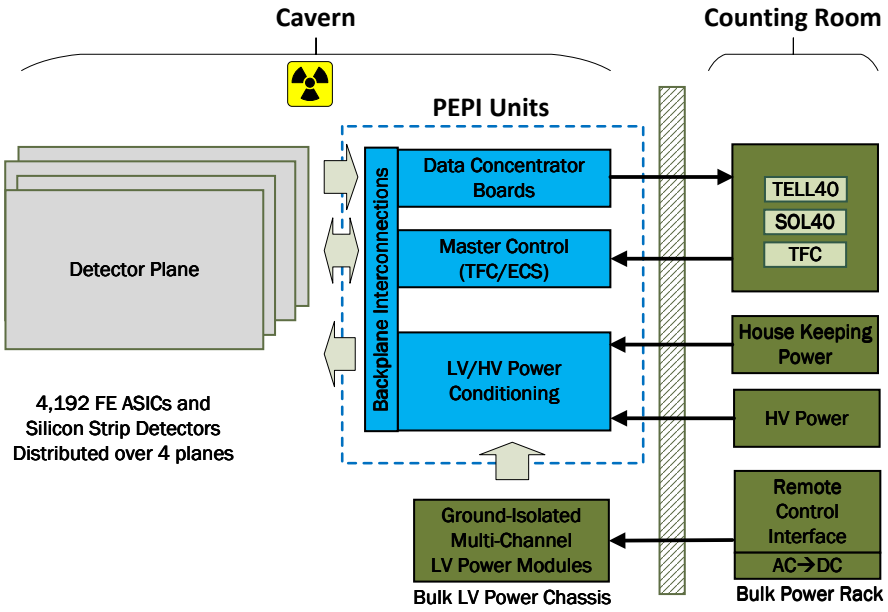

Figure 9: Block diagram of the electronics in the cavern and in the counting room. The peripheral electronics is shown in blue.

11. Test beam activities and general planning

Some prototype sensors of both technologies are already available: they have been irradiated with different doses, up to 23 MRad, using low energy protons at the Massachusetts General Hospital in Cambridge, and will be tested during a test beam at the SPS at CERN in October/November 2014. Since the SALT chip is not available yet, a Beetle-based readout system (ALIBAVA) [8] will be used. The setup has been commissioned during an exploratory test beam at the PS at CERN in July/August 2014 and has been successfully synchronized with the Timepix beam telescope [9]. An 8-channel prototype of the SALT chip is planned to be submitted in autumn 2014 and should be available for tests in early 2015. For the next year, it is foreseen to test prototype sensors with circular opening using the 8-channel prototype of the SALT chip. In parallel, many R&D activities are carried out in the participating institutes.

The R&D phase is foreseen to continue until 2016, partially overlapping with the production and testing phase in 2015-2018, to conclude with the installation of the UT in the cavern, expected for the first quarter of 2019.

References

[1] LHCb collaboration, A. A. Alves Jr. *et al.*, *LHCb tracker upgrade technical design report*, CERN-LHCC-2014-001, LHCB-TDR-015.

[2] LHCb collaboration, A. A. Alves Jr. *et al.*, *The LHCb detector at the LHC*, *JINST* **3** (2008) S08005.

[3] LHCb collaboration, A. A. Alves Jr. *et al.*, *LHCb trigger and online upgrade technical design report*, CERN-LHCC-2014-016, LHCB-TDR-016.

[4] E. Bowen and B. Storaci, *VeloUT tracking for the LHCb upgrade*, LHCb-PUB-2013-023, CERN-LHCb-PUB-2013-023.

[5] T. T. Bohlen, F. Cerutti, M. P. W. Chin, A. Fassò, A. Ferrari, P. G. Ortega, A. Mairani, P. R. Sala, G. Smirnov, and V. Vlachoudis, *The FLUKA code: developments and challenges for high energy and medical applications*, *Nuclear Data Sheets* **120**, 211-214 (2014).

[6] A. Ferrari, P. R. Sala, A. Fassò, and J. Ranft, *FLUKA: a multi-particle transport code*, CERN-2005-10 (2005), INFN/TC_05/11, SLAC-R-773.

[7] P. Moreira, *The GBTx link interface ASIC*, https://espace.cern.ch/GBT-Project/GBTX/Specifications/gbtxSpecsV1.8.pdf, October, 2012.

[8] ALIBAVA collaboration, R. Marco-Hernandez *et al.*, *A portable readout system for microstrip silicon sensors*, *IEEE Trans. Nucl. Sci.* **56**, 1642-1649, 2009, doi:10.1109/TNS.2009.2017261.

[9] K. Akiba *et al.*, *The Timepix telescope for high performance particle tracking*, http://arxiv.org/abs/1304.5175.