PROCEEDINGS OF SCIENCE

CMS Pixel Detector: Operational Experience and Run 1 to Run 2 Transition

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The CMS Pixel detector is at the centre of the CMS experiment and is made of three barrel layers and four endcap disks. It is essential for the reconstruction of track seeds and secondary vertices. Some aspects of the CMS Pixel detector operations during the first LHC run are presented. The work carried out during the first long shutdown of LHC (LS1) to prepare the detector for Run 2 and the plan for 2015 operations are also described.

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1. Introduction

The inner tracking system of the Compact Muon Solenoid (CMS) experiment [1] has at its core silicon pixels surrounding the beam pipe. This is the innermost detector system of CMS, which operates in the harsh LHC (Large Hadron Collider) environment, providing high precision tracking in the region closest to the interaction point. It plays a key role in secondary vertex reconstruction, fundamental for the identification of jets originating from the decay of b quarks. It generates the innermost seeds for tracks reconstruction, providing complementing information to the strips detector.

LHC delivered proton-proton collisions since 2010 at a centre of mass energy of 7 TeV for two years until 2012, when the energy was increased up to 8 TeV. The machine reached a peak instantaneous luminosity of 7.7 x 10^{33} cm^{-2} s^{-1}, with up to 20 hard interactions per single bunch crossing on average. By the end of Run 1, LHC delivered 6 fb^{-1} of data at 7 TeV and of 23 fb^{-1} of data at 8 TeV. The LHC operations stopped in early 2013 to upgrade the machine during a first long shutdown period (LS1) in 2013 and 2014.

The CMS Pixel detector (Fig. 1) is structured in three cylindrical barrel layers, BPix, and four forward disks, FPix. The BPix layers are located at distances of 4.3, 7.2 and 11 cm from the beam line and extend for 55 cm along the beam line. The endcap disks are placed at 34.5 and 46.5 cm from the interaction point along the beam direction (z axis) at each side of the barrrel. They extend from an inner radius of 6 cm to an outer radius of 15 cm. The disks/layers overlapping structure provides a coverage in pseudorapidity [1] up to $|\eta| = 2.5$. The entire detector includes 66 million

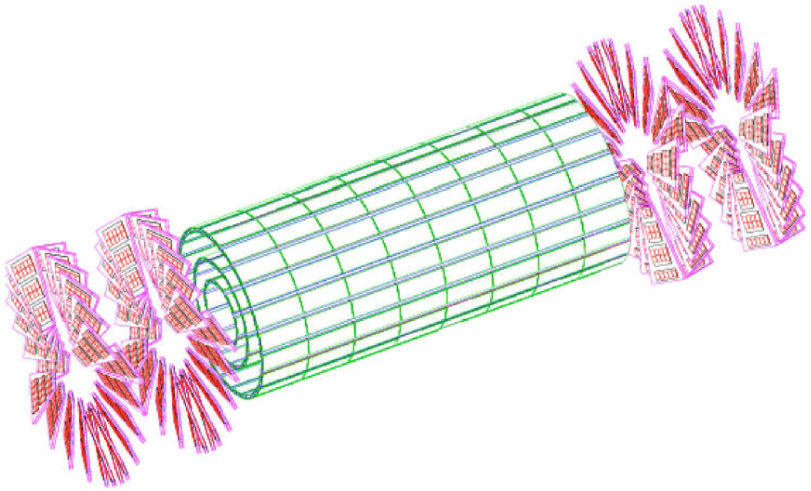


Figure 1: Schematic view of the CMS Pixel detector. The three barrel layers (green) surround the interaction point. Two endcap disks (red) are located on each side of the barrel.

$100 \times 150\ \mu m^2$ pixels . The pixel detector is based on an n+ implant on n bulk silicon sensor tech-

[1] CMS uses a right-handed coordinate system with the z-axis pointing along the LHC counter-clockwise beam direction, the x-axis pointing toward the center of the ring, and the y-axis pointing upward. The pseudorapidity is defined as $\eta = -\ln \tan(\theta/2)$, where θ is the polar angle.

nology. The readout chips (ROCs) [2] are bump-bonded to the sensor serving an array of 52 x 80 pixels each. The ROC applies zero suppression on data: only signal passing a threshold constitute a "hit". The hit analog pulse height, the pixel address and time information are buffered and read out if the event matches a trigger. Charge sharing is exploited to achieve hit position resolution much better than pixel size. ROCs are wire bonded to the High Density Interconnect (HDI), a low-mass printed circuit board, on which the Token Bit Manager (TBM) chip are located. The TBM distributes clock and trigger to ROCs, manages the ROC controls and readout [3]. The analog electrical signal is translated to optical by analog-to-optical transducers (Analog Optical Hybrids, AOHs) and sent via optical fibers to the Front End Drivers (FEDs) for digitisation and distribution to the central CMS Data Acquisition (DAQ).

2. Run 1 operation experience

2.1 Detector status

By the end of Run 1 the fraction of operational channels was 97.7% in the barrel and 92.2% in the endcaps. Few channels in BPix were lost most likely because of disconnected wire-bonds, while others were deactivated later in 2012 because they generated occasional readout errors which required module resets. In the endcaps an entire panel of one of the external disks was lost due to a broken optical readout. Other channels were lost because they produced a distorted pulse shape which resulted in a signal misidentification in the analog pulse train. The repair of the disabled channels was planned for LS1 after the extraction of the pixel detector from CMS.

2.2 Calibration routine

Detector functioning and performance depend on proper calibrations of readout chain parameters. The analog signal readout from the ROC contains information about each pixel hit: pixel coordinates and charge collected. An example of a ROC readout is shown in Fig. 2. The pixel address is encoded into six discrete levels and is contained in five clock cycles. The charge information follows the address and it's stored in the last clock cycle [4]. During commissioning and operations, the detector needed to be re-calibrated in order to guarantee optimal data readout and transfer to off-detector electronics and to central DAQ.

Most of the readout parameters are quite stable unless major changes occur, such as the detector operating temperature. Other parameters are more sensitive to environmental variations. For these parameters a re-calibration on a regular basis was necessary during Run 1 operations, mainly once per week. The offset of the optical receiver in the FED needed to be adjusted to keep the baseline level of the signal in the middle of the ADC range. This baseline calibration was performed often because of its sensitivity to temperature variations. Automatic corrections are also applied to cope with minor temperature fluctuations. After baseline calibration, the address level calibration was also performed to ensure a good separation of address levels for an optimal decoding of pixel coordinates.

Pixel thresholds and noise were measured weekly to monitor their evolution with integrated luminosity. The SCurve method is used to characterise threshold and noise. It consists of measuring the efficiency of a pixel as function of the injected charge. The threshold is measured from the

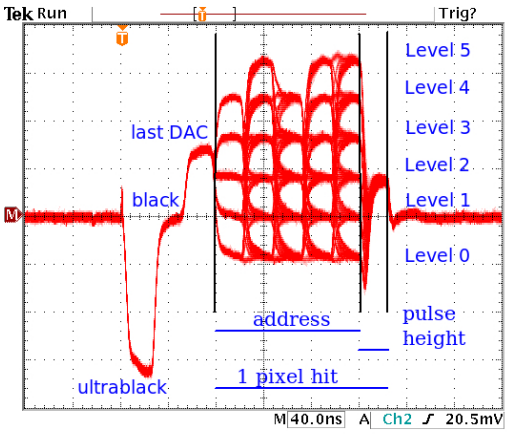


Figure 2: Oscilloscop view of the overlay of several signals read out from the same ROC.

resulting curve, a sigmoid, as the value of injected charge corresponding to an efficiency of 50% (Fig. 3).

Pixel thresholds affect detector resolution. With lower thresholds, larger clusters are reconstructed,

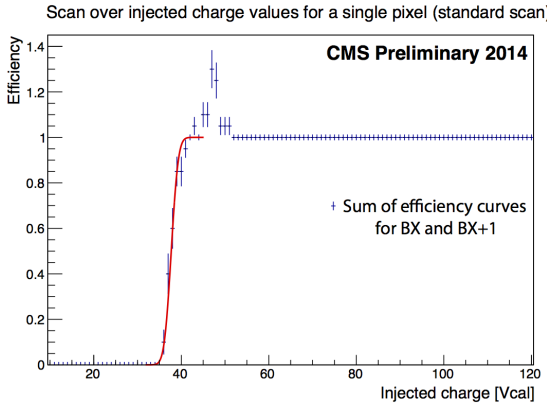


Figure 3: Single pixel efficiency curve determined performing a scan over 110 values of injected charge (Vcal units). The curve is the result of the sum of efficiency curves for the In-Time bunch crossing and the following one (BX and BX+1). The measured threshold is given by the value of the injected charge for which the efficiency is equal to 50%. Points exceeding 100% efficiency are due to statistical fluctuations of the two curves in the turn-on region. The effect on the fit is negligible.

which improves charge sharing. Threshold adjustment was performed during Run 1 at every LHC technical stop, about every 6-8 fb^{-1}. We lowered thresholds just above the failing points, by following an iterative procedure which is based on the SCurve technique.

About three times a year the signal pulse height in ADC counts is measured as a function of the injected charge (gain calibration) to determine the linearity of response. The constants of response

parametrization are stored and used later for offline reconstruction.

3. Radiation damage

The CMS pixel detector was designed to cope with the high radiation environment of LHC and to operate with the highest performance even after the accumulation of significat radiation doses. Nevertheless, it is necessary to monitor the radiation damage during operations. One of the first visible effect of radiation is the increase of the sensor leakage current with integrated luminosity, due to the damage in silicon bulk. Figure 4 shows the trend of the leakage current versus integrated luminosity. The damage was only partially recovered by annealing. Between the end of 2011 and the beginning of 2012 the operating temperature was decreased from 7.4°C to 0°C achieving a reduction in leakage current by a factor two. The overall trend of leakage current observed in CMS

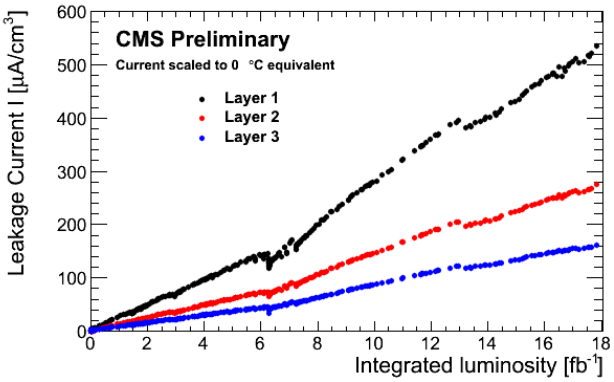


Figure 4: Average leakage current in each barrel layer as function of the accumulated integrated luminosity. The measured currents are normalized to the volume of active silicon and extrapolated to 0°C for comparison purposes.

in Run 1 is in agreement with models except for the normalization. The reason for this discrepancy remains under investigation. A variation of the leakage current with azimuthal angle was also observed (Fig. 5). This is due to an offset of the barrel pixel position with respect to the beam spot of LHC.

The depletion voltage was also monitored during operations. A dedicated scan of bias voltage was performed several times per year, by varying the detector bias voltage from the operating value (300 V for BPix and 600 V for FPix) to 0 V and measuring the hit efficiency. Figure 6(a) shows the results of hit efficiency measurements for Layer 1 of the barrel between 2011 and the beginning of 2013. The dependence of the voltage needed to achieve 99% efficiency on the integrated luminosity is shown in Fig. 6(b) for the barrel layers and endcap disks. The presence of a minimum for Layer 1 and Layer 2 is evidence for type inversion occurrence for the two layers.

The evolution of the pixel thresholds and the analog currents was also frequently monitored in Run 1. An increase of both pixel thresholds (Figure 7(a)) and analog currents (Figure 7(b)) was observed with integrated luminosity. The possible explanation for these changes is the radiation

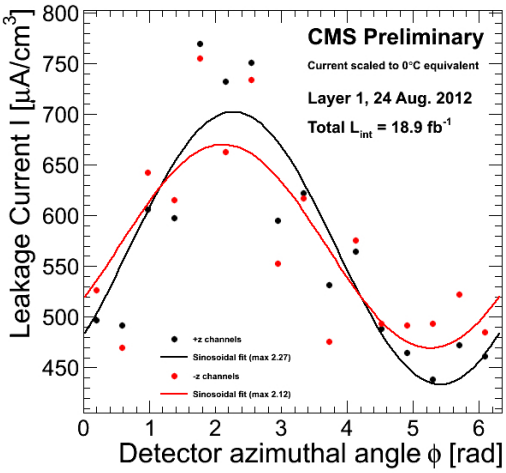
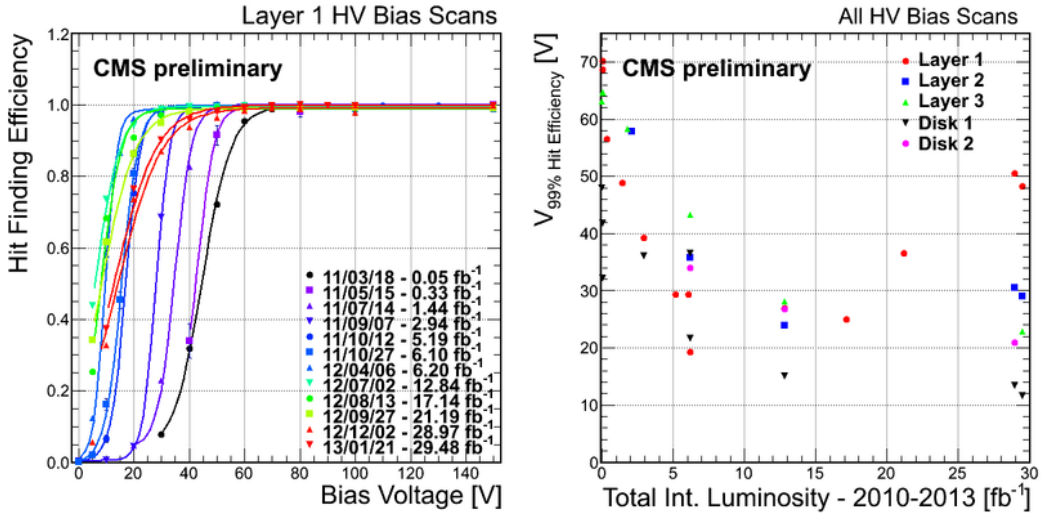


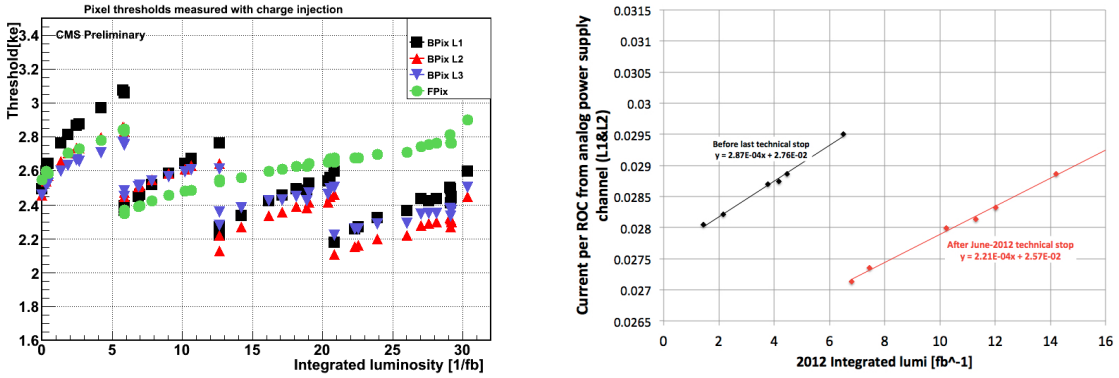
Figure 5: Leakage current as function of azimuthal angle for Layer 1.

damage in the bad-gap reference voltage circuit, which would shift al voltage settings inside the ROC. The described effect required a re-calibration of the analog voltage and the pixels threshold during technical stops, in order to recover the optimal ROC performane.



(a) (b)

Figure 6: Left: hit efficiency measurement versus bias voltage for Layer 1 scans performed up to 2013. Points are fitted with a turn-on curve. Right: bias voltage at 99% hit efficiency as function of integrated luminosity for all the bias scans performed up to 2013 on barrel layers and endcap disks.



(a) (b)

Figure 7: Left: average pixel thresholds in units of 1000 electrons for barrel layer 1 (black), 2 (red) and 3 (blue), and for the forward pixels (green) as a function of delivered integrated luminosity in 2011 and 2012. Right: average analog current per ROC drawn by the power supply as a function of integrated luminosity delivered in 2012.

4. Detector performance

Spatial resolution is measured with the triplet method [5]: tracks with 3 hits in the pixel detector are used and a refit is performed using hit positions in pixel Layer 1 and 3. The position in Layer 2 is hence extrapolated and compared to the actual position of the reconstructed hit. The resolution is then extracted from the residual distribution. A degradation is observed with integrated luminosity (Fig. 8), however the measured resolution was still better than 10 μm at the end of Run 1.

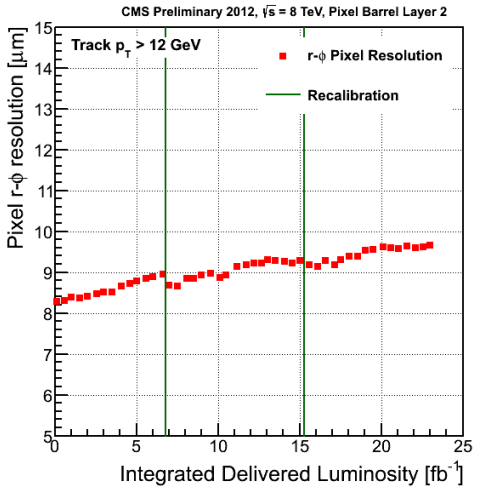
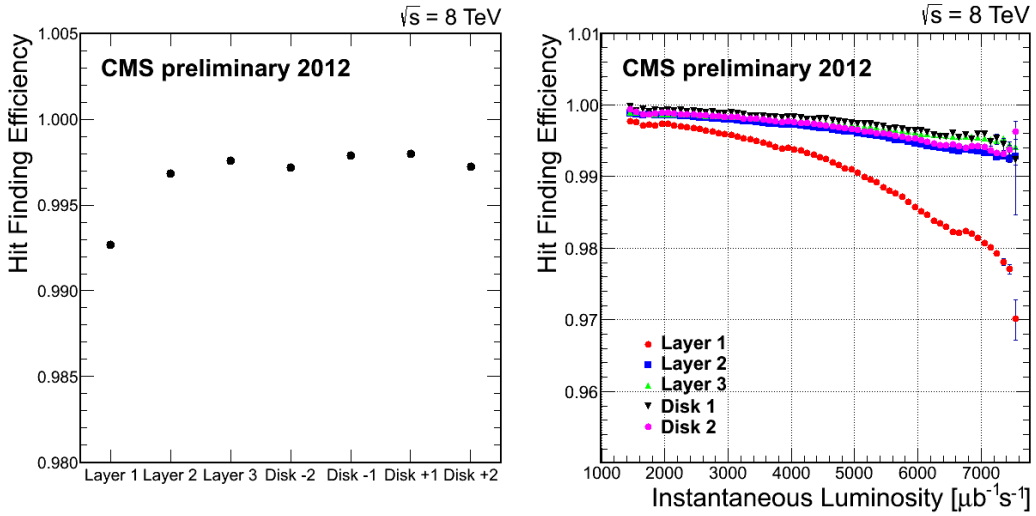


Figure 8: Barrel hit resolution measured in the r-ϕ plane as a function of integrated luminosity delivered in 2011 and 2012.

Pixel hit efficiency for working ROCs is well above 99% for all barrel layers and endcap disks (Fig. 9(a)). Inefficiencies have been observed as the LHC luminosity increased (Fig. 9(b)). This is due to dynamic data losses, mainly ROC event buffer overflow caused by high occupancy. This dependence of efficiency versus instantanous luminosity was predicted, and will be taken into account in the simulation for Run 2.



(a) (b)

Figure 9: Left: average pixel-hit finding efficiency in 2012 data. Right: Pixel-hit finding efficiency as function of instantaneous luminosity for all barrel layers and forward disks.

5. Long Shutdown 1

5.1 Detector Status

At the end of Run 1, the fraction of operational channels in the barrel pixel detector was about 98%, and about 92% in the forward disks. During LS1, both BPix and FPix were extracted from CMS for maintenance with the purpose to recover the broken channels.
In the barrel some channels were deactiveted later in 2012 because they generated occasional read-out errors which required a module reset. The failure of the other channels was most likely due to a break of wire bond connections between ROCs and HDI PCB. Seven inoperative modules, placed on the outer face of Layer 3 ($\sim$ 1.1% of BPix channels) were substituted. An effort is ongoing to repair or replace all remaining faulty modules by the end of LS1.
In addition to the faulty modules, some problems involving services were also observed. Two AOHs were not working properly. The fault was due to disconnected wire bonds between the laser and the AOH PCB. Both AOHs were replaced.

The fraction of not operational FPix channels at the end of data-taking was about 7.8%. In the endcap there were different kinds of failures: for 3.6% of the FPix readout channels, the analog signal could not be digitized by the back-end electronics due to distortion of the signal. This was found to be related to a poor connection between the HDI and the AOH. A total of 3.1% of FPix channels (6 panels) was unavailable because the AOHs had become disconnected; and for 1.1% of

FPix there were problems at the sensor level. All these failures have been investigated, understood and repaired during LS1.

5.2 Calibration procedure improvements

Pixel thresholds adjustment is an iterative procedure, based on the measurement of pixel thresholds using the SCurve method. The threshold measurement is performed for several ROC threshold settings to find the minimum value of the threshold. Such kind of measurement is highly time consuming due to the large range of charge values injected per ROC. The scan range is much larger than the region of interest: the turn-on of the curve. An improved technique was developed during the LS1 to reduce the range by more than a factor three and centre it around the turn-on point for each ROC. Figure 10 shows the efficiency curve resulting from the reduced scan for one pixel. The method exploits the knowledge of the linear dependence of the ROC global DAC threshold and the calibration charge to centre the range around the expected value for the pixel threshold. The decision of which values of charge to inject is then taken ROC by ROC. Moreover the entire procedure was automatized. This new implementation hugely speeds up the adjustment procedure, reducing the time needed for each iteration by more than a factor three.

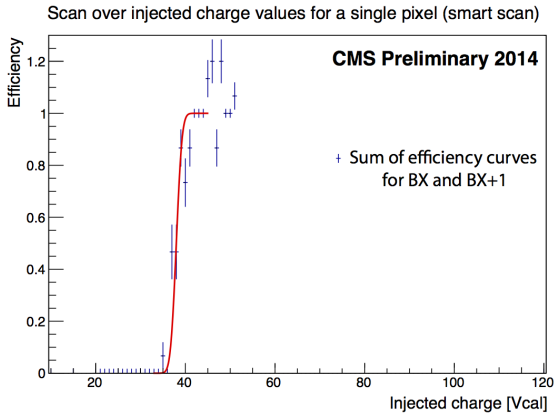


Figure 10: Single pixel efficiency curve determined performing an ad-hoc scan for each ROC (smart scan) limited to 30 values of injected charge (Vcal units) around the turn-on region. The curve is the result of the sum of efficiency curves for the In-Time bunch crossing and the following one (BX and BX+1). The measured threshold is given by the value of the injected charge for which the efficiency is equal to 50%. Points exceeding 100% efficiency are due to statistical fluctuations of the two curves in the turn-on region. The effect on the fit is negligible.

5.3 Single Event Upset

The ionizing particles traversing the pixel volume can deposit enough charge in the detector electronics to induce a bit flip in memory. These events are called Single Event Upset (SEU). They can affect registers at different levels. SEUs affecting single pixels have negligible impact on the data quality and don't need any intervention. If the operation of an entire ROC is compromised,

the ROC is not recovered immediately. When an SEU affects a TBM, or the auxiliary electronics, like an AOH, stopping data flow from a whole module or more, then immediate actions are taken and the detector is reprogrammed. ROCs in an upset state are also recovered then. In 2012 an automatic SEU identification and recovery mechanism was implemented [6]. It takes few seconds to identify an SEU, stops the CMS central data aquisition, reprogram the detector and restart data acquisition. The occurence of an SEU needing recovery was observed about every 73 pb^{-1}. The implementation of the automatic recovery mechanism allowed to reduce the pixel downtime by a factor of three.

6. Towards 2015 data taking

The second LHC collision run will start in spring 2015. The LHC will provide collisions at a centre-of-mass energy of 13 TeV with initial bunch spacing of 50 ns and instantaneous luminosities similar to 2012. After the first weeks of data-taking, collisions will take place at 25 ns bunch spacing with a planned peak instantaneuos luminosity of $1.7 \times 10^{34} cm^{-2} s^{-1}$. LHC should deliver up to 150 fb^{-1} of data by the end of Run 2.

The plan for 2015 is to keep the pixel detector cold in order to avoid reverse annealing and to limit the impact of radiation damage. The detector will operate at -15° C, a much lower temperature with respect to the previous Run. This is made possibile by the work done during the shutdown to improve the sealing of the pixel volume against humidity [7].

The position of the barrel pixel detector will be adjusted by a few millimeters during the installation in order to better place the centre of the pixel detector witwh respect to the beam axis. It was slightly shifted from the right position in the previous run, causing an unhomogeneous aging of the detector. The effect is visible in Figure 5.

A new and smaller radius beam pipe has been installed to allow the insertion of the Phase 1 Pixel Upgrade detector [8] during the 2016-2017 technical stop. The Phase 1 Upgrade Pixel detector has an additional barrel layer and two additional forward disks with respect to the present detector. It utilizes new digital readout chips. During the current shutdown new modules hosting the digital ROCs have been installed in two forward half disks added to the present detector (pilot system). This system will be extensively tested in the upcoming LHC run, before the insertion of the Upgrade detector.

7. Conclusions

The CMS Pixel detector performed very reliably during the first period of data taking. It coped well with the evolving high luminosity scenario of LHC, operating with an average hit efficiency above 99% for barrel layers and forward disks. The challenges of operating the detector in such rapidly changing environment were promptly faced thanks to the continuos effort in detector calibrations and online operations.

During LS1 the detector channels which showed malfunctioning in Run 1 were repaired: the 7.8% of FPix channels and the 2.3% of BPix channels. The 99.9% of FPix channels are again operational after repair, and an effort to similarly repair the BPix channels is undergoing.

In the next Run, LHC is expected to deliver data at high instantaneous luminosity and with much

higher pile-up with respect to the previous run. In order to reduce the effect of radiation the pixel detector will be operated at -15°C. The detector environment was prepared to operate at this temperature during LS1: a new sealing of the tracker volume has been provided ensuring a better protection against humidity.
The pilot system of the Phase-1 Upgrade Pixel detector has been installed in the present detector and will operate in 2015 to test the new modules before the insertion of the upgraded detector in the technical stop between 2016 and 2017.

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