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A prototype for the data acquisition of the CBM Micro-Vertex Detector

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The Compressed Baryonic Matter Experiment (CBM) will be installed at the SIS-100/SIS-300 heavy ion synchrotrons of the FAIR facility, which is currently under construction at Darmstadt, Germany. Its purpose is the study of hadronic matter in the region of highest net baryonic densities with rare probes, e.g. open charm particles. To reconstruct those particles, an ultra light Micro-Vertex Detector (MVD) with a spatial resolution of few micrometers and a material budget of 0.3% X_0 is required. Moreover, this MVD needs to handle an ambitioned collision rate of $\sim 10^5$ Au+Au collision with up to 35 AGeV beam energy.

The MVD will rely on CMOS Monolithic Active Pixel Sensors (MAPS), which are being developed by the PICSEL group of IPHC Strasbourg. To integrate the MAPS into the global, trigger-less data acquisition (DAQ) system of CBM, one requires equipping the MVD with a free-streaming, dead-time free DAQ. The latter has to steer and to synchronize the ~ 400 sensors of the MVD and to handle their continuous data stream of several 100 Gbit/s.

We introduce a prototype of this local DAQ system, which is based on the Trigger and Readout Board (TRB) originally developed for the upgrade of the HADES detector, and demonstrate the feasibility of matching the requirements. Moreover, we discuss results from an in-beam test of the system, which was carried out at the CERN-SPS.

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1. Introduction

The Compressed Baryonic Matter (CBM) experiment is currently being prepared for the upcoming FAIR facility in Darmstadt, Germany. The heavy ion experiment will investigate exotic states of matter in the region of highest baryonic densities (up to $\sim 35\,$AGeV beam energy for Au-Au). The CBM detector is designed as a dedicated high-luminosity, multi-purpose device with a fixed-target layout.

CBM plans to detect open-charm particles with a Micro-Vertex Detector (MVD) by means of secondary vertex reconstruction. In order to achieve the necessary vertex resolution of $\sim 50\,\mu$m, the MVD needs to provide a spatial resolution in the order of few µm, a material budget of $0.3\%\,X_0$ for the first and of $0.5\%\,X_0$ for the other three detector stations, respectively. Moreover, the rates needed for obtaining the required measurement statistics (~ 100 kHz Au+Au collisions) call for a radiation tolerance of $\gtrsim 3\,$MRad and $\gtrsim 10^{13}\,n_{eq}/cm^2$, and readout time of $\lesssim 30\,\mu$s.

To match those requirements, we intend to equip the MVD with CMOS Monolithic Active Pixel Sensors (MAPS), which provide an excellent spatial resolution of $\sim 3\,\mu$m and tolerate up to $\sim 10^{14}\,n_{eq}/cm^2$ and ~ 10 MRad [1].

The studies on the MVD prototype were carried out with $50\,\mu$m thick MIMOSA-26AHR [2] sensors, which hosts 660k pixels with $18.4\,\mu$m pitch on an active area of $2.2\,cm^2$. The readout is done within $115.2\,\mu$s by means of a column-parallel rolling shutter. The pixels are integrated on a standard CMOS wafer, which allows for adding the circuits needed for performing data digitization and data sparsification based on zero suppression within a 3 mm wide passive strip on the same chip. The data obtained is buffered in an internal SRAM memory and pushed out via two 80 Mbit/s LVDS output channels towards the DAQ system. For configuration, the sensor hosts a JTAG interface. Despite the fact that this (meanwhile outdated) sensor does not yet match the requirements of CBM in terms of radiation tolerance, readout time and data rates, its architecture is considered as a valuable precursor of the final MVD sensor.

2. Requirements on the local DAQ system of the MVD

The MVD will be formed from four planar detector stations hosting a total of ~ 400 sensors, which create a total data flow of few 100 Gbit/s after data sparsification and data compression. The sensors will be read out with a rolling shutter, and thus with a fixed readout time. The data obtained will be pushed continuously to the DAQ of the MVD. Here, the data packets have to be decoded in real time, to be checked for potential data corruption as caused by single event upsets (SEU) and to be re-encoded to the data format of the central DAQ of CBM. Among others, this encoding requires to add time stamps based on the absolute system time of CBM, which are to synchronize the data from the MVD with the one from the other sub-systems of the experiment. Moreover, the local DAQ may carry out first pre-processing steps like grouping fired pixels and an additional data compression [3] in the future.

The local DAQ needs to be able to monitor the sensors and to recognize sensor failing due to SEU or latch-ups. In both cases, it needs to recover the sensors by performing a rapid power cycle and restarting the sensors hereafter in a controlled way. Moreover, a data throttling mechanism is necessary in order to react to a potential input overflow caused by beam fluctuations.

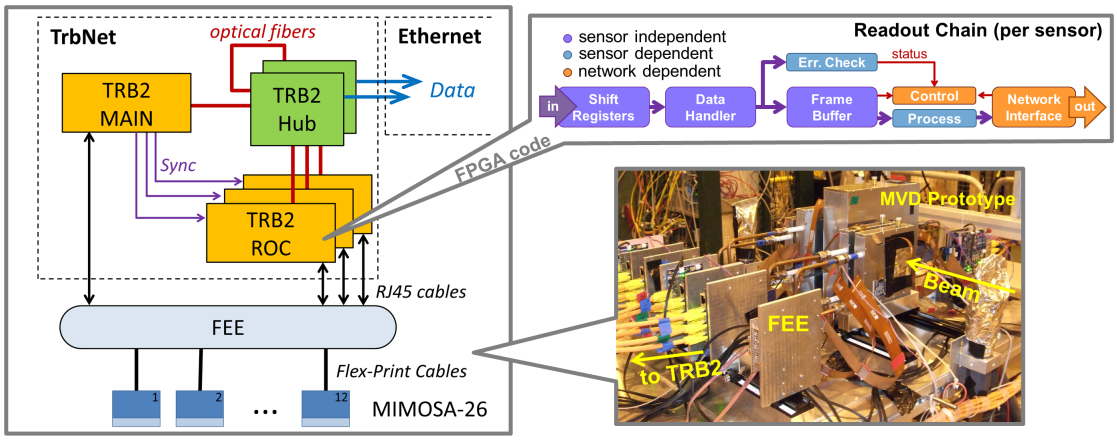

Figure 1: Block diagram of the MVD DAQ prototype

3. The MVD prototype DAQ

The first MVD prototype based on MIMOSA-26AHR was recently assembled and tested with a $40-120\,\mathrm{GeV/c}$ pion beam at the CERN-SPS [2]. The prototype DAQ [4] is designed to operate a total of 12 sensors, which are arranged as a six layer beam telescope. The sensors are biased via dedicated flex print cables connected to customized front-end electronics (FEE), which host circuits for voltage regulation. Moreover, the current of each individual sensor is monitored and a power cycling is carried out in case of a latch-up. The active part of the prototype DAQ bases on TRB2-FPGA boards [5] designed for the upgraded DAQ system of the HADES experiment, which allow to extend the prototype DAQ to any reasonable bandwidth and number of sensors by adding hardware.

As shown in Fig. 1, TRB2 boards with three different kinds of firmware were deployed. The so-called MAIN-board synchronizes the network by sending periodic synchronization pulses, which are among others used to recognize potential losses of synchronization between the sensors. Moreover, it performs the fast and the slow control of all sensors by providing a common clock to all sensors and configuring them by means of a JTAG slow control interface. Once being configured, the sensors are started by a dedicated LVDS signal and remain in synchronous operation due to their fixed and deterministic readout time. The sensor push their $2\times80\,\mathrm{Mbit/s}$ data streams and their clock toward the Read-Out Controller boards (ROC), which handle up to four sensors each. As mentioned before, the ROCs decode the data, perform error checks and add status information and time stamps indicating the start time of the related readout cycle. An integrated buffer stores the data from several frames in order to compensate for data rate fluctuations. Finally, the data is encoded to the TrbNet standard [5] and sent via $2\,\mathrm{Gbit/s}$ optical links to the Hub-boards. These serve as a data concentrator and translate the data to the UDP-protocol. This protocol over optical Ethernet is used to push the data to the mass storage computer.

4. Test results and conclusions

The in-beam test was used to study the full readout scheme under realistic operating condi-

tions. A focus was laid on confirming the stability of the FEE and FPGAs, as well as the reliability of the JTAG and slow control utilities. Furthermore, the correctness of the sensor synchronization and the timestamping mechanisms were validated. Finally, we tested the behavior of the system at the limits of data throughput, which was 100 MB/s due to the limits of the Gigabit Ethernet links used for sending the data to our PC-based data server.

The system was operated during four full days and tested with the highest particle flow delivered by the beam line ($\sim$ 90 particles per frame and sensor corresponding to $\sim$ 40 kHz/cm^2). Typical data rates were in the range of 6 - 26 MB/s. The particle tracks were successfully reconstructed by means of off-line data analysis and a particle detection efficiency substantially above 99% was demonstrated. This confirms the successful synchronization of all sensors, which was furthermore monitored by comparing the syncronization signals generated by the sensors with the ones generated by the MAIN-board. No loss of synchronization was observed during the entire beam time. Individual incidents, which may have been caused by Single-Event-Upsets (SEU), were automatically recovered.

The throttling mechanism of the DAQ was tested by intentionally reducing the thresholds of some sensors to very low values. Due to this setting, the affected sensors generated each 20 MB/s of useless data each, which overloaded the bandwidth of the Ethernet connection toward the mass storage PC. As expected, the readout network recognized this problem and continued operating in a stable way by applying a controlled throttling scheme: data bursts of up to 50 synchronous and useful frames were recorded coherently from all sensors. Hereafter, a controlled dead-time was initiated. During this dead-time, the sensors remained in synchronous operation but the data obtained was rejected by the ROCs. This allowed the data stored in the buffers to be evacuated to the mass storage.

5. Conclusion and outlook

The concept of the local DAQ of the CBM-MVD was tested and validated by means of a dedicated prototype. Due to its scalable design, the prototype system is considered as being conceptually suited to build a full local DAQ. However, we started migrating our concept to the novel and more powerful TRB3-board [6]. This step will ease handling the higher data rates of the MAPS foreseen for the final detector and allow for handling more sensors per board. Both features should turn into a more cost efficient solution. Finally, we are developing FPGA-based pre-processing routines [3], which are expected to reduce the load on the central CBM DAQ.

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