

## Topology in the future ATLAS Level-1 Trigger

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### ABSTRACT:

The ATLAS experiment examines the decays of highly energetic particles produced in proton-proton collisions at the Large Hadron Collider (LHC). Resuming operation at the beginning of 2015 for Run 2, the LHC will work with an increased center-of-mass energy of 13 – 14 TeV, which will result in an unprecedented luminosity and higher bunch intensity. The first trigger level (Level-1) of the ATLAS trigger system, based on custom-made electronic modules, needs to be upgraded to control the increased trigger rate, while keeping good efficiency for interesting physics events. In Run 1 the Level-1 trigger decisions were mostly based only on multiplicities of trigger objects (such as electrons/photons, jets, taus, muons above energy/momentum thresholds) observed in the calorimeters and the muon spectrometer. As part of the Level-1 upgrade a new trigger module, the topological processor (L1Topo) will be included into the trigger chain. It is intended to evaluate spatial correlations of trigger objects and to perform more complex kinematic calculations such as an invariant mass. This requires having as much as possible of the trigger object information in one place for maximum flexibility in the evaluation of the topological information. Therefore both of the two identical topological processor modules need an aggregated input bandwidth of at least 1TBit/s. The processing of the incoming data takes place in real-time and in less than the budgeted 200ns. In this contribution the design of the L1Topo modules is discussed and test results on prototypes of the L1Topo modules are presented.

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## 1. Introduction

The ATLAS experiment [1] at the Large Hadron Collider (LHC) is a general-purpose detector designed to examine rare physical processes by observing particles produced in proton-proton collisions. In the first phase of the experiment (Run 1, ended in March 2013) the LHC collided proton bunches at a frequency of 20 MHz with a center-of-mass energy of up to 8 TeV, resulting in a peak luminosity of  $0.77 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ . The trigger system, subdivided in three levels, selected events of interest for a storage rate of 200 – 400 Hz. The first level (Level-1 [2]) consists primarily of FPGAs and custom ASICs and evaluates coarse granularity data of the calorimeters and the muon spectrometer. Because it is buffering the whole detector data in pipeline memory, this level is limited to make its trigger decision in less than  $2.5 \mu\text{s}$ . Therefore this level is designed as a pipelined, synchronous system, which is further divided into the calorimeter trigger (L1Calo), the muon trigger (L1Muon) and the Central Trigger Processor (CTP) (see figure 2). Based on multiplicities of trigger objects (electrons/photons, taus, jets and muons) and the missing transverse energy (MET), the CTP makes its trigger decisions with a trigger rate of up to 75 kHz. Currently the LHC is undergoing an upgrade during the Long-Shutdown 1 (LS1) to achieve its design center-of-mass energy of 13 – 14 TeV and will resume operation at the beginning of 2015 (Run 2) [3]. Simultaneously, the bunch crossing frequency will be doubled to 40 MHz with more focused proton bunches. These improvements will result in an unprecedented luminosity of up to  $3 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ .

## 2. Motivation of Topological Trigger

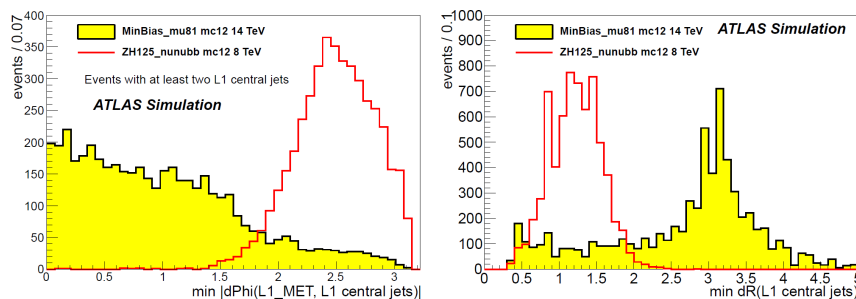


Figure 1: Comparison of the distributions of the minimum azimuthal angular distance  $\Delta\phi$  between MET and all central jets (left) and of the minimum radial distance  $\Delta R$  between central jets of the  $ZH \rightarrow \nu\bar{\nu}b\bar{b}$  decay (red) and background (yellow) [3]

To cope with this higher event rate and higher energetic background signals while keeping the Level-1 trigger rate below 100 kHz and maintaining yet a good efficiency for interesting events, it is necessary to upgrade the Level-1 trigger system along with the LHC during the LS1. Maintaining the given maximum Level-1 trigger rate without changes in the hardware would only be possible by increasing the energy / momentum thresholds of trigger objects. As such higher thresholds would reject rare events of interest as well, new trigger criteria have to be introduced to maintain efficiency. By evaluating the topological information, some interesting events can be distinguished by spatial correlations between decay products. As an example, the correlation in the azimuthal angular distance  $\Delta\phi$  and the radial distance,  $\Delta R = \sqrt{(\Delta\phi)^2 + (\Delta\eta)^2}$ , of the central jets of the decay

$ZH \rightarrow \nu\bar{\nu}b\bar{b}$  are shown in figure 1. For this case a cut of  $|\Delta\phi| > 1$  reduces the Level-1 trigger rate from  $\approx 10\text{kHz}$  to  $\approx 5\text{kHz}$ . Besides geometric cuts, further background reduction can be achieved by computing and cutting on kinematic variables, such as  $H_T = \sum p_T(\text{jets})$  or the invariant mass  $M = \sqrt{E_{T,1}E_{T,2}(\cosh(\Delta\eta) - \cos(\Delta\phi))}$ .

### 3. The Topological Processor

#### 3.1 The Topological Processor as part of the Level-1 Trigger Upgrade

While several modules of the Level-1 trigger system are facing upgrades, one of the major changes is the introduction of a new module in the trigger chain: the Topological Processor (L1Topo, see figure 2). It is intended to process the inputs from the Cluster Processor (photon/electron and tau cluster), from the Jet/Energy Processor (jets and MET) and the Muon CTP Interface [4] (muons). These sources need to be updated to deliver trigger objects (TOBs) with quantities like coordinates and energy. Therefore, the former merger modules of the Cluster Processor and the Jet/Energy Processor are substituted by newly developed modules (Common Merger Extended (CMX) [5]), which provide a higher output bandwidth.

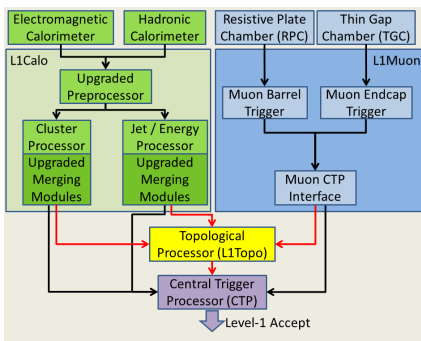


Figure 2: Outline of the Level-1 trigger system after the upgrade

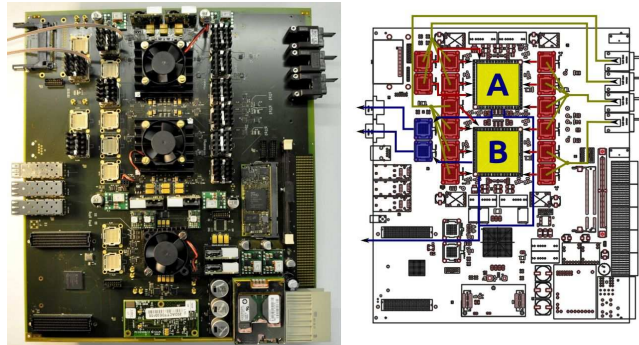


Figure 3: Photo of the first L1Topo module prototype and schematic overview of a L1Topo module and its real-time path (A,B: Processor FPGAs)

#### 3.2 Requirements and Implementation of the Topological Processor

To be able to provide the functions mentioned in section 2 it is necessary to evaluate the correlations of the trigger objects on the maximal possible number of combinations of these objects. This implies dividing the topological processor in as few as possible processing units (Processor FPGAs), therefore requiring a high input data bandwidth. Like the other Level-1 trigger modules, L1Topo is strictly limited in the time for receiving and processing the incoming data. Its latency budget is a maximum of 8 LHC bunch crossings, which is 200ns at the bunch crossing frequency of Run 2.

The Topological Processor consists of two identical AdvancedTCA modules (see figure 3), each supporting two Processor FPGAs. Chosen for the Processor FPGAs were Xilinx Virtex-7 690T-3 FPGAs providing 13.1 GBit/s on each of the 80 high-speed input channels [6]. The incoming data is transmitted by the sources on optical fibres at 6.4 GBit/s and converted into electrical signals in

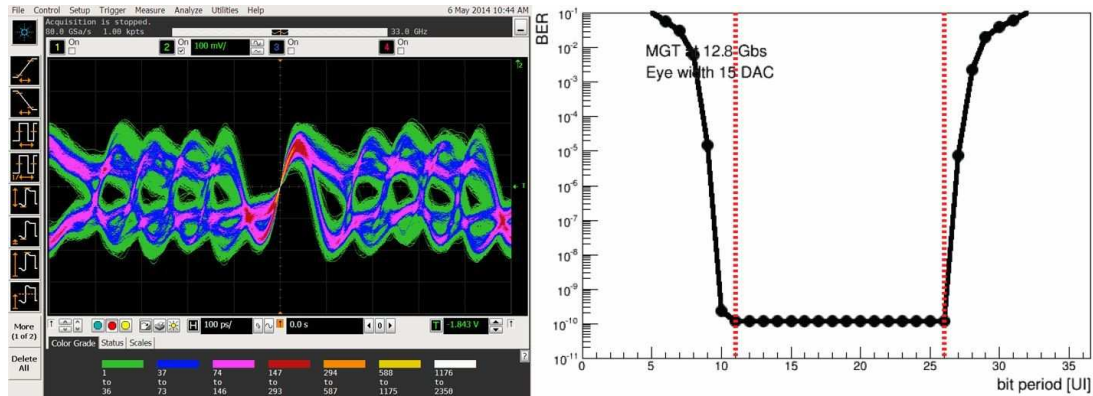


Figure 4: Eye-diagram and BER scan at 12.8 Gbit/s on a stand-alone L1Topo prototype module in a short measurement for demonstration purpose.

Avago MiniPODs, chosen because of their high spatial density and their low latency. Presently the processing of the data in the Processor FPGAs takes five LHC bunch crossings, after which the results of the L1Topo algorithms results are sent either optically or electrically to the CTP.

#### 4. Commissioning at CERN and Summary

Two fully functional prototypes of L1Topo modules have been manufactured and have been extensively tested for functionality (power, clock, configuration, ...). The high quality of the high-speed links at 6.4 Gbit/s between a CMX and a L1Topo module and the MUCTPI and L1Topo has been shown and tests of data transmission using the intended data formats are on their way. To explore the boundaries of the L1Topo design and for the research for future upgrades the reception of incoming data at 12.8 Gbit/s has been examined. Having a bit error rate (BER) of less than  $10^{-15}$  (no error was observed) a regular data transmission at this bit rate would be possible (see figure 4). The final L1Topo modules will be installed and commissioned at CERN at the end of 2014, being ready for Run 2.

#### References

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- [3] ATLAS Collaboration, *Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System*, <https://cds.cern.ch/record/1602235>
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