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Development of a Data Acquisition System for the Belle II Silicon Vertex Detector

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The silicon-strip vertex detector in the Belle II experiment is one of essential detectors to search for physics beyond the Standard Model. To read out all 223,744 readout strips of the double-sided silicon strip detectors in high beam background, 1748 APV25 chips are employed for the front-end electronics. Hence, flash analog-to-digital conversion with high-density inputs is required on the back-end electronics. We developed prototypes of the back-end electronics and successfully performed a full integration test at the DESY electron beam line. In this paper, we report on the development of the prototypes and results from the beam test.

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1. Introduction

Belle II [1] is an experiment to search for physics beyond the Standard Model with high statistics of B meson, D meson, and τ lepton decays. Belle II uses the SuperKEKB accelerator at KEK (Tsukuba, Japan) which employs a low-emittance collision scheme with electron and positron beams colliding at 7 GeV and 4 GeV, respectively, with a half crossing angle of 41.5 mrad. The designed luminosity of SuperKEKB is 8.0×10^{35} cm^{-2}s^{-1} which is the world-highest luminosity ever. Due to the high beam current and luminosity, the Belle II detectors have to be operated under high beam background and up to 30 kHz trigger rate.

The Belle II detector is a general purpose spectrometer. The innermost detector in the spectrometer is Vertex Detector (VXD) which plays an essential role to determine the secondary vertex positions of the weakly decay events. The VXD consists of inner DEPFET [2] Pixel Detector (PXD) and outer Silicon-Strip Vertex Detector (SVD). The SVD is comprised of four layers of Double-sided Silicon Strip Detectors (DSSDs) to measure the two-dimensional track positions in the four layers for charged particles. A track reconstructed from these measured positions together with outside tracker information gives us a Region Of Interest (ROI) [3] on the PXD which reduces the PXD data size and also provides a high-efficiency vertex determination.

From inner to outer, the four SVD layers are called as layer-3, layer-4, layer-5, and layer-6. The layer-3, 4, 5, and 6 consist of 14, 30, 48, and 80 DSSDs which are located on the radii of 38 mm, 80 mm, 104 mm, and 135 mm, respectively. A DSSD in layer-3 has 768 readout strips for each p-side (50 μm pitch) and n-side (160 μm pitch), and one in other layers have 768 readout strips for p-side (50-75 μm pitch) and 512 readout strips for n-side (240 μm pitch). As the result, signals from 223,744 strips in total have to be handled by the SVD readout system.

2. Development of Readout System of Silicon-Strip Vertex Detector

2.1 SVD readout system overview

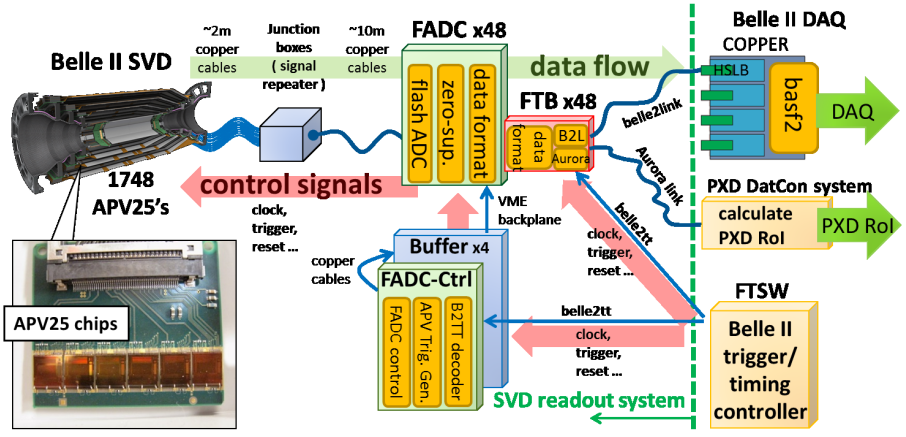


Figure 1: Schematic view of the SVD readout system.

Considering high beam background, a short shaping time is required for front-end electronics of the SVD readout system to reduce the hit occupancy. This requirement is satisfied by using the

APV25 front-end chip [4] which has a shaping time of 50 nsec. The APV25 has 128 input channels for DSSD signal. Therefore, 1748 APV25s in total are necessary to read out all the DSSD readout strips. Each channel of the APV25 has an analog pipeline of 192 cells and an FIFO of 32 samples depth, which stores pipeline addresses to be read at the trigger acceptance. In the SVD readout system, the APV25 is operated with a clock with 31.8 MHz frequency. Using the multi-peak mode of the APV25, where $3n$ ($n = 1, 2, ..., 10$) consecutive samples from the pipeline are read for each trigger acceptance, the signal profile can be reconstructed.

The APV25 restricts a maximum trigger rate to 38 kHz for the 6-sample mode and 76 kHz for the 3-sample mode, because the data transmission of the APV25 in the 6-sample mode and the 3-sample mode for each trigger takes 26.5 μsec and 13.2 μsec, respectively. The maximum trigger rate in the 6-sample mode is close to the designed Belle II maximum trigger rate of 30 kHz and then trigger dead time has to be considered. The 6-sample mode is preferable for effective peak finding, on the other hand it has a tighter requirement on the trigger rate compared with the 3-sample mode. The study of the trigger dead time in the SVD readout system is discussed in Sec. 4.

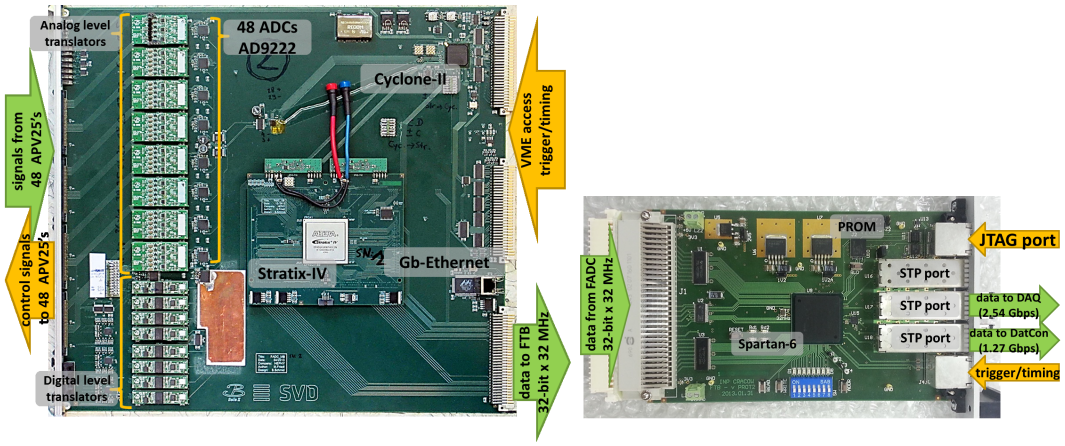
Figure 1 shows the concept of the whole SVD readout system. The analog outputs from the APV25s are transmitted to Flash Analog-to-Digital Converter (FADC) boards via repeater boards. The FADC board is a 9U VME module with a depth of 400 mm. The input density of the FADC board is maximized. As a result, an FADC board receives up to 48 APV25 analog outputs and performs flash analog-to-digital conversion with 31.8 MHz clock against these APV25 outputs to obtain digitized DSSD signals. The digital data are decoded on an FPGA, and propagated to Finesse Transmitter Board (FTB) through the backplane. The FTB is a 3U module with a depth of 160 mm. The FTB sends the data to the COmmon Pipelined Platform for Electronics Readout (COPPER) [5] which is a Belle II DAQ interface through an optical cable, using Belle II unified high-speed serial protocol (belle2link) [6]. In parallel, the FTB also sends a replica output to a PXD Data Acquisition Tracking Concentrator Online Node (DATCON) system [7] using Xilinx Aurora link. The DATCON system roughly reconstructs SVD tracks and provides ROIs for the PXD online. In the Belle II experiment, 48 FADC boards and 48 FTBs will be installed.

The control signals including clock, trigger, and reset signals from Belle II DAQ are provided using Belle II trigger/timing protocol (belle2tt) from Front-end Timing SWitch (FTSW) boards which are the Belle II trigger/timing controller. These control signals are distributed to all the FADC boards and APV25 chips by an FADC-Controller board via four buffer boards. The FTBs directly receives belle2tt signals from the FTSWs.

All the components other than the APV25 chips in the SVD readout system are being developed and the first prototypes for these components have been successfully produced and tested. In the following sections, the prototype development of the FADC board and FTB are explained.

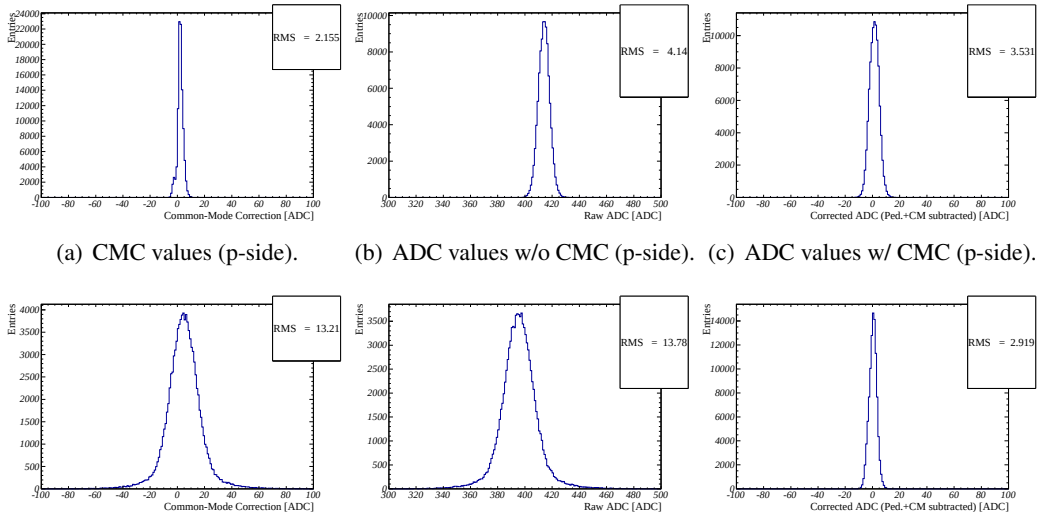
2.2 Prototype development of the FADC board

Figure 2(a) shows the developed prototype of the FADC board. At the first step of the data processing, analog levels of 48 APV25 signals are converted with capacitive couplers. These level-converted analog signals are digitized with eight ADC chips (AD9222) into 10-bit data and the data are sent to the main FPGA (Altera Stratix IV). In the FPGA, a Finite Impulse Response (FIR) filter is applied, and then the data are decoded to extract the ADC values of the DSSD signals. The data are transmitted to the FTB through the backplane with a data rate of 32 bits $\times$ 31.8 MHz.



(a) (b)

Figure 2: Prototype of the FADC board (a) and prototype of the FTB board (b).



(a) CMC values (p-side). (b) ADC values w/o CMC (p-side). (c) ADC values w/ CMC (p-side).

(d) CMC values (n-side). (e) ADC values w/o CMC (n-side). (f) ADC values w/ CMC (n-side).

Figure 3: Distributions of CMC values for p-side (a) and n-side (d), raw ADC values of noise before CMC for p-side (b) and n-side (e), and common-mode corrected ADC values of noise which are after subtraction of the pedestals and CMC values for p-side (c) and n-side (f).

Due to the large number of the total DSSD readout strips, a data-size reduction by zero-suppression is necessary. In the SVD readout system, the zero-suppression is performed by suppressing signals with ADC values less than threshold values which are determined from means (pedestals) and RMSs of noise distributions. However, a common-mode noise, which causes baseline-shift on the whole 128-channel outputs globally, has to be subtracted to correct the pedestal levels before the zero-suppression. This Common-Mode Correction (CMC) value is calculated in firmware as an average of ADC shifts from pedestals among the 128 channels except shifts above the thresholds. Figure 3 shows distributions of common-mode correction values for p-side (Fig. 3(a)) and n-side (Fig. 3(d)), ADC values of noise before the CMC for p-side (Fig. 3(b)) and

n-side (Fig. 3(e)), and common-mode-corrected ADC values of noise for p-side (Fig. 3(c)) and n-side (Fig. 3(f)). All these distributions are calculated in offline from obtained raw ADC data of noise without the CMC and zero-suppression. The distribution of the CMC values for p-side signals is rather narrower than the one for n-side signals, because a signal inverter applied only on the p-side APV25 also plays a role of the CMC and then the common mode noise in p-side is suppressed inside APV25. By applying the CMC in firmware, RMS of about 4.1 (p-side) and 13.8 (n-side) ADC counts in the raw ADC distributions can be decreased into about RMS of about 3.5 (p-side) and 2.9 (n-side) ADC counts in the common-mode corrected ADC distributions. The typical Most-Probable-Value (MPV) of the signal charge for the Minimum-Ionizing-Particle (MIP) is about 50-70 (p-side) and 60-80 (n-side) ADC counts. The noise RMS becomes well smaller than the signal height by applying the CMC.

The Belle II clock and trigger signals from the FADC-Controller board are received through the backplane. These signals are also distributed to all the APV25s connected on the FADC board using digital level translators of inductive couplers.

2.3 Prototype development of the FTB board

Figure 2(b) shows the developed prototype of the FTB. The data from the FADC board are directly sent to the FPGA (Xilinx Spartan-6). In the FPGA, the data are formatted and transmitted to the Belle II DAQ and DATCON system using Xilinx GTP cores. The bandwidths of the high-speed serial links are 2.54 Gbps for the DAQ and 1.27 Gbps for the DATCON system. The FTB has three SFP ports for the serial links including one spare port.

To confirm stability on these high-speed serial links, a communication test with two FTBs was performed. In the test, three SFP ports on one FTB were connected to three SFP ports on another FTB. On each of the three serial links between the two FPGAs, Pseudo-Random Bit Sequences with a 7-stage linear feedback shift register (PRBS-7) were transmitted with a data rate of 3.175 Gbps from both GTP transmitters and consistency of the received sequences was checked at both GTP receivers. As the result, no errors were observed during an 8-day long bench test with the two-FTB system. This result corresponds to 11 days of correct FTB data transmission with the final 48-FTB system in 95% confidence level, where 1 kB event size from an FADC board and 30 kHz trigger rate are assumed.

3. Beam Test at DESY

3.1 Introduction and experimental setup

An integrated SVD readout test was performed with the full prototype system using an electron beam at DESY (Hamburg, Germany). The energy of the electron beam was 2 to 6 GeV. On the electron beam line, four test SVD modules were installed in a light-shielding box. The four layers were assumed as the four SVD layers in the Belle II experiment, and then the same DSSD sensors were used. The four layers are also called as layer-3, 4, 5, and 6 from the beam upstream to the downstream. These layers were in parallel each other and in a direction perpendicular to the beam line. The distances from the layer-3 to the other three layers were 42 mm, 66 mm, and 97 mm, which are the same differences in radii of the SVD layers in the Belle II experiment. In the front of

the layer-3 and the rear of the layer-6, scintillator counters were installed for trigger signals. The setup box was placed in a superconducting solenoid magnet which applies magnetic field up to 1.0 T in a direction perpendicular to the beam line[1].

All the prototype components for the SVD readout system described in the previous section and components of the Belle II DAQ and DATCON system were setup at the experimental hall. Therefore, a same readout chain as the Belle II experiment was build up and it was a test of the full readout chain at the first time. The trigger rate was around 100-600 Hz.

3.2 Results

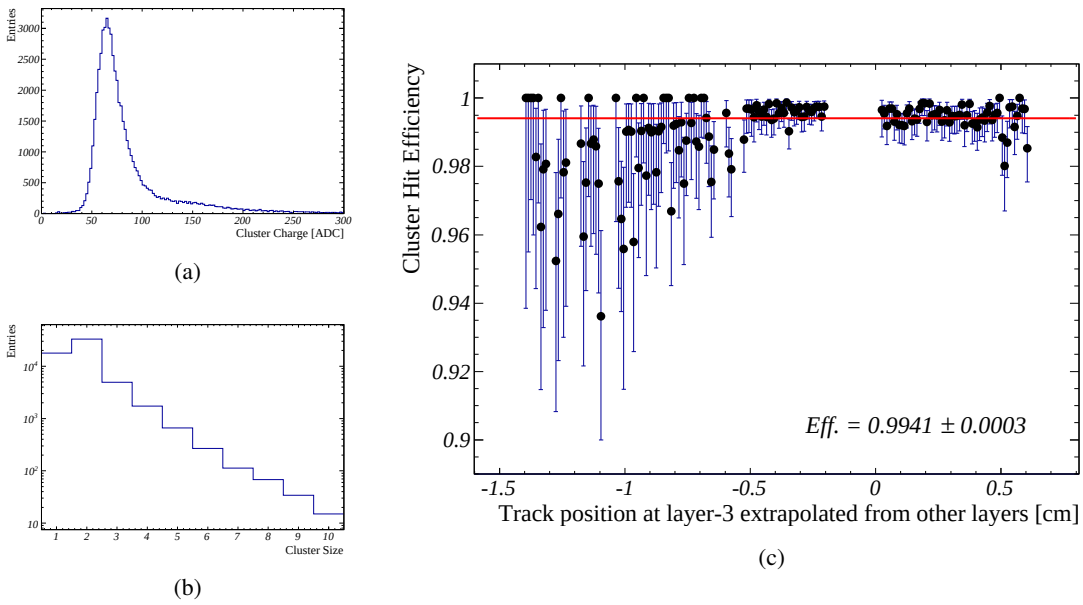


Figure 4: Distributions for cluster charges (a) and cluster sizes (b) on p-side signals from the layer-3 DSSD sensor. (c) Cluster hit efficiency of layer-3 p-side as a function of extrapolated track positions from other layers. The red line corresponds to the net cluster hit efficiency for all the fiducial area.

The correctness of the data processing on the electronics and data transmission to the Belle II DAQ and DATCON system is checked by the event number consistency and a Cyclic-Redundancy-Check (CRC) sum. As the result of these data quality checks, stable operation of the readout system during the beam test for about three weeks was confirmed.

The performance of the SVD modules was calculated from the obtained data to check the functionality of the readout system. Figures 4(a) and 4(b) show observed distributions of the cluster charges and cluster sizes on the p-side readout signal of the layer-3 DSSD. The MPV signal charge of the landau distribution corresponds to about 22,000 e. These results are well consistent with our expectation.

From positions of cluster hits on the layer-4, 5, and 6, an extrapolated positions on the layer-3 are calculated. Using the extrapolated positions, the cluster hit efficiency on the layer-3 was obtained. Figure 4(c) shows the result of the cluster hit efficiency in p-side. The horizontal axis

[1] All results in Sec. 3.2 are obtained from the data of 3 GeV electron beam without the magnetic field.

is the extrapolated position and the vertical axis is the cluster hit efficiency at the position. The missing area in the plot is due to a fiducial area cut which is related to known dead or hot strips and not related to the readout electronics performance. Resulting efficiency was 99.4% for all the fiducial area. From the obtained performance, an excellent functionality of the SVD readout system including the CMC and zero-suppression is confirmed.

4. Trigger Dead Time by SVD Readout System

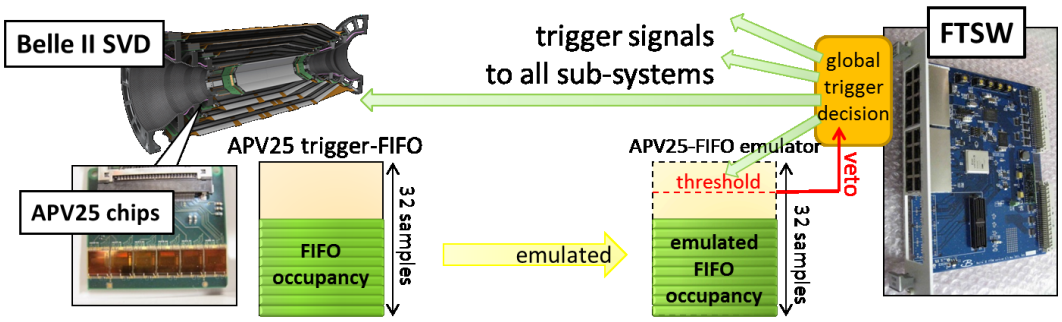


Figure 5: Schematic view of APV25-emulator implementation.

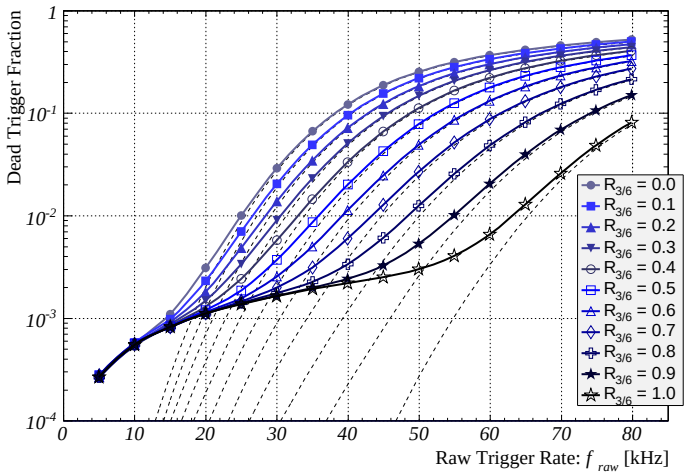


Figure 6: Trigger dead times from the APV25-emulator veto and minimum trigger interval of 189 nsec as functions of raw trigger rate. Various curves correspond to various fractions of 3-sample mode events $R_{3/6}$. The associations between the points and $R_{3/6}$ are indicated in the legend. See body text for more details.

As described in Sec. 2.1, data transmission of the APV25 in the SVD readout system takes a couple of 10 μsec for each trigger. These transmission dead times are absorbed by the FIFO in the APV25. However, the available FIFO depth is 32 samples, and then a back-pressure to avoid the FIFO overflow has to be implemented. For the back-pressure, an emulator for the APV25 FIFO occupancy (APV25-FIFO emulator) will be implemented on the master FSTW module, which performs a global trigger decision for all the Belle II sub-systems. Figure 5 shows the concept

of the APV25-FIFO emulator. The APV25-FIFO emulator calculates the FIFO occupancy, and if it advances to a threshold of 26 ($= 32 - 6$) samples, it asserts a trigger veto to the global trigger decision to stop the trigger and avoid the FIFO overflow in the APV25. Hence, the trigger dead time caused by the new veto system has to be studied before the implementation.

A simulation was performed with a minimum trigger interval of 189 nsec. The trigger dead times resulting from the APV25-FIFO emulator veto and the minimum trigger interval are shown in Fig. 6. The points of the filled circles are results from the 6-sample mode. The dashed line on these points represents the trigger dead time only from the APV25-FIFO emulator veto without the minimum trigger interval (set to 0). From the results, trigger dead time at the Belle II maximum trigger rate of 30 kHz is 3% which would be acceptable.

Furthermore, the trigger dead time can be decreased by introducing the 3-sample mode. To reconstruct the peak profile of the hit signal in the 3-sample mode, the peak timing has to be in the middle of the 3 samples. Therefore, the time resolution of the triggers for the 3-sample mode has to be enough less than the period of the 31.8 MHz clock (31 nsec). Hence, the 6-sample and 3-sample modes are switched event-by-event according to the time resolution of the accepted trigger which is provided by the FTSW [8]. The other various points in Fig. 6 are the results of the various fractions of the 3-sample modes, $R_{3/6}$. If $R_{3/6}$ can be increased to more than 0.7, 50 kHz trigger rate would be also acceptable.

5. Conclusion

The SVD readout system is being developed toward the start of the Belle II experiment. We developed the full chain of the SVD readout system with the prototypes. With the developed system, the successful integration test of the system was performed at the DESY electron beam line. We also studied the trigger dead time from the APV25-FIFO emulator, which will be implemented on the master FTSW in future. The resulting trigger dead time in 6-sample mode of the APV25 at 30 kHz trigger rate is 3% which would be acceptable, and it can be decreased if we introduce the 3-sample mode in a portion of events. As a conclusion, we confirmed that the system provides excellent performance for the Belle II SVD readout. For the future prospect, we will apply minor modifications on the FADC board and start the mass production in 2015.

References

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