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The TDCPix ASIC: Tracking for the NA62 GigaTracker

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The TDCPix is a hybrid pixel detector readout ASIC designed for the NA62 GigaTracker detector. The asynchronously operating pixel array consists of 1800 pixels, each 300x300 μm^2. The requirements are a single-hit timing resolution better than 200 ps RMS and a read-out efficiency of 99% or better in the presence of a beam rate between 800 MHz and 1 GHz. The discriminator time walk effect is compensated by time-over-threshold discriminators connected to an array of 360 dual TDC channels. The TDCpix processes up to 210 $Mhits/s$ and provides the hit data without the need of a trigger in a continuous data stream via four 3.2 Gb/s serialisers. Under test since January 2014, the TDCPix chip is fully functional and shows excellent performance.

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1. Introduction to NA62

The NA62 Experiment [1] is a fixed target experiment at CERN's SPS aiming to measure the branching fraction of the ultra-rare decay $K^+ \to \pi^+ + \nu\bar{\nu}$ ($O(10^{-10})$). The experiment comprises a 250 m long decay line into which a very intense (800 MHz→1 GHz) beam of p^+ (23%), K^+ (7%) and π^+ (70%) is sent. Only 10% of the K^+ will decay in the 60 m long fiducial region, with about 1 in 10 billion of these giving the final state under study. A RICH detector at the end of the beam line is designed to identify the π^+ from the decay, whilst the ν and $\bar{\nu}$ escape undetected. The experiment must match the π^+ with the K^+ from whence it came, and in order to do this, a high performance tracker has been designed: the GigaTracker (GTK).

2. Introduction to the GigaTracker

The GTK subdetector comprises 3 stations placed into the path of the beam before the fiducial region. Each tracking plane is made from a hybrid pixel detector (HPD) with a single detector element measuring 27x60 mm^2, thus instrumenting the full beam envelope. The detector is a P-on-N planar pixel detector 200 μm thick connected to two rows of 5 TDCPix chips by Pb-Sn bump bonds. The TDCPix chips abut along the centre of the detector and vertically between adjacent pairs giving full coverage with no dead area. The TDCpix chips extend beyond the edge of the sensor where all power and signal connections required by the chip must be made.

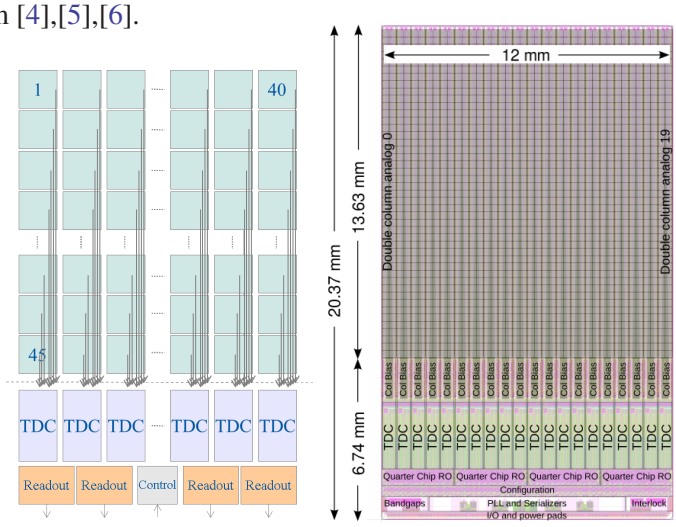
The GTK plane is situated in vacuum and hence must be bonded to an active cooling layer. A maximum material budget of less than 0.5 % X_0, corresponding to 480 μm of silicon, places stringent constraints on the technology that may be used. The TDCpix chips will be thinned to 100 μm, leaving approximately 180 μm for the cooling plates [2].

The sensor thickness was chosen as a trade-off between fast charge collection time and signal-to-noise ratio. The charge spectrum given by the sensor follows a Landau distribution with a most probable charge of 2.4 fC. In order to preserve the timing information in the signal, the detector must be biased at 300 V above full depletion (which occurs at approximately 20 V). The current pulse created by the charge liberated in the sensitive volume during the passage of a particle lasts about 5 ns. With this thickness and at this bias voltage, the expected fraction of hits that share charge up to the 10 % level is approximately 6 % for an angle of incidence of 50 mRad. This is not expected to degrade the time resolution significantly. Indeed, prior studies with both a high precision laser system and particle beam [3] have shown that fluctuations in the charge pulse from the sensor due to both the weighting potential and inhomogeneities in the column of charge, dominate the time resolution of the system. In the case of the former, at least, knowledge of where the charge was deposited due to charge sharing will lead to a potential improvement in the timing resolution since the time walk correction can be adjusted to take the weighting potential into account, however, this has yet to be demonstrated experimentally.

3. Introduction to the TDCpix ASIC

The TDCPix ASIC comprises an asynchronously operating pixel array of 1800 pixels organised into 40 columns of 45 rows, connected to an End-Of-Column (EOC) time-stamping and hit

processing unit. Figure 1 (a) shows an overview of this architecture and 1(b) an annotated screen shot of the layout. Each pixel measures 300x300 μm^2. The pixels do not receive any timing reference signal, instead the discriminated hit signals are driven to the EOC region using a dedicated hit signal per pixel. The front-end amplifier has been designed with a peaking time of approximately 5 ns. This matches the detector characteristics, permitting the signal to be fully integrated whilst preserving the timing information. The stochastic nature of the charge release mechanism results in a charge dependent slew rate at the pre-amplifier output, the magnitude of which for the given architecture over the charge range of interest is of the order of 2-3 ns peak to peak. To time stamp at the $O(100\,ps)$ level, a discriminator time-walk correction mechanism is necessary. As the time over threshold is a monotonic function of the charge, a look-up table (LUT) is used to estimate a correction to the leading time based on the time-over-threshold measured on an event-by-event basis. This correction is effected off-detector. The approach was evaluated with a small-scale demonstrator system [4],[5],[6].



(a) Architectural summary (b) Layout Screen-shot

Figure 1: The TDCPix Chip architecture summary and layout

The hit signals sent from the pixel to the EOC region are received first by some arbitration circuits that map five pixel channels to a single TDC channel. The first active pixel in a group blocks the hit arbiter and any subsequent hits occuring whilst this hit is being processed are latched as pile-up events. This approach permits the number of TDC channels to be reduced to 360, with each channel providing one leading edge and one trailing edge measurement for each hit. The hit arbiter is an asynchronous circuit that fully preserves the timing information of the hit signals from the matrix.

The TDC [7] has a nominal bin size of 97 ps. This is generated by a Delay-Locked Loop (DLL) containing a delay line with 32 contributing delay elements locked to a 320 MHz high-precision reference clock. Upon the arrival of a hit from the hit arbiter, the state of the 32 signals from the DLL is latched into a register array. The position of the edge within this array gives the time of the event relative to the reference clock signal. This position is encoded into a 5-bit binary number using a combinatorial logic block. The second stage of the TDC is provided by a 12-bit coarse time, from a Gray encoded binary counter. This extends the range of the TDC to 6.4 μs. A full time stamp is built from the fine time codes for the leading and trailing edges, the coarse

time of the leading edge trigger, a coarse time-over-threshold, the pixel address, and any pile-up information. Each of the 360 channels has a FIFO buffer for hit derandomisation. The data from nine such buffers are merged into a single column FIFO.

The TDCpix chip is organised into four quarter chips, each of which operates independently, containing a data concentration block, named the QChip, and a high-speed serialiser running at $3.2\,Gb/s$. Thus the data from ten columns are merged into a single data stream. The QChip additionally provides the generation of a frame word containing a 28-bit counter that increments each time the TDC coarse counter wraps. This extends the TDC dynamic range to just over 1700 s.

As the ASIC will be placed in a relatively harsh radiation environment, all state and configuration registers have been triplicated. In the end of column region, the schemes use free running clocks, whereas in the pixel matrix, a combinatorial SEU error indicator is propagated to the end of column region, where it can be monitored by the off detector electronics.

The TDCpix chip was designed in a $130\,nm$ commercial CMOS process, and manufactured during the latter part of 2013. Chips became available for testing at the beginning of December 2013 and have been under test since January 2014. A photo of the chip bonded to the test system is shown in Figure 2. No bugs have been detected so far and a re-spin of the design is currently not anticipated. Consequently, sensor assemblies are being bump bonded at the time of writing and delivery is expected at the end of June 2014.

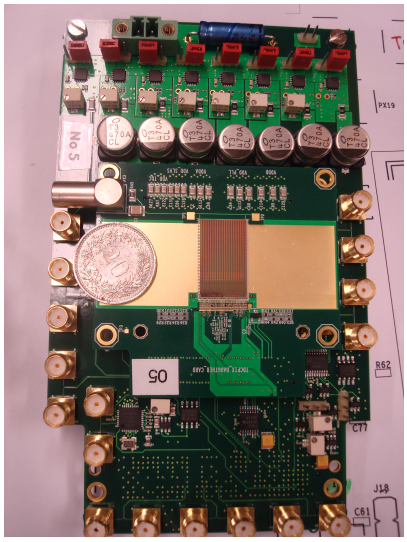


Figure 2: The TDCPix Chip bonded to the test card.

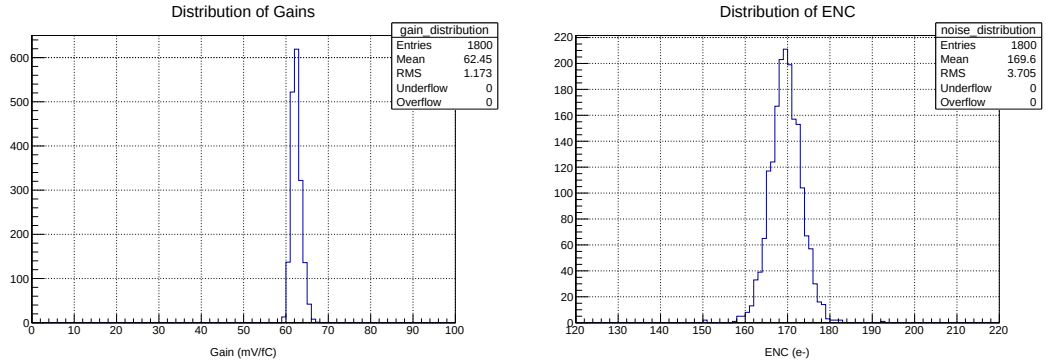
4. Measured Performance

4.1 Introduction

The TDCPix chip is equiped with several test mechanisms that permit the independent testing of key components in the chip. In the absence of the sensor to provide a charge signal, test charges may be injected in the front end via a charge-injection capacitor with a nominal capacitance of $21.5\,fF$. The voltage step is generated on-chip, is of programmable amplitude, and is triggered by an external digital trigger signal and thus may either be synchronised or not with the TDC reference clock. Two of the hit signals at the end of column are connected to test pads permitting indirect observation of the discriminator hit signals. As these test signals originate after the hit arbiter, all five of the pixels driving the inputs may be examined, albeit individually. The hit arbiters have a test input allowing the TDC to be triggered from the external trigger signal directly, thus bypassing the pixel array and permitting an independent characterisation.

4.2 Pixel Performance

Gain and noise measurements were made on the pixel array using a standard "S-Curve" methodology. The measured cummulative distribution function is then fitted to extract the properties of the pulse height distribution. From the measurements of different charges, the transfer function can be extracted, and from this the front-end amplifier gain. Once the gain is known the width of the pulse height distribution can be referred to the input of the pre-amplifier, giving the equivalent noise charge.



(a) Distribution of Pixel Front-End Gains

(b) Distribution of ENC

Figure 3: Gain and ENC distributions for a complete array of 1800 pixels.

A drawback of this method is that the noise contribution from the charge injection circuit is included in the measurement. This can be avoided by sweeping the threshold into the pedestal, however for a self-triggering system a mechanism to normalise the triggers is required and the TDCPix chip does not have this functionality.

Figures 3 (a) and (b) show the gain and ENC distributions respectively measured across a complete 1800 pixel array. Note that these measurements were made on a bare ASIC, so the ENC does not include the contribution from the sensor. The total noise budget for the system will permit an ENC up to $250\,e^-$. The measured gain distribution is narrow and within a 5 % of the design value of $65\,mV/fC$. The measured offsets were compensated for using the in-pixel trimming mechanism, permitting measurements to be made at a fixed threshold for all pixels. Using the test output connected to a high-performance digitising oscilloscope, a measurement of the pixel timing performance was made as a function of input charge and for several different thresholds, with the results shown in Figure 4. The shape of the curves reflects the gradient of the pre-amplifier output at the point at which it crosses the discriminator threshold.

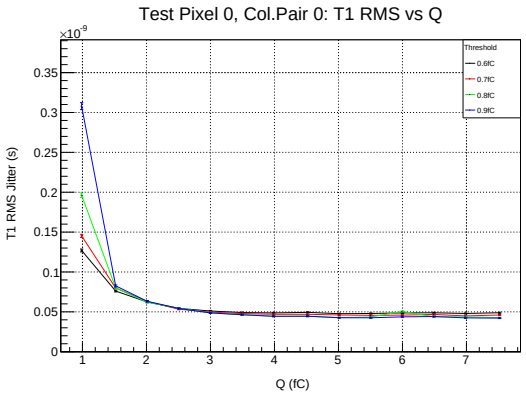
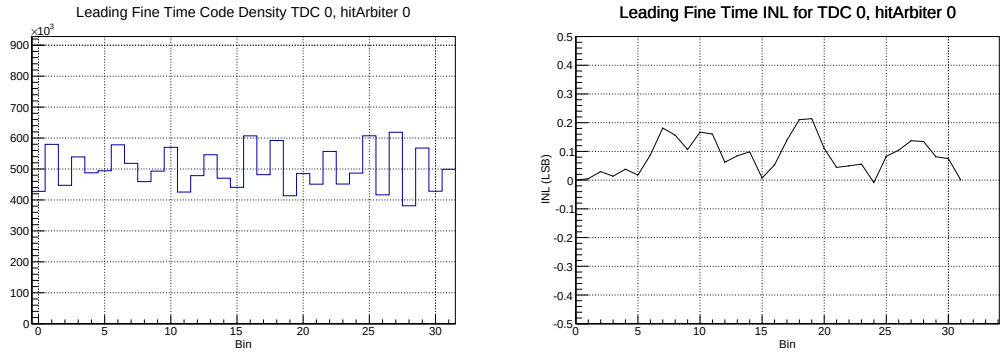


Figure 4: RMS pixel jitter measured using an oscillioscope as a function of injected charge for threholds at 0.6, 0.7, 0.8 and 0.9 fC.

Since a lower charge results in a lower pre-amplifier output slew rate, the noise present on the signal has a longer lever arm to translate the noise signal into the time domain. This can be clearly seen as a turn up of the curves at low charges. The effect is exacerbated if the threshold is set higher, and this is also clearly visible in the curves. Above the 2.4 fC most probable charge expected from the sensor, the RMS jitter is better than 60 ps. Note that this value contains contributions from many different sources, namely: the trigger distribution circuit; the charge generation circuit; the transmission lines bringing the signal to the end of column; the hit arbiter and the test signal buffering in the end of column. The contributions from the scope and pulse generator are estimated to be less than 30 ps (RMS).

4.3 TDC Performance

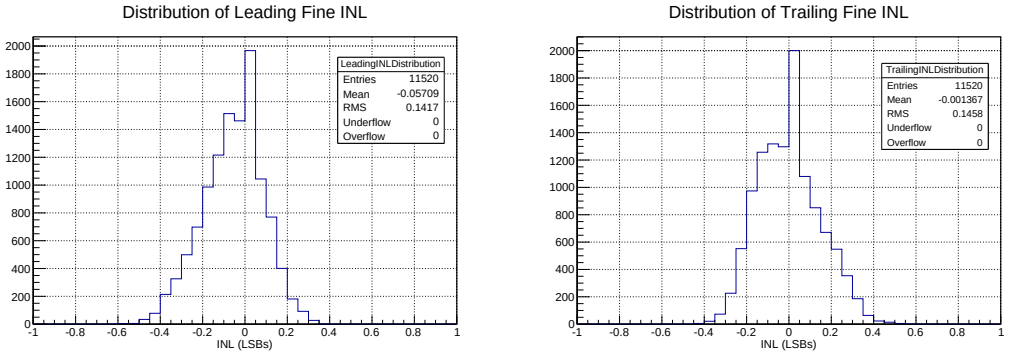
The TDC linearity was measured using un-synchronised triggers to perform a statistical code density test. A reasonably large number of triggers ($1.6\text{x}10^7$) was collected and fine time code was histogrammed.



(a) (b)

Figure 5: An example code density histogram (a) and corresponding integral non-linearity curve (b).

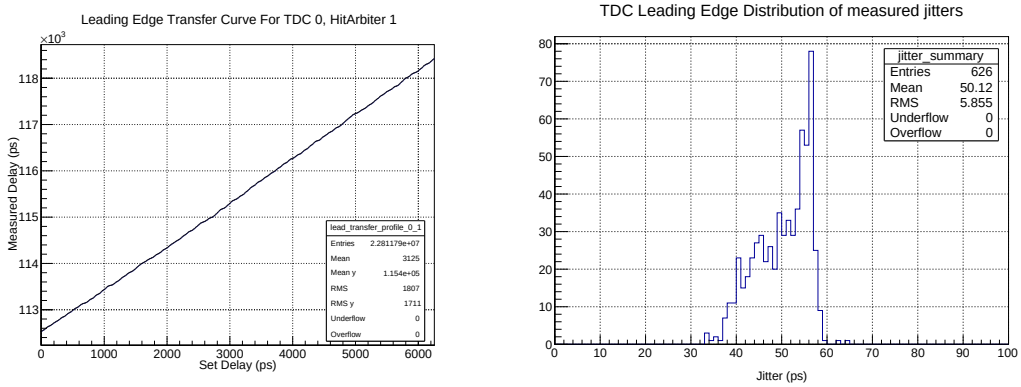
An example of such a distribution is shown in Figure 5 (a). With sufficiently large statistics, the bin content as a fraction of the total number of triggers approximates the bin width as a fraction of the reference clock period.



(a) (b)

Figure 6: Summary histograms for the INLs of the leading (a) and trailing (b) TDC channels for a complete chip.

From the bin widths the transfer function can be calculated, and from this, the non-linearities. Figure 5 (b) shows the integral non-linearity (INL) for the channel in question. To try to summarise the behaviour of the chip as a whole, a histogram of all the INL points was made across all channels in the TDCPix chip. These distributions are shown for the leading and trailing hit register channels in Figures 6 (a) and (b) respectively. The RMS INLs are typically 0.15 Least Significant Bits (LSBs, where a LSB is $\sim$97 *ps*). This remains at a level where a per-channel correction to the INL is unnecessary, simplifying the usage of the chip.



(a) Delay reported by the TDC as a function of the delay set on the pulse generator spanning two reference clock cycles.

(b) The distribution of RMS jitters.

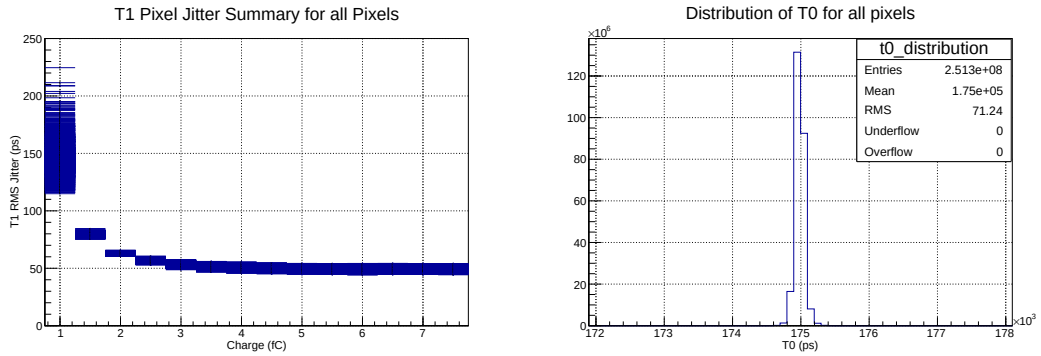
Figure 7: Summary plots of the TDC performance.

The TDC resolution was measured by synchronising the pulse generator to the TDC reference clock generator and sweeping the time of the trigger pulse through the clock period in steps of 10 *ps*, collecting 3x10^4 hits per position. Figure 7 (a) shows the delay reported by the TDC as a function of the delay set in the pulse generator. The monoticity of this curve indicates that the full time stamp is being correctly reconstructed. Each point on this curve is a (vertical) histogram with 3x10^4 entries. The standard deviations of all these points are summarised in Figure 7 (b), including the TDC quantisation error. The most probable value (mode) is 56 *ps*.

4.4 Full Chain Performance

Figure 8 (a) shows the RMS pixel jitter measured as a function of the charge injected at the front end for all pixels measured by the TDCs within the TDCPix chip. The RMS jitter is better than 65 *ps* for charges above 2.4 *fC*. This measurement does not contain the discriminator time-walk correction necessary to achieve the measurement resolution required from the chip.

Figure 8 (b) shows the discriminator time-walk corrected time, termed T_0, as measured for all pixels and charges. In order to make this measurement, a calibration data set was taken from which a separate LUT for each pixel was filled. A second, statistically independent, measurement data set was then taken. For each time stamp from this second data set, the corrected time was calculated using a continuous parameterisation of the time-walk correction LUT. The resulting distribution has a standard deviation of just over 70 *ps*. This can be termed a "resolution" because the time walk has been corrected for, however, it must be noted that this is an "electronics" resolution, since all charges have been given equal weighting, which will not be the case with the sensor.



(a) (b)

Figure 8: (a) Leading edge RMS discriminator jitter measured by the TDC as a function of charge. (b) Time-walk corrected electronics resolution across all pixels and all charges.

5. Summary

The NA62 experiment requires a tracker capable of processing $800\,MHz \rightarrow 1\,GHz$ hits whilst timestamping with a precision of better than $200\,ps$ RMS per station. A hybrid pixel readout chip for this tracking detector was designed comprising a matrix of 1800 pixels, operating asynchronously. High precision, per-pixel, discriminator hit signals are driven to the end of column region where both the leading and trailing discriminator edges are timestamped to approximately $97\,ps$. A time-over-threshold approach to correct for the discriminator time-walk has been adopted, with off-detector LUTs effecting the correction off-line. The readout is done via four serialisers, each running at $3.2\,Gb/s$. The TDCPix chip became available for testing at the end of 2013. All functionality has been tested and no bugs have been discovered. The front-end gain is measured to be $62.5\,mV/fC$ with a spread of $1.2\,mV/fC$, compared to the design gain of $65\,mV/fC$. The ENC in the absence of the sensor is measured to be $170\,e^-$ on average across a whole pixel array. The pixel jitter measured with a high performance oscilloscope is better than $60\,ps$ RMS above the most probable charge of $2.4\,fC$. Measurements of the TDC performed independently of the pixel array indicate a RMS INL of 0.15 LSBs, and a resolution of $60\,ps$ RMS. The full chain RMS jitter was measured to be better than $65\,ps$ above $2.4\,fC$. A calibration data set was acquired for all pixels in the matrix and a time walk correction look-up table extracted for each pixel. Applying this correction to a second independent data set yields an electronics resolution of just over $70\,ps$ RMS for all pixels and charges.

References

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