Vertex-Detector R&D for CLIC

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A detector concept based on hybrid pixel-detector technology is under development for the CLIC vertex detector. It comprises fast, low-power and small-pitch readout ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin sensors (planar or active HV-CMOS) via low-mass interconnects. The power dissipation of the readout chips is reduced by means of power pulsing, allowing for a cooling system based on forced air flow. In this contribution the CLIC vertex-detector requirements are reviewed and the current status of R&D on readout and sensors is presented.

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1. Introduction

The proposed Compact LInear Collider (CLIC) concept of a linear electron-positron collider with a centre-of-mass energy of up to 3 TeV has a large physics potential, complementing and extending the measurements of the LHC experiments [1, 2, 3]. The demands for precision physics in combination with the challenging experimental conditions at CLIC have inspired a broad detector R&D program. In particular the vertex-detector systems have to fulfil unprecedented requirements in terms of material budget and spatial resolution in a location close to the interaction point, where the rates of beam-induced background particles are very high. The ongoing CLIC vertex-detector studies focus on ultra-thin hybrid pixel detectors and aim for integrated solutions taking into account constraints from mechanics, power delivery and cooling.

2. Vertex-detector requirements

The primary purpose of the CLIC vertex detector is the efficient tagging of heavy quarks through a precise determination of displaced vertices. Monte Carlo simulations show that these goals can be met with a high-momentum term in the transverse impact-parameter resolution of $a \approx 5\mu$m and a multiple-scattering term of $b \approx 15\mu$m, using the parametrization

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \text{GeV}^2/(p^2 \sin^3 \theta)}, \tag{2.1}$$

where p is the momentum of the particle and θ is the polar angle with respect to the beam axis. These requirements on the measurement precision exceed the results achieved in any of the currently existing full-coverage vertex systems. They can be met with multi-layer barrel and endcap pixel detectors operating in a magnetic field of 4-5 T and using sensors with a single-point resolution of $\approx 3\mu$m and a material budget at the level of $< 0.2\%$ of a radiation length (X_0) for the beam-pipe and for each of the detection layers. The single-point resolution target can be met with pixels of $\approx 25\mu$m $\times$ 25μm and analog readout.

The time structure of the collisions at CLIC severely constrains the vertex-detector technology choices. Bunches of particles collide every 0.5 ns during only 156 ns train duration, followed by 20 ms gaps between bunch trains. Time slicing of hits with an accuracy of ≈ 10 ns will be required to separate physics events from beam-induced backgrounds occuring within the same bunch train.

The material-budget target corresponds to a thickness equivalent to less than 200 μm of silicon, shared by the active material, the readout, the support and the cooling infrastructure. This implies that no active cooling elements can be placed inside the vertex detector. Instead, cooling through forced air flow is foreseen. This limits the maximum power dissipation of the readout to ≈ 50 mW/cm^2. Such low power consumption can be achieved by means of power pulsing, i.e. turning off most components on the readout chips during the 20 ms gaps between bunch trains.

The radiation exposure of the vertex detector is expected to be small, compared to the corresponding regions in high-energy hadron-colliders [4]. For the non-ionizing energy loss (NIEL), a total neutron-equivalent fluence of less than 10^{11}n$_{eq}$/cm^2/year is expected for the inner barrel and forward vertex layers. The simulation results for the total ionizing dose (TID) predict approximately 200 Gy/year for the vertex-detector region.

2.1 Vertex-detector concepts

Vertex-detector concepts meeting the CLIC requirements are under development. They are optimized for low readout occupancies [4] and for high flavor-tagging performance [5]. The resulting detector layouts contain 3 double pixel layers or 5 single layers both in the barrel and forward-disk region, operated in a magnetic field of 4-5 T. The pixel size is $25\mu\text{m} \times 25\mu\text{m}$. The coverage extends to low polar angles ($7° < \theta < 173°$). The inner radius of approximately 30 mm is constrained by direct hits from beam-induced backgrounds. The beam pipes include conical portions in the forward and backward directions consisting of stainless steel with a wall thickness of 4 mm. These provide shielding against backscattering upstream and downstream backgrounds. The resulting total background occupancies do not exceed a few percent in the innermost layers. The total pixel-detector area is approximately 1 m^2, corresponding to 2G pixels. Figure 1 (a) shows a view of the inner tracking region in a detector layout for CLIC.

Refined engineering and simulation layouts of the vertex-detector region take into account constraints from detector integration and assembly. A staggered arrangement of the forward disk layers (Fig. 1 (b)) allows for cooling through forced air flow [6].
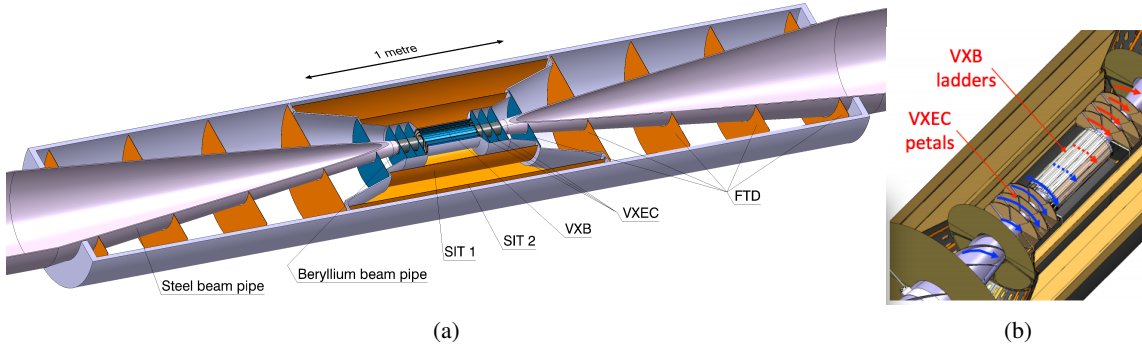

Figure 1: (a) View into the inner and forward tracking region of the CLIC_ILD simulation model. Shown are the vertex barrel (VXB) and endcap (VXEC) pixel layers, the two inner silicon barrel strip layers (SIT 1/2), the forward tracking disks (FTD), the beam pipe, and the support shells for the silicon layers. (b) View into the inner region of a refined engineering model for the CLIC_ILD vertex detector. Shown are the vertex barrel (VXB) and endcap (VXEC) pixel layers. The curved arrows indicate the foreseen stream of air for the cooling of the detector.

3. Hybrid readout technology

The R&D on pixel sensors and readout is focused on hybrid solutions, combining high-resistivity sensors (planar or active HV-CMOS) with high-performance readout ASICs. The target thickness for both the sensor and readout layers is only 50 μm each. Slim-edge sensor designs are under study and Through-Silicon Via (TSV) technology is foreseen for vertical interconnection. The hardware R&D on sensors and readout is complemented by TCAD [7] silicon simulations and Geant4-based detector simulations [8], to evaluate the impact of the technological parameters on the detector performance under various operating conditions.

Table 1: Comparison of simulated and measured parameters of the CLICpix demonstrator chip. All measurements were performed on chips from the same wafer. Values labeled with * are obtained assuming a nominal value of 10 fF for the test capacitor.

Parameter	Simulated Value	Measured Value
Rise time	50 ns	-
ToA accuracy	< 10 ns	< 10 ns
Gain	44 mV/ke^- $\pm 20\%$	40 mV/ke^-
Dynamic Range	up to 40 ke^-	up to 40 ke^- *
Integr. nonlinearity (TOT)	< 0.5 LSB	< 0.5 LSB
Equivalent Noise (bare chip)	$\sigma = 60e^-$	$\sigma = 55e^-$ (average) *
DC Spread (uncalibrated)	$\sigma = 160e^-$	$\sigma = 128e^-$ *
DC Spread (calibrated)	$\sigma = 24e^-$	$\sigma = 22e^-$ *
Minimum threshold	388 e^-	417 e^- *
Power consumption per pixel	6.5 μW	7 μW

3.1 CLICpix readout chip

The CLICpix hybrid readout chip [9] will be implemented in a 65 nm CMOS process. The pixel size is 25 μm$\times$25 μm. Simultaneous 4-bit Time-Of-Arrival (ToA) and Time-Over-Threshold (ToT) measurements are implemented in each pixel, allowing for a front-end time slicing with approximately 10 ns and for measuring the charge to improve the position resolution through interpolation. A photon counting mode allows for threshold equalization. A compression logic is implemented with three selectable readout modes: (1) no compression; (2) pixel-to-pixel compression; (3) pixel-, cluster- and column-based compression. The full chip can be read out in less than 800 μs (for 10% occupancy), using a 320 MHz readout clock. The power consumption of the chip is dominated by the analog frontend with a peak power corresponding to 2 W/cm^2. The total average power consumption can be reduced to a value below the target of 50 mW/cm^2 by means of power gating for the analog part and clock gating for the digital part.

A CLICpix demonstrator chip has been produced in 65 nm CMOS technology, including a 64×64 pixel matrix and power-pulsing capability. Readout tests have confirmed that the chip is fully functional and the power consumption and performance are in agreement with simulations [10]. The front-end wake-up time was estimated to be less than 15 μs, allowing for a reduction of the average power consumption by more than a factor 100 through power pulsing. An irradiation test showed radiation hardness of the chip up to a dose of 250 MRad.

Table 1 summarizes the results of the characterisation measurements and compares them to the expectations from simulations. Very good agreement between measurements and simulations is observed.

3.2 Thin-sensor assemblies

Planar pixel sensors with 55μm pitch and different thicknesses (50-300 μm) were procured from Micron Semiconductors [11] and from Advacam [12]. Assemblies with Timepix readout ASICs (100 and 450 μm thickness) were produced by IZM [13] and by Advacam and characterised

in laboratory measurements and in beam tests with the EUDET telescope in the DESY II electron beam. Slim-edge sensor designs (250-450 μm, two guard rings) are compared to designs with active edges (20-50 μm, one guard ring above the edge pixels).

Preliminary results show very good efficiencies in both cases, extending beyond the edge pixels. Figure 2 (a) shows the efficiency for observing hits in a 100 μm thick sensor coupled to a 100 μm thinned Timepix readout ASIC, for different settings of the energy threshold. Efficiencies are not corrected for inactive regions. The observed efficiency is above 99% for the operating energy threshold of 380 DAC counts.

Single-point resolutions have been extracted for various cluster sizes using charge interpolation and taking into account non-linear charge sharing. Figure 2 (b) shows the residual distribution for two-hit clusters in a 50 μm thick sensor with 20 μm wide active edges, coupled to a regular Timepix readout ASIC. The data was obtained with electrons of 5.6 GeV momentum. The observed resolution is 4.6 μm. This includes the track-prediction resolution of the telescope of 3.2 μm. Unfolding of the telescope resolution yields a single-point resolution of 3.3 μm for this assembly.

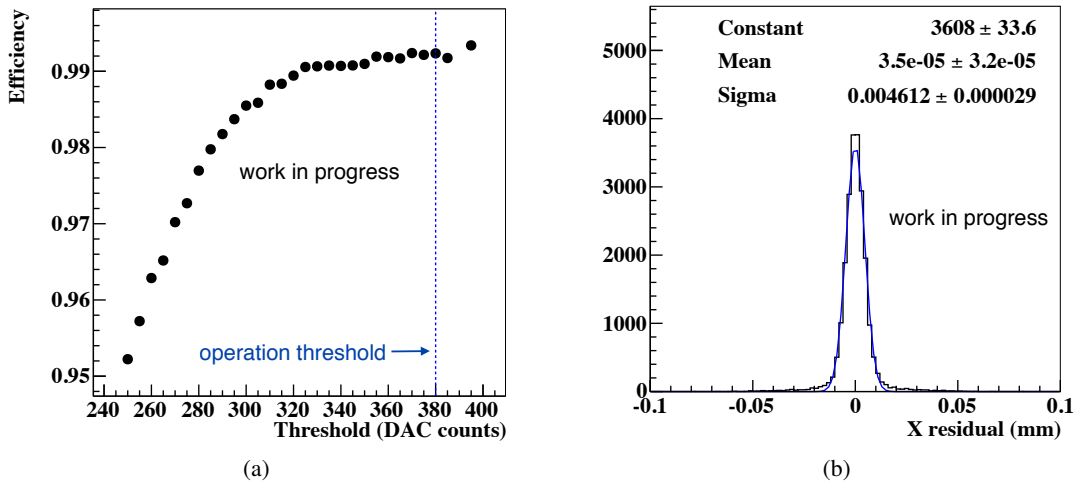(a)   (b)

Figure 2: (a) Detection efficiency as a function of energy threshold setting for a 100 μm thick sensor coupled to a 100 μm thinned Timepix readout ASIC. (b) Residual distribution for two-hit clusters in a 50 μm thick active-edge sensor coupled to a regular Timepix readout ASIC.

3.3 HV/HR-CMOS active sensors

An alternative sensor concept for the CLIC vertex detector is currently under study. It is based on active CMOS sensors with capacitive charge coupling to separate readout ASICs [14]. A depleted drift region under the signal collecting diode is created by either using a high-voltage CMOS process or by backside biasing of a high resistivity bulk material. The HV/HR-CMOS technology has the potential for ultra-thin sensors with large and fast signals, flexible readout granularity, sufficient radiation hardness and cost-effective detector integration.

Prototypes of Capacitively Coupled Pixel Detectors (CCPD) have been produced in the AMS H18 180 nm HV-CMOS process. The CCPDV3 prototype contains a 64x64 pixel array with 25 μm

pitch, matching the footprint of the CLICpix demonstrator readout ASIC. Each pixel contains a two-stage amplifier connected to a metal readout pad on the top (Fig. 3 (a)). A coupling capacitance of a few femtofarad per pixel between sensor and readout ASIC is achieved through a thin layer of glue (approximately 5-10 μm) between the two chips. Figure 3 (b) shows one of the produced CLICpix-CCPDV3 assemblies. The readout setup for these assemblies is currently in production.
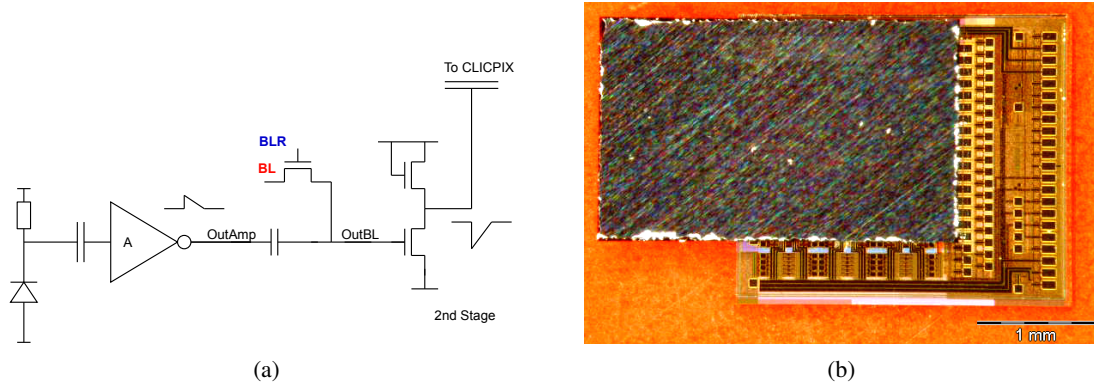

Figure 3: (a) Schematics of the two-stage amplifier for the CLICpix pixels inside the CCPDV3 chip. (b) Photo of a CCPDV3-CLICpix assembly, with the CCPDV3 front side mostly covered by the back side of the CLICpix demonstrator ASIC on the left.

Preliminary calibration measurements have been performed using test output connections of the CCPDV3 CLICpix amplifiers. Figure 4 shows the spectrum obtained for a ^{55}Fe source. The Kα and Kβ absorption lines can clearly be dinstinguished. A resolution of approximately 30 e$^-$ is observed for the Kα peak at 1.6 ke$^-$. The noise was measured to correspond to an ENC of 35 e$^-$.
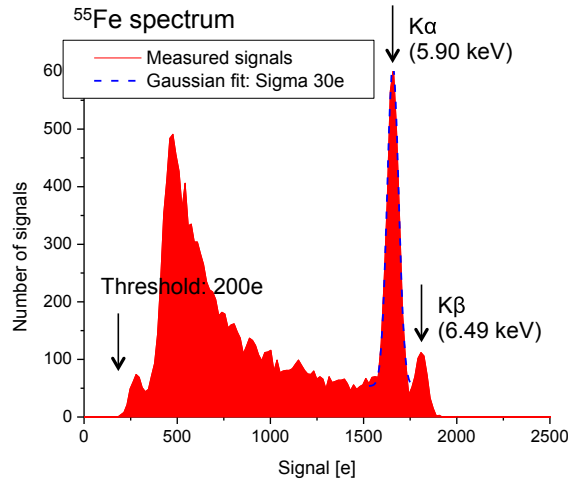

Figure 4: ^{55}Fe spectrum observed on the CLICpix amplifier test output of the CCPDV3 chip with a bias voltage of 35 V, from [15].

4. Conclusions

The CLIC machine environment and the requirements for precision physics measurements

place challenging demands on the vertex-detector systems. Initial detector layouts meeting these demands have been proposed and are currently being refined in line with results from detector-optimisation and hardware development studies. An R&D program on sensor and readout technologies is in place, focussing on hybrid solutions with ultra-thin planar or active CMOS sensors coupled to high-performance ASICs implemented in 65 nm technology.

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