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# 128 channel waveform sampling digitizer/readout in the TOP counter for the Belle II upgrade

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Extremely fast Micro-Channel Plate PhotoMultiplier Tubes (MCP-PMTs) and multi-gigasample per second (GSa/s) waveform sampling ASICs will allow precision timing to play a pivotal role in the next-generation of Ring Imaging Cherenkov (RICH) detectors. We have developed a second prototype of the electronics to instrument the Time of Propagation (TOP) counter for the Belle II detector at KEK in Tsukuba, Japan. The front-end electronics modules consist of an array of waveform sampling / digitizing ASICs controlled by FPGAs with embedded microprocessor cores. The ASICs digitize amplified signals from an array of multi-anode MCP-PMTs coupled to a quartz radiator bar. Online feature-extraction is performed directly on the front-end via digital signal processing. Readout and control are done via multi-gigabit per second fiber optic links to a custom back-end.

A previous generation of these modules has been running in a prototype Focusing Detection of Internally Reflected Cherenkov (FDIRC) counter mounted in a Cosmic-Ray Stand (CRT) at SLAC continuously for over 12 months. The most recent version was taken to a beam test at the LEPS experiment at the Japanese SPring-8 facility in mid-2013. These experiences have influenced the design of the next set of ASICs and PCBs for the front-end.

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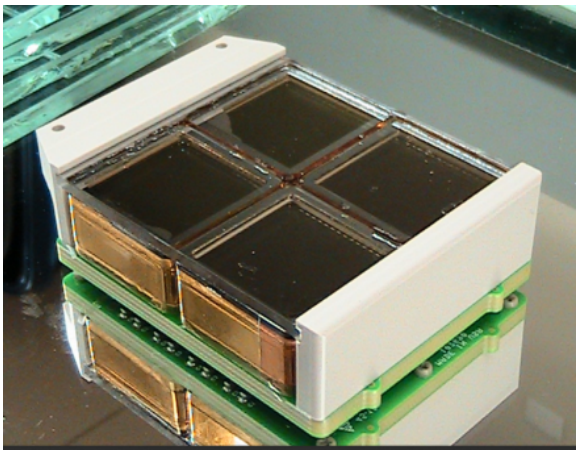
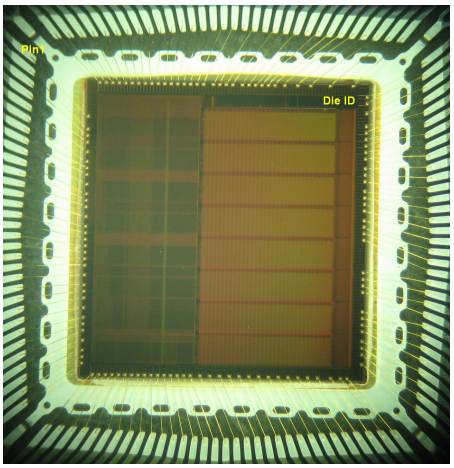


(a) four MCP-PMTs on a PCB. They are mounted with a pitch of 28 mm.




(b) 8 channel multi-GSa/s Ice Radio Sampler (IRS) ASIC with deep storage.

Figure 1: key components for the TOP counter's perfomance

## 1. Introduction

The Belle detector was built to study rare decays in the B meson system. Belle operated at the KEKB asymmetric electron/positron accelerator for 10 years and collected data from decays of more than 770 million $B\bar{B}$ pairs. Belle II is an upgrade to most of its systems' sensors and the electronics that read them out[1].

SuperKEKB is an upgrade to the KEKB facility that will deliver higher instantaneous luminosity both by increasing the beam currents, as well as by focusing the intersecting beams to a much smaller cross-section. One of the consequences of this higher luminosity is that the sensors and readout systems must cope with much higher background radiation during operation.

The Time Of Propagation (TOP) counter will be the Particle IDentification (PID) system in the barrel region of Belle II. It will be used primarily to distinguish kaons from pions, a job that was performed in Belle by the Time Of Flight (TOF) and Aerogel Cherenkov Counter (ACC) systems. The TOP concept[2][3] is based on that of a Detection of Internally Reflected Cherenkov light (DIRC) counter[4]. In our case, this consists of a highly-polished quartz radiator bar which both generates Cherenkov light and propagates it via total internal reflection to a set of photosensors mounted at one end. The photosensors (Figure 1a) are Micro-Channel Plate PhotoMultiplier Tubes (MCP-PMTs), each with 16 anodes and an $\approx 40$ ps Transit-Time Spread (TTS)[5].

## 2. Readout electronics for the TOP counter

The overall timing resolution performance of the TOP is the quadrature sum of the timing resolutions of its constituent parts (the TTS of the PMT[5], TOP readout electronics and the timing distribution system[6]). Therefore the goal is a timing resolution for the readout electronics that is as low as possible, where ideally it does not contribute significantly to this quadrature sum.

The Application-Specific Integrated Circuit (ASIC; Figure 1b) consists of 8 channels of switched-capacitor array memory, allowing the capture and storage of time-sampled analog waveforms. The

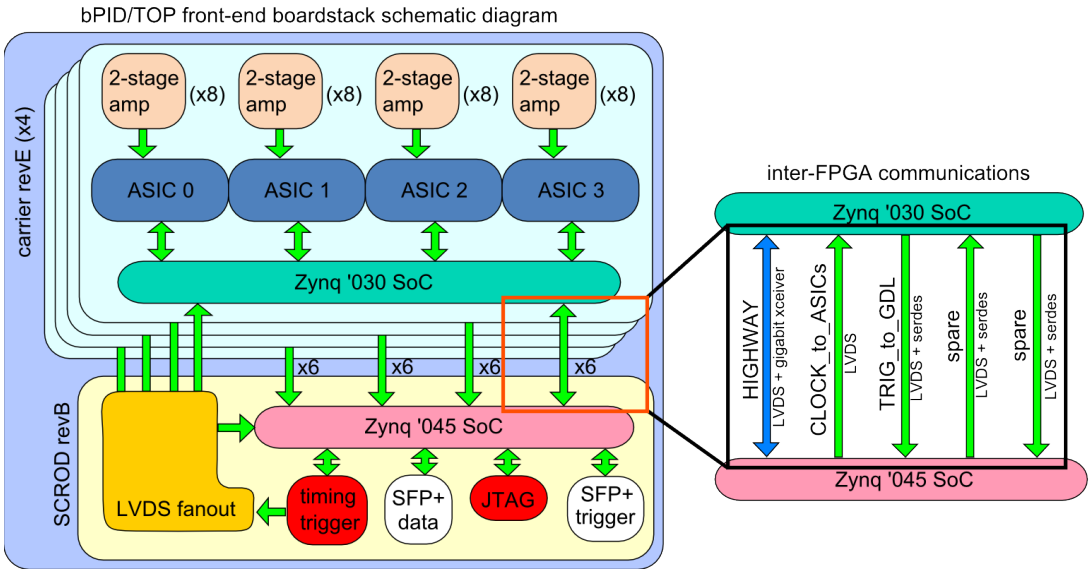


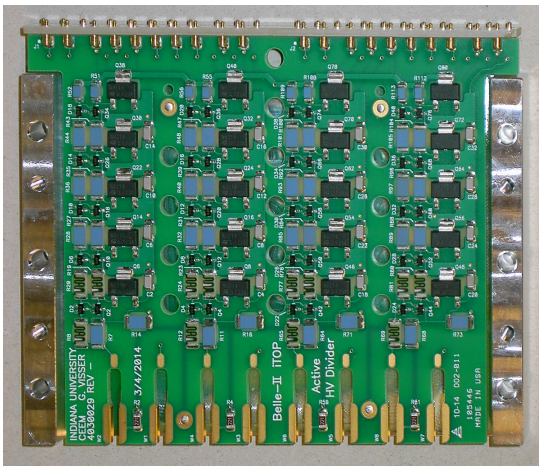

Figure 2: block diagram for a boardstack (1/4 of the readout for a TOP module) showing input amplifiers, waveform-sampling ASICs, FPGAs and the scheme for inter-FPGA communications.

analog storage is 32,768 samples deep for each channel, and with a nominal sampling rate of 2.7 GSa/s, this corresponds to an ability to record 12 $\mu$s of waveform before having to wrap around and overwrite the memory. Upon receipt of a system-level trigger, the ASIC will digitize the parts of the analog memory that are of interest using Wilkinson conversion. Digitization of groups of 64 samples occurs simultaneously for all channels in parallel using a Wilkinson ramp tuned to the speed of a clock feeding 12 bit counters. On-die comparators near the analog inputs provide a means for the TOP to ignore channels (during digitization selection and readout) that did not have a hit that crossed threshold. These 'trigger bits' are also used to determine the precise interaction t0, which is forwarded to the Global Decision Logic (GDL) to help reduce out-of-time hits for the Silicon Vertex Detector (SVD).

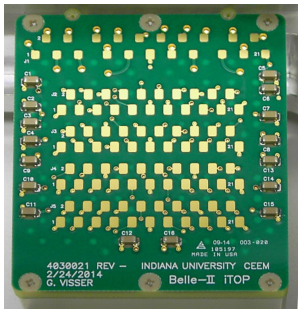
The block diagram in Figure 2 shows the basic flow of data from the 128 PMT anodes through amplifier chains to 16 ASICs, which are read out by four FPGAs when a system trigger[7] is received. After the data are read out, they are transferred to the controller FPGA which processes the data and extracts the hit time and an estimate of the charge collected on the anode for that hit. These feature-extracted data are then stamped with the system event number and sent through gigabit/s fiber optic links to the back-end Data AcQuisition system (DAQ)[8], where it is collected and associated with other data from other systems for offline analysis.

To deal with the expected data rate, the new electronics will use a more recent generation (Xilinx Zynq) of Field-Programmable Gate Array (FPGA) as compared to the previous version (Xilinx Spartan6). This is mainly because of advancements in semiconductor technology (over the intervening years since the upgrade was devised) but partly also to future-proof ourselves against the obsolescence of the tools to program them.

The limited space alloted for the TOP modules feeds the need for dense multilayer boards with fine-pitch components. The Belle II design specifies that the upgraded barrel PID system will fit in the same envelope as the TOF system. The magnet steel and barrel Electromagnetic CaLorimeter




(a) 'high voltage' board consisting of 8 channels of 400 MΩ resistive divider buffered with high voltage transistors to deliver voltages to the photocathode and MCPs of the PMT. Since the MCP resistance is fairly low (10 MΩ), a passive voltage divider with adequate regulation consumes significantly more power.




(b) 'front' board showing landing pads for spring-loaded pogo pins; reverse side has machined pin sockets installed in blind holes and holds four PMTs. This concept of mechanically decoupling the PMTs from the electronics has been tested successfully at a CRT at KEK.

Figure 3: HV and front boards

(ECL) will remain in place, and the space formerly occupied by the ACC will be used to expand the Central Drift Chamber (CDC).

### 2.1 PCBs

There are four unique Printed Circuit Board (PCB) designs for these front-end electronics. The 'HV' board is tasked with dividing 8 channels of high voltage (corresponding to the 8 PMTs on a boardstack; Figure 3a) to properly bias the photocathode and back-to-back MCPs. The 'front' board is for PMT mounting mechanics, high voltage distribution and anode connections for the raw analog signals (Figure 3b). This front board is 7 copper layers and is made with sequential lamination so that 'through-hole' pin sockets can be buried in the PMT side of the board and isolate the high voltage distribution from the readout electronics. Each of the 32 discrete amplifier chains (Figure 4) on the 'carrier' board (Figure 5a) takes the signal from a PMT anode and delivers it to a waveform-sampling ASIC where it is recorded in analog memory, and later digitized. The carrier board includes an FPGA to control and readout the ASICs. 'SCROD' (Figure 6a) is the control and readout board for each boardstack and it primarily consists of an FPGA, some Random Access Memory (RAM), timing distribution facilities and a pair of fiber optic transceivers to connect to the back-end DAQ. Both the carrier and SCROD boards have 12 copper layers, which is required to fit all the components and routing in the space allocated. The layer stackup for SCROD is shown in Figure 6b.

Improved performance comes at higher cost, with the new FPGAs drawing more power than before. Closely aligned with the power requirements are the thermal considerations. All power delivered to the modules is converted to waste heat and that must be removed from the detector to

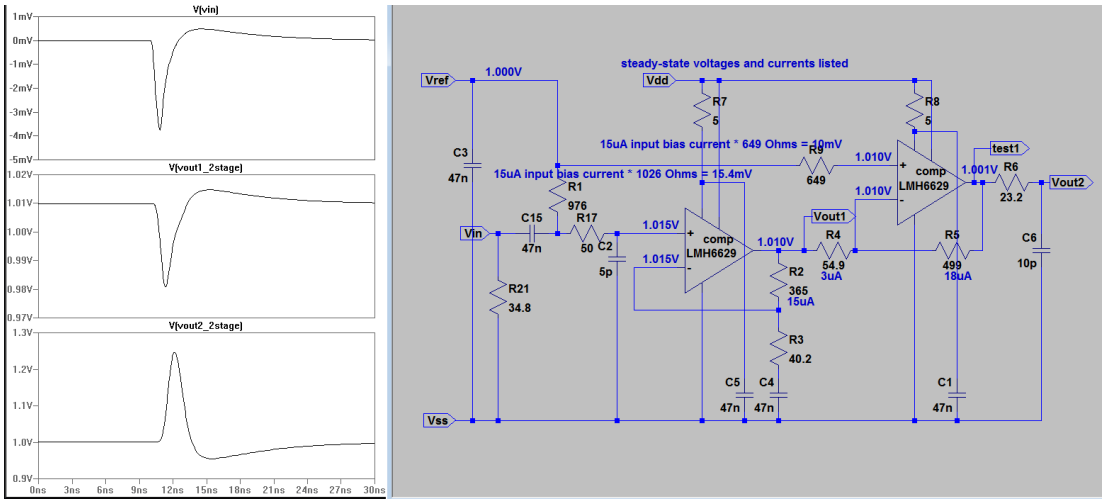
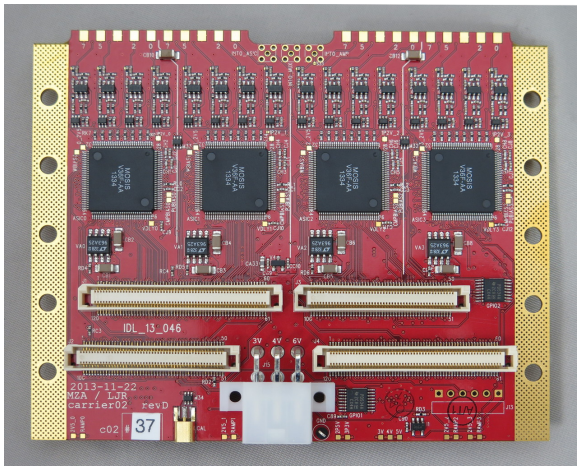
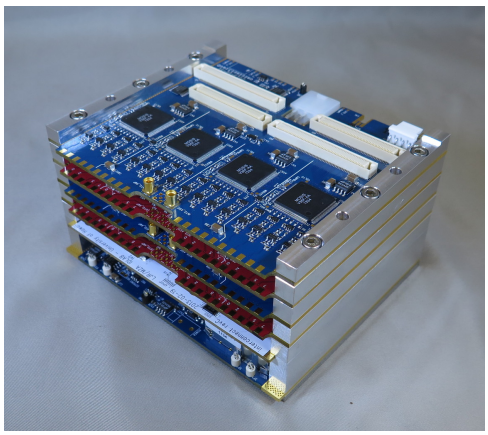



Figure 4: simulation showing test signal and amplified output from preliminary version of two-stage amplifier chain.



(a) previous revision of 'carrier' board, which houses amplifiers and ASICs. The final version will have twice as many discrete amplifiers and will have an FPGA.



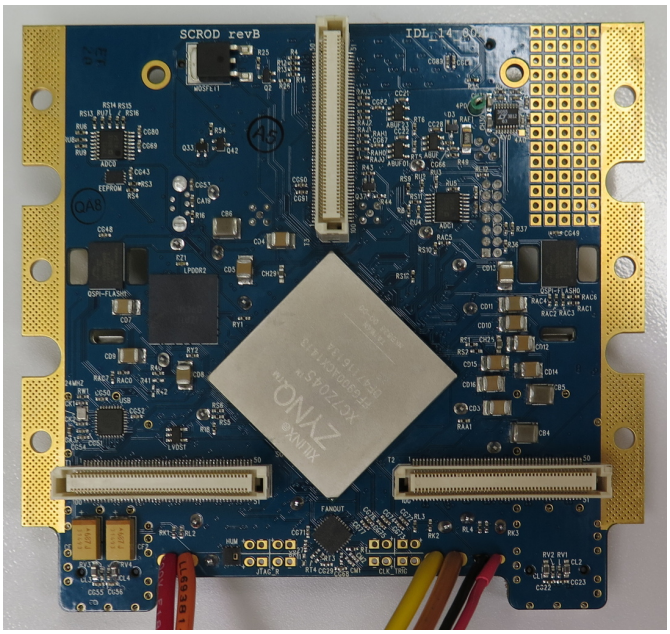
(b) current prototype 'intermediate' board-stack, showing thermal walls to conduct heat vertically to a cold plate.

Figure 5: carrier board and thermal walls

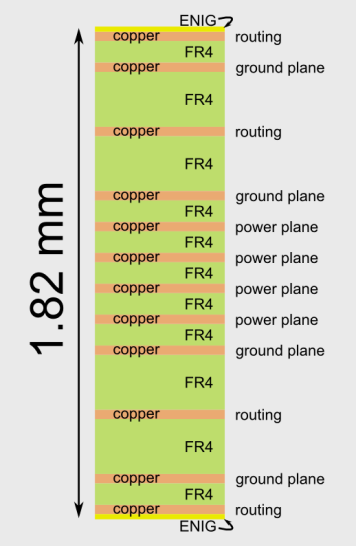
prevent thermal runaway. A system of chilled water will be circulated, with temperature and flow rate monitored on input and output during operation. To prevent condensation, the volume where the electronics are housed will be purged with a flow of nitrogen. Research is ongoing on exactly how best to couple the heat out from these boards in the limited space available (Figure 5b).

## 3. Previous incarnations

The ASICs and other electronics for this experiment have been developed by many people over the course of more than 10 years[3][5][9][10][11], and efforts continually improve upon previous




(a) new revision of 'SCROD' board, with controlling FPGA, RAM, dual multi-gigabit per second SFP connections to back-end DAQ, a clock fanout and power supply sequencing logic.




(b) scale drawing of 12 layer PCB stackup for SCROD.

Figure 6: SCROD board

work.

In mid-2012, we installed a previous version of this system at a Cosmic-Ray Test stand (CRT) at SLAC. It ran through the end of 2013, and the experience of operating it has provided valuable input on improvements to the Belle II PID system.

We took a later variant of these electronics to the SPring-8 testbeam facility in Hyogo Prefecture in Japan in mid-2013. The timing resolution during this beamtest was 95 ps, and the triggering efficiency was $\approx 75\,\%$, as it used a discrete amplifier circuit with a low gain. The resultant ring image is shown in Figure 7. Vertical bands are due to poor optical coupling and dead channels; a new concept for mechanics (Figure 3b) should alleviate the poor optical coupling.

## 4. Timing resolution performance

The timing resolution (Figure 8) for the current electronics is below 65 ps and the efficiency is above 95 % (improvements are due primarily to using an amplifier circuit with a higher gain). To improve this timing performance further, we now have a two-stage amplifier chain and new designs for the ASIC and PCBs.

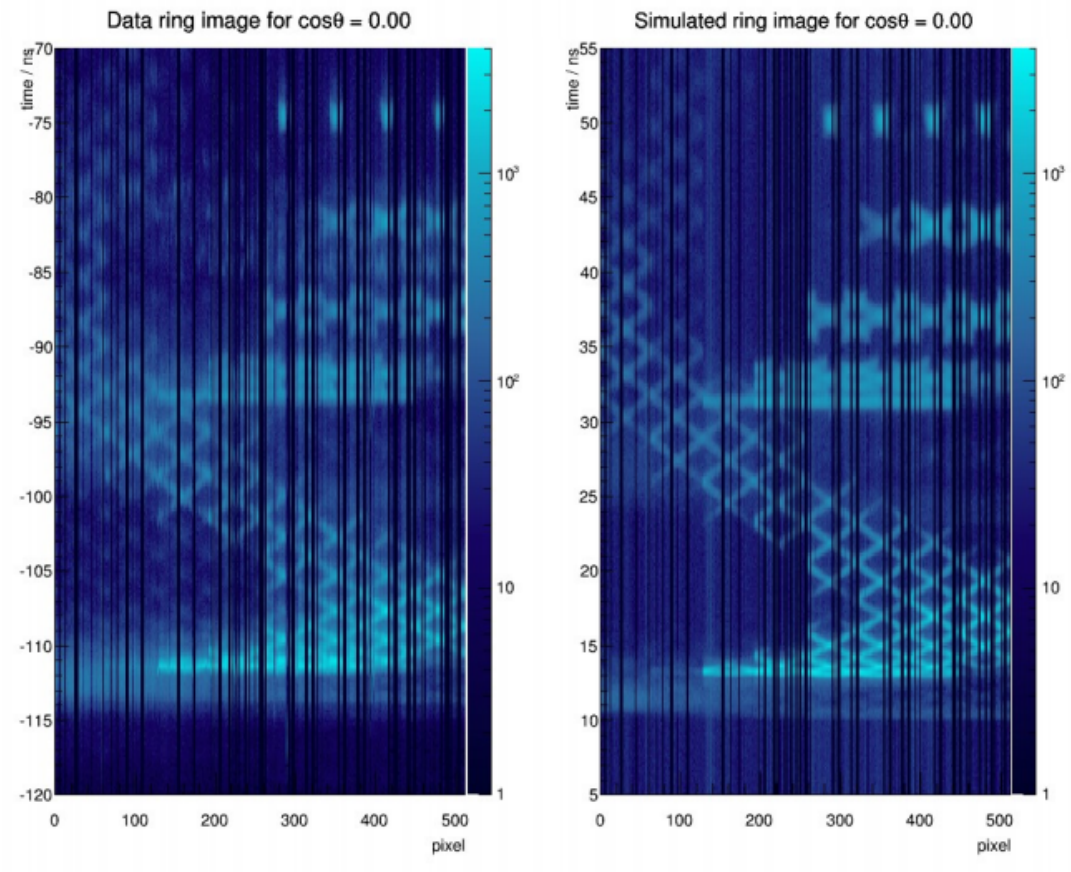



Figure 7: folded ring image of the type expected in the TOP counter during operation of Belle II.

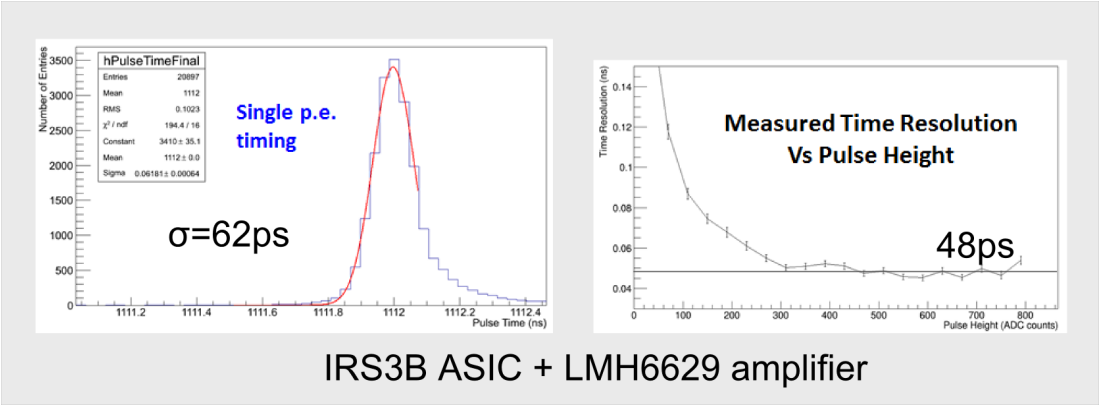



Figure 8: time resolution as a function of pulse height, showing the need to get more signal from the amplifier chain.

## 5. Conclusion

We have demonstrated a functional prototype for the front-end electronics for the TOP counter for the Belle II detector. To obtain desired improvements, we have pursued avenues such as using a newer generation FPGA, adding a second stage to the discrete amplifier circuit and a refined ASIC design. Final prototyping is commencing now, and with production beginning later this year, the TOP counter is on track to be installed in Belle II in 2015.

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