PROCEEDINGS OF SCIENCE

Concepts for Pre-Assembly Data Acquisition for the PANDA Experiment

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The PANDA detector will be a located at the high energy storage ring (HESR), at the facility for anti protons and ion research (FAIR) in Darmstadt, Germany.

It will operate with a very high interaction rate of up to 20 MHz, in a free streaming mode without hardware trigger. Data filtering will be performed by complete online event recontruction with a highly parallelized farm of FPGAs as first level and on a farm of GPUs or PCs as a second level. The requirement is a background reduction by a factor of > 1000.

Parts of the PANDA detector will be pre-assembled and tested at the Forschungszentrum Jülich, before being transported to GSI at a later stage. The data acquisition (DAQ) system for the pre-assembly comprises two different kinds of FPGA boards for data concentration, event building and filtering. In this contribution, we present the DAQ system for the pre-assembly for PANDA, which will have up to 36 optical links as inputs and Gb/Ethernet as output.

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1. PANDA Experiment

The PANDA (anti-Proton ANnihilations at DArmstadt) experiment is a fixed target experiment at the future Facility of Antiproton and Ion Research (FAIR)[2]. It will investigate $\bar{p}$ + p and $\bar{p}$ + A collisions with various internal proton (p) or nuclear (A) targets, using a high precision anti-proton ($\bar{p}$) beam with momentum resolutions of $\frac{\Delta p_{beam}}{p_{beam}} \leq 4 \times 10^{-5}$ in a range from 1.5 GeV/c to 15 GeV/c[1]. This will allow precise researches in an energy regime from 2.5 GeV to 5.5 GeV. The main focus of the PANDA physics program are proper measurements to investigate the nature of the strong interaction in the non-pertubative region and exploring the QCD spectrum as well as the structure of the hadrons. It covers charmonium spectroscopy above and below open charm threshold, likewise searches for exotic states like tetra quarks, glueballs and hybrids. Other topics of the program are open charm spectroscopy, hypernuclear physics, electromagnetic processes and also studies of hadrons in matter[3]. Even the high precision electron positron experiments and their currently planned updates can not reach this spectrum especially not in the charm quark sector, because of the limitation to the quantum numbers of the virtual photon. In this context the PANDA experiment will be unique. It will prove both statistics and precision of existing data and furthermore explore the physics in the charm quark sector.

The PANDA detector will consist of 16 sub detectors distributed to a target spectrometer (TS) and a forward spectrometer (FS). Both spectrometers together will cover a polar angle from 5 deg to 170 deg according to the beam axis z. Thus the acceptance of the PANDA detector will be almost 4π[3].

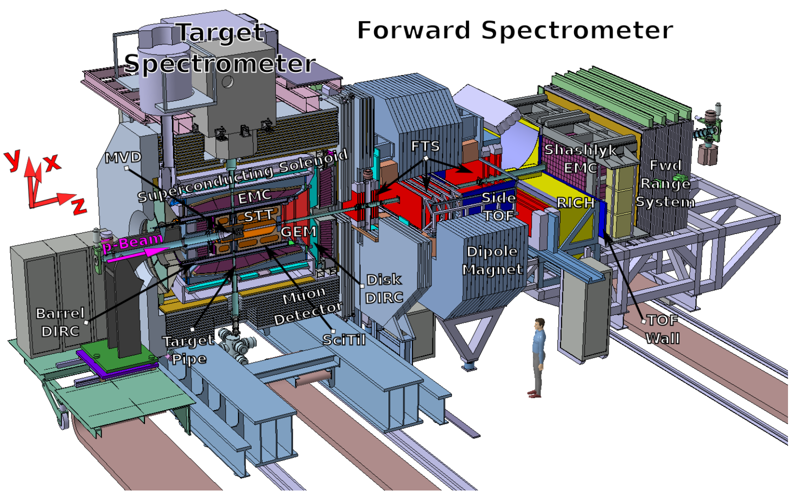

Figure 1: Schematic view of the PANDA detector, a fix target experiment divided into two parts: a target spectrometer and a forward spectrometer. The PANDA detector will consist of 16 sub detectors: The micro vertex detector (MVD), the straw tube tracker (STT), forward tracker (FTS) the forward Gas Electron Multiplier (GEM) detectors, Detection of Internally Reflected Cherenkov (DIRC) one in the barrel and one in forward direction, electromagnetic calorimeter (EMC), Muon Detectors, Scintillator Tile Barre (SciTil), a Time of flight (TOF) in the FS

2. The PANDA Data Acquisition (DAQ)

The PANDA DAQ will be a system operating in a free steaming mode without any hardware trigger. According to the high average interaction rate of 20 MHz with a peak up to 50 MHz and an event size of a few kilobyte it will handle a data rate of several hundreds of GB/s before storage. This data rate has to be reduced by at least three orders of magnitude. The reduction will be achieved by filtering the events online using information from tracking, calorimetry and particle identification. Because of high interaction rate the PANDA DAQ has to handle an other feature, the read out time of some of the sub-detectors is larger than the time between two interactions and thus overlapping of events occurs. Since there is no hardware trigger a different kind of data synchronization has to be done, by using SODANET [7] (synchronization of data acquisition) time stamps distributed to all sub-systems. The trigger-less operating is due to the fact that background events have similar topological signatures than benchmark channels. Here, the events will be fully reconstructed and disentangled online on a highly parallelized and pipelined architecture including FPGAs, (field programmable gate arrays), GPUs (graphics processing unit) and PCs farms.

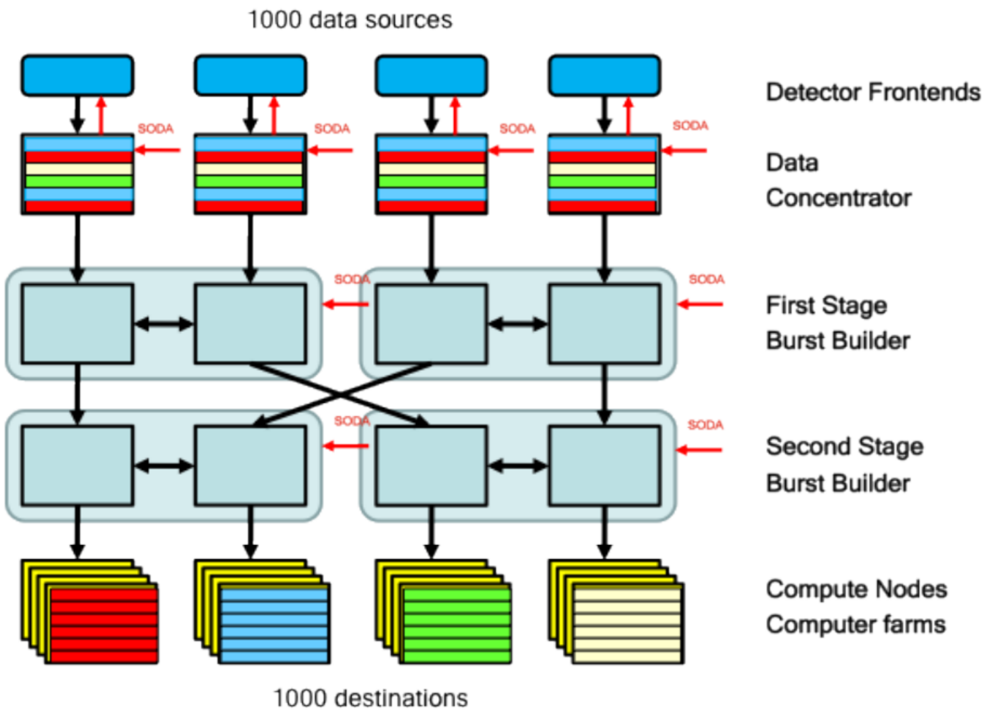

Figure 2: The PANDA DAQ has to handle a very high data rate, with has to be reduced be at leased a factor of more then 1000. This will be achieved in a hierarchical way. The first part will be burst building, which is clustering and sorting the data, and the second stage will be reconstructing, entangling and filtering the data.

2.1 Hardware

The FPGA base hardware for the PANDA DAQ will be the so called Compute Node (CN). The revision 3 of the CN is an ATCA (advanced Telecommunication Computing Architecture) based carrier board, for carrying up to 4 xFP boards. A xFP board is an extended Telecommunications Computing Architecture (xTCA) compliant board. The CN is equipped with a Xilinx Virtex 4FX60, as a switching FPGA to connect the xFP boards in an intelligent way to the backplane. It supplies also direct high speed communications between these boards via rocked I/O[5].

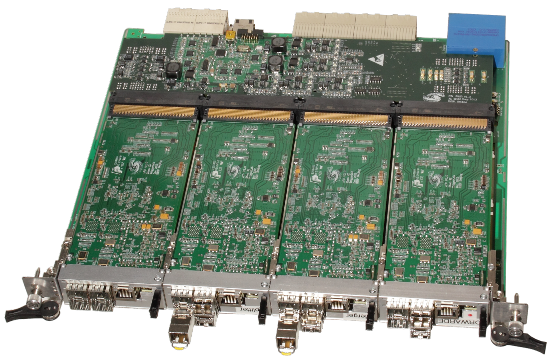

Figure 3: Compute Node revision 3, ATCA based carrier board, carrying 4 xTCA compliant boards[5].

The xFP board is a FPGA based board with a μTCA form factor, featuring a Xilinx Virtex 5FX70T-2 FPGA, 2 x 2 GB DDR2, 1 Gb Ethernet, and 4 SFP+(Small Form- Factor Pluggable) cages. These cages can be equipped for example with optical or RJ45 interfaces [5].

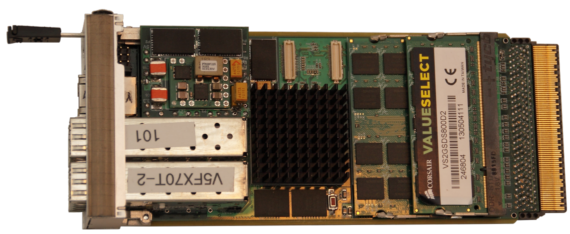

Figure 4: xTCA compliant board, a FPGA based board with a μTCA form factor, featuring a Xilinx Virtex 5FX70T-2 FPGA, 2 x 2 GB DDR2, 1 Gb Ethernet, and 4 SFP+(Small Form- Factor Pluggable) cages.[5]

3. The Prototype Trigger-less DAQ for PANDA

Due to the fact that it is planned to pre-assemble the PANDA detector at the Research centre Jülich, a preliminary kind of DAQ has to be built. It will be a DAQ system with similar components and similar functionality as the PANDA DAQ. This will be realised in three steps. As a first step the prototype trigger-less data acquisition (PTDAQ), a small but scalable start version, is prepared. It will be used for testing sub detector prototype, as well as testing the online reconstruction algorithms.

The next step is an extended version which includes the CN. This version can than be expanded to the final pre-assembly DAQ.

The PTDAQ consists of up to 4 xFP boards plugged in a μTCA shelf. It is driven by up to 9 data concentrators (DC) connected via optical links. The DCs process the received digitalized data from sub-detector front-end electronics (FEE). One of their purpose is adding the SODANET time stamp to the data and they also do feature extraction. A possibility for a DC is the TRBv.3 (trigger and readout board) an FPGA based board equipped with 5 Lattice ECP3 [6].

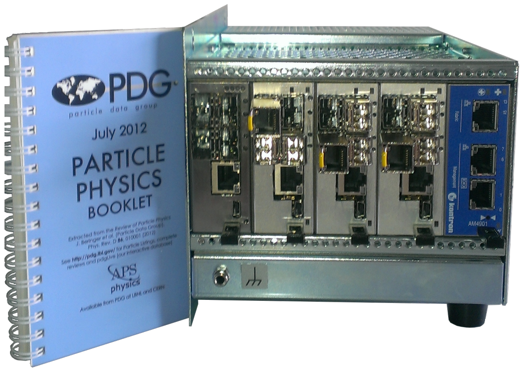

Figure 5: The PTDAQ setup consist of up to 4 xTCA compliant boards plugged in μTCA shelf.

The functionality that is provided by the PTDAQ so far is clustering the incoming data according to their SODANET time stamp into bursts. Due to the fact that the interaction rate during the prototype test is smaller then it will be in the PANDA experiment, bursts from a single sub-detector are used for sub-event building. The sub-events of all used sub-detectors can be combined to events. Each step of the Data Acquisition chain features optional event filtering.

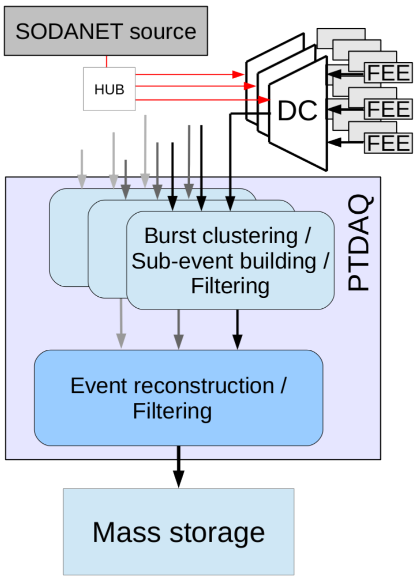

Figure 6: Schematic of the PTDAQ functionalities, the PTDAQ will be used as a prototype of the PANDA DAQ.

4. Summary & Outlook

To summarize the pre-assembly DAQ of the PANDA experiment will be established in three steps. The first step is the already existing PTDAQ. It is a small but scalable start version using similar hardware components then the later PANDA DAQ. It is foreseen that parts of the functionalities of the PANDA DAQ, like the reconstruction and filler algorithms will be implemented for testing reasons. PTDAQ provides burst clustering, sub-event and event building. Its functionalities has been tested on hardware by using emulated data concentrators.

As a next step the PTDAQ will be tested with real data concentrators. Later, a full DAQ chain during prototype tests with beam at the Forschungszentrum Jülich. The second step will be a extended version using one or two ATCA based Compute Nodes. This system can be upgraded to the final pre-assembly DAQ for PANDA.

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